Ancillary ASIC - test preparations

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for SVT WP2

January 21, 2025, ePIC Collaboration Meeting, Frascati

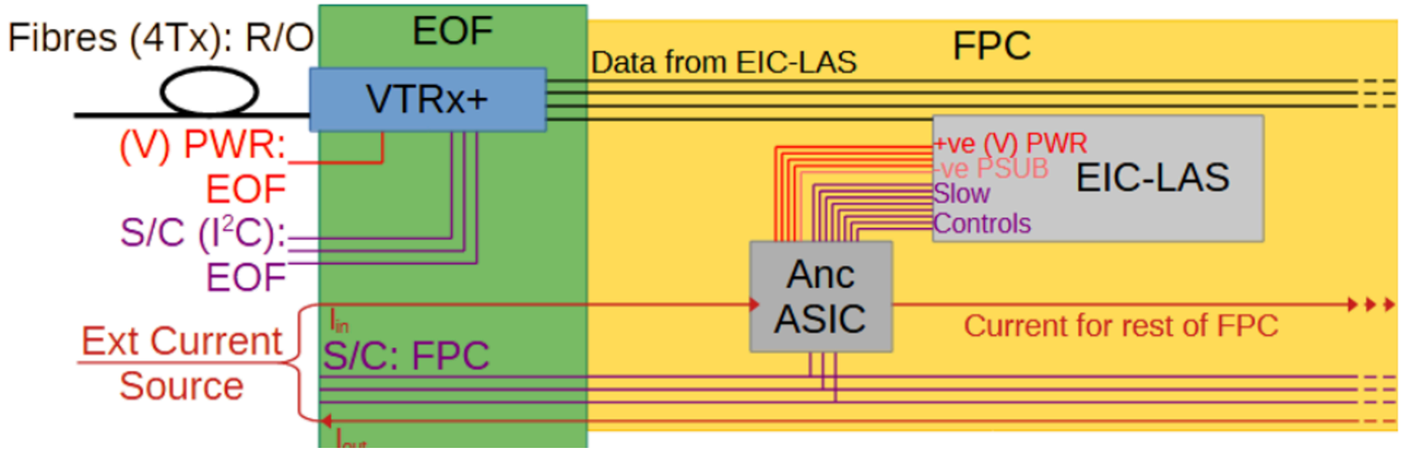
AncASIC

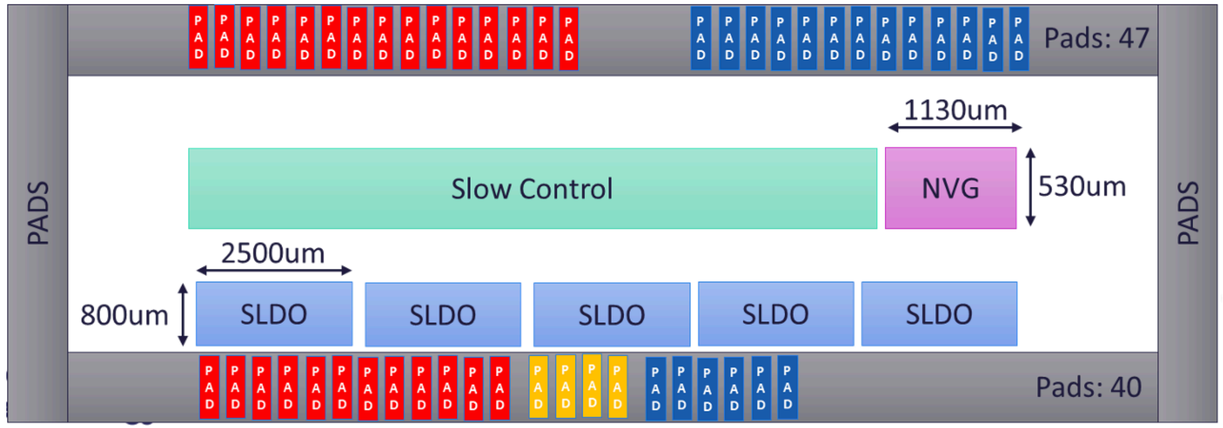
Main blocks:

- Negative Voltage Generator NVG
- SLDO
- Slow Control

(4) development stages (preliminary):

- MPW1, 2, 3, x - prototype (chiplets)
- ER AncASIC production on 8“ wafers





MPW1/MPW2

Main blocks MPW1:

- Negative Voltage Generator (NVG)
- SLDO Pre-Regulator
- CML Transceiver
- Transistor Test Structures (for radiation hardness validation of XT011 process)

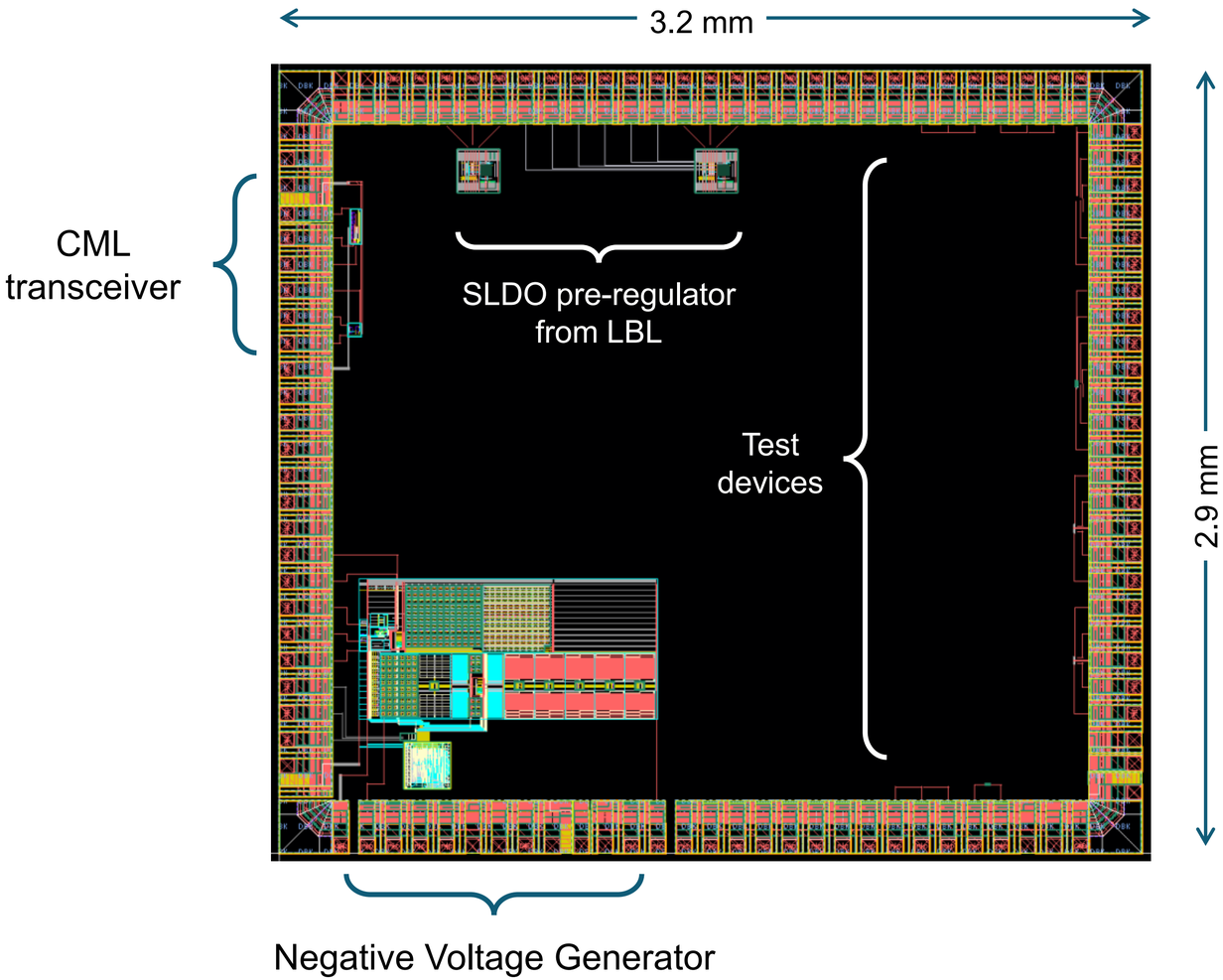
MPW2:

- SLDO

Details:

- 45 individual chipsets for each MPW
- Number of available pads = 110
- Submission is planned to May 2025
- **Delivery from the fab in September 2025**

1st Prototype: AncASIC sub-blocks and test devices



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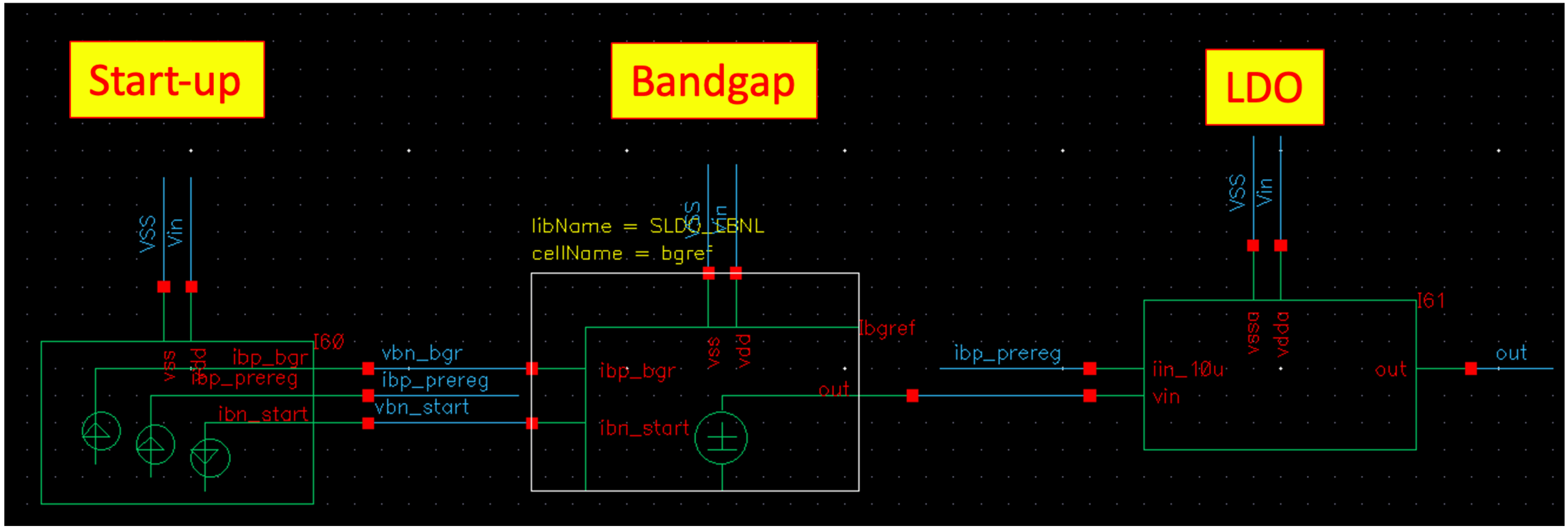
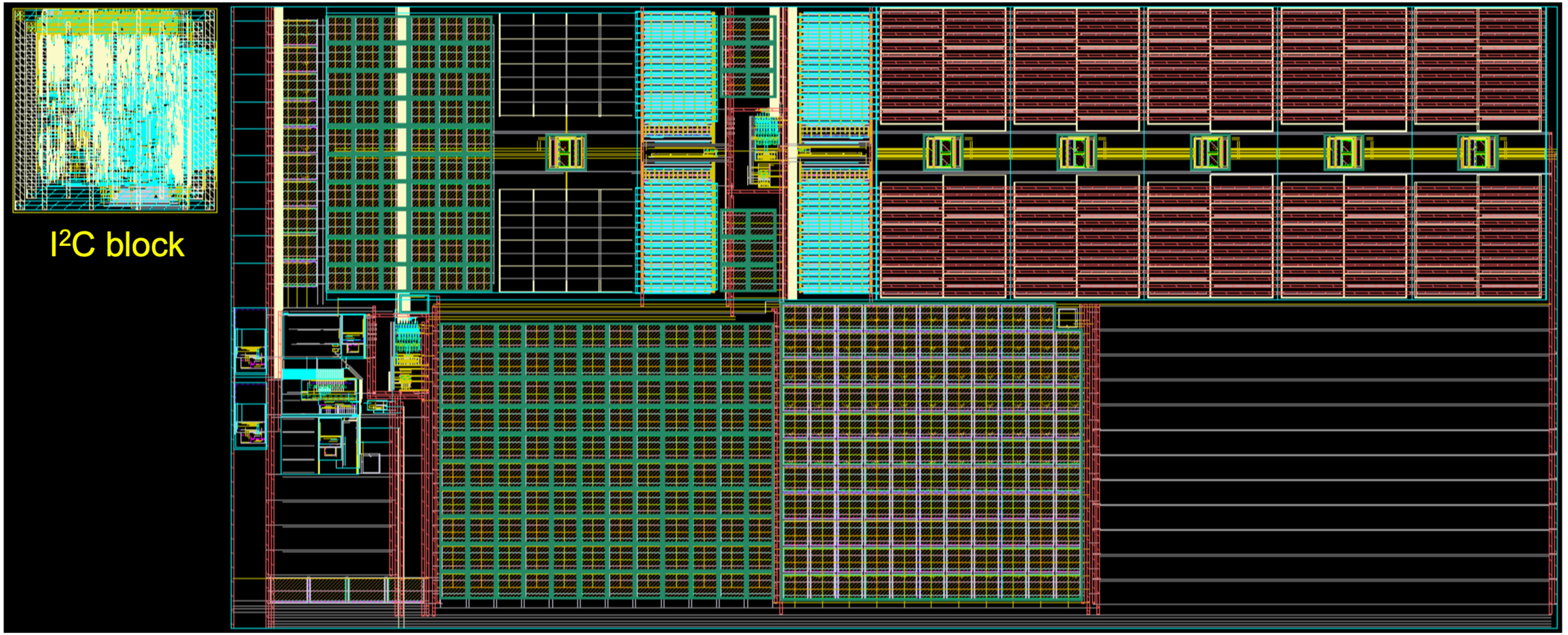
MPW1 - SLDO Pre-Regulator



- Power source
- Measure output and some internal signals

MPW1 - NVG



- Power source
- I²C control via FPGA
- Measure output voltage (default -3V)

MPW1 - Transistor Test Structures

- LVTs
- BJT
- MOSVC Capacitor
- Resistor

- Transistor charasteristics scan
- IV measurement
- LCR meter

- nelvt
  - W=1u, L=110n
  - W=1u, L=150n
  - W=1u, L=500n
  - W=1u, L=1u
- pelvt
  - W=1u, L=110n
  - W=1u, L=150n
  - W=1u, L=500n
  - W=1u, L=1u

- BJT
  - qpva
  - qpvb
- mosvc (7u x 7u cell)
- Rpp1 (w=3u and l=20u)
- nelvt, pelvt
  - Weff. = 100um, L=150nm
  - Interdigitation layout to measure leakage
  - Two copies
    1. minimum DTI enclosure spacing
    2. 1.0um DTI enclosure spacing

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MPW1/MPW2 testing needs

- PCB carrier board
- Standard test equipment (power sources, IV, LCR meters, oscilloscope etc.)
- Transistor test structure IV setup
- Temperature chamber
- I^2C FPGA control for NVG
- Irradiation (X-ray, Cobalt-60) - TID up to 1MRad
- (SEE/SEU of I^2C in a proton beam)

Testing details defined by WP1:

- https://docs.google.com/spreadsheets/d/1VWeK98f8jZUxhvNr1PAeVBIMx0neTcvY2W6wPgqrf0A/edit?usp=sharing

MPW1/MPW2 - Task list

	MPW1			
	Task	**Testing details, conditions**	**Comments**	**Equipment**
	MPW1 tapeout/submission (WP1 task)			
	MPW1 testing			
1	**Test specs definition**			
2	**Carrier board PCB design + manufacturing, pre-testing**			
3	**Chip+PCB assembly, wirebonding**			
4	**SLDO Pre-Regulator characterization**			Standard lab equipment (power supply, IV meters, oscilloscope etc.)
	Output Ripple/Noise	Load Capacitance - 1pF, **10pF**, 100pf, 1nF	Number in red is the expected value. Others are for exploring the parameter space	
	Transient Response (overshoot and settling time)	ESR - **3.5k**		
	PSRR and line regulation	Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber
	Start-up	Standard Radiation Range	0 - 1MRad in 100kRad steps	
		Ramp rate - 10u, 100u, **1m**, 10m, 100m, 1s		
5	**NVG characterization**			Standard lab equipment (power supply, IV meters, oscilloscope etc.) **I2C control via FPGA**
	Output Ripple/Noise	Load Capacitance - RANGE?		
	Transient Response (overshoot and settling time)	Frequency - RANGE?		
	PSRR and line regulation	Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber
	Start-up	Standard Radiation Range	0 - 1MRad in 100kRad steps	
		Standard Supply Variation	Plus and Minus 20%	
		Ramp Rate - RANGE?		
	Test in combination with APTS/DPTS/ER1		Use NVG to generate back bias for already existing APTS and DPTS chips	
6	**Transistor Test Structures characterization**			Standard lab equipment (power supply, IV, LCR meters, oscilloscope etc.)
	Ids vs Vgs			TTS characterization IV setup
	Vt extraction			
		Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber
		Standard Radiation Range	0 - 1MRad in 100kRad steps	
		Standard Supply Variation	Plus and Minus 20%	
7	**CML transciever**			
8	**Irradiation**			
		X-rays Cobalt60	Chips powered during the irradiation, temperature monitoring	
		Standard Radiation Range	0 - 1MRad in 100kRad steps	
9	**SEE/SEU Tests in a proton beam**			Proton beam with XY table

MPW3/MPWx

Main blocks:

- Negative Voltage Generator NVG
- SLDO
- Slow control

Details:

- 45 individual chipsets ?
- Functionality and layout „identical“ to the final AncASIC

Testing needs:

- PCB carrier board with connectors compatible with existing FPGA controls for slow control
- Probe card prototyping if pin-out changes are not expected
- Standard test equipment (power sources, IV meters, oscilloscope)
- Temperature chamber
- Slow control FPGA code
  - (Jo Schambach/ORNL works on MOSAIX emulator, BNL and LBNL AncASIC emulator slow control on FPGA)
- Irradiation (X-ray, Cobalt-60) - TID up to 1MRad
- SEU/SEE tests of the sensitive digital circuits in a proton beam

MPW3 - Task list

	MPW3			
	Task	**Testing details, conditions**	**Comments**	**Equipment**
	MPW3 tapeout/submission (WP1 task)			
	MPW3 testing			
1	**Test specs definition**			
2	**Carrier board PCB design + manufacturing, pre-testing**			
3	**Chip+PCB assembly, wirebonding**			
4	**SLDO characterization**			Standard lab equipment (power supply, IV meters, oscilloscope etc.)
	Output Ripple/Noise	Load Capacitance - 1pF, **10pF**, 100pf, 1nF	Number in red is the expected value. Others are for exploring the parameter space	
	Transient Response (overshoot and settling time)	ESR - **3.5k**		
	PSRR and line regulation	Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber
	Start-up	Standard Radiation Range	0 - 1MRad in 100kRad steps	
		Ramp rate - 10u, 100u, **1m**, 10m, 100m, 1s		
5	**NVG characterization**			Standard lab equipment (power supply, IV meters, oscilloscope etc.)
	Output Ripple/Noise	Load Capacitance - RANGE?		
	Transient Response (overshoot and settling time)	Frequency - RANGE?		
	PSRR and line regulation	Standard Temperature Range	-20, 27, 60, 105 C	Temperature chamber
	Start-up	Standard Radiation Range	0 - 1MRad in 100kRad steps	
		Standard Supply Variation	Plus and Minus 20%	
		Ramp Rate - RANGE?		
	Test in combination with APTS/DPTS/ER1		Use NVG to generate back bias for already existing APTS and DPTS chips	
6	**Slow control characterization**			Standard lab equipment (power supply, IV meters, oscilloscope etc.), **Slow Control FPGA**
7	**Irradiation**			
		X-rays Cobalt60	Chips powered during the irradiation, temperature monitoring	
		Standard Radiation Range	0 - 1MRad in 100kRad steps	
		SEU/SEU tests of digital circuits in a proton? beam		
8	**SEE/SEU Tests in a proton beam**			Proton beam with XY table

AncASIC production

Main blocks:

- Negative Voltage Generator NVG
- SLDO
- Slow control

Details:

- ER production on 8“ wafers
- Production tested on wafer probing machine before dicing

Testing needs:

- Probe card design, manufacturing, pre-testing (might be developed already in the previous MPWx)
- Wafer probing HW/FW/SW control setup
  - could be used modification of MOSAIX/LAS setup, for the slow control FPGA code AncASIC emulator
- Production database for storing the test results (common DB used also for the sensor testing etc.)
- Wafer prober + physical testing of the production wafers

AncASIC - Task list

	AncASIC final
	Task
	AncASIC production (WP1 task)
	AncASIC testing
1	**Test specs definition**
2	**Probe card design, manufacturing, pre-testing**
3	**Database for testing results**
4	**Wafer probing HW/FW/SW control setup**
5	**Production testing on wafer prober**

Task List comments

Close collaboration with WP1 necessary to define test parameters and report the results back to AncASIC designers during prototyping.

Carrier board PCB design

Manufacturing of PCB for Carrier board
Manufacturing of PCB for probe card

Pre-testing of carrier board and probe card

Slow control test setup:
- Assumption is that the readout and testing is done via FPGA based emulator system designe by BNL/LBNL
  - Any help needed?

General questions:
- Results analysis and performance definition
- DB structure needed to store the analysis results and general characterization
- Software integration needs to automatize testing procedures

Conclusion

The purpose of this presentation is to show the tasks that will need to be completed for prototype testing and production of AncASIC. The list of tasks and tests is not final, it will of course be revised and **we would be happy to receive any input here.**
We have preliminary applicants for some tasks, but most are available for volunteers from the SVT collaboration to join. We need to collect interest and people that can do the work. So please think about which tasks your group wants to participate in and let us know, because very soon it will be necessary to assign the responsibility for the tasks at least for MPW1/2.

At the same time as the assignment of tasks, it will be necessary to think how to divide chips from MPWs' into tasks/groups.