MOSAIX
&
EIC-LAS Modifications

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João de Melo - BNL
jmelo@bnl.gov

Outline

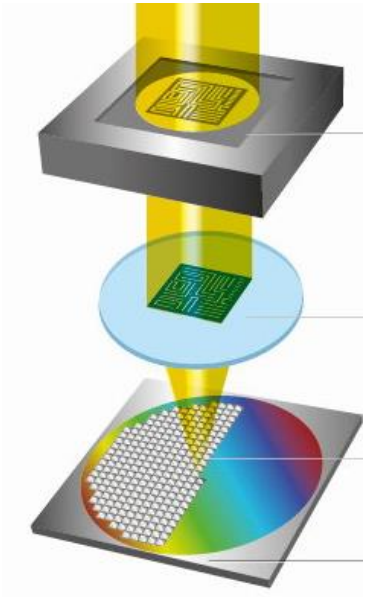
- Monolithic Stitched Sensor (ER1 Submission)
  - Introduction
- MOSAIX (ER2 Submission)
  - Architecture (Alice/ITS3 upgrade)
  - Design Status
- MOSAIX to EIC-LAS
  - Modifications
  - Timeline & Resources
  - Further Improvements!?

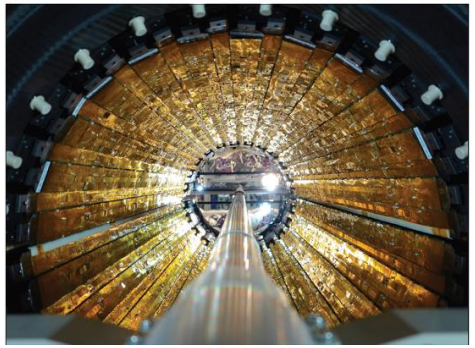
Introduction

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - Typical sizes of few cm^2
  - modules are tiled with chips connected to a flexible printed circuit board

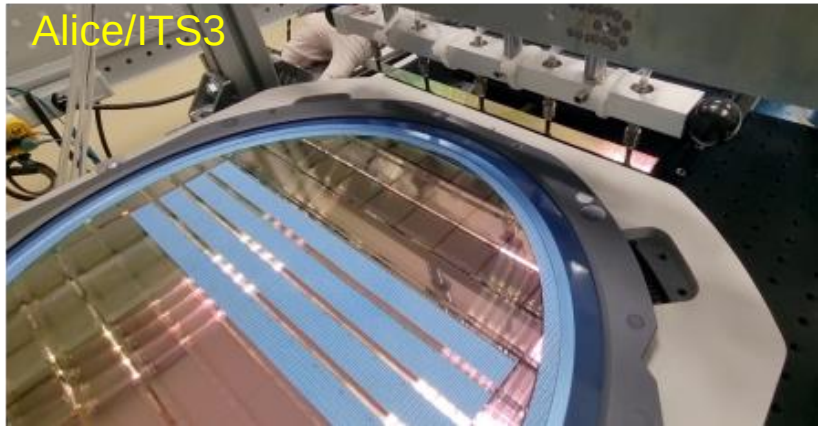
- Wafer-scale sensors: stitching
  - New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - wafer-size chip

Principle of photolithography





Alice/ITS2

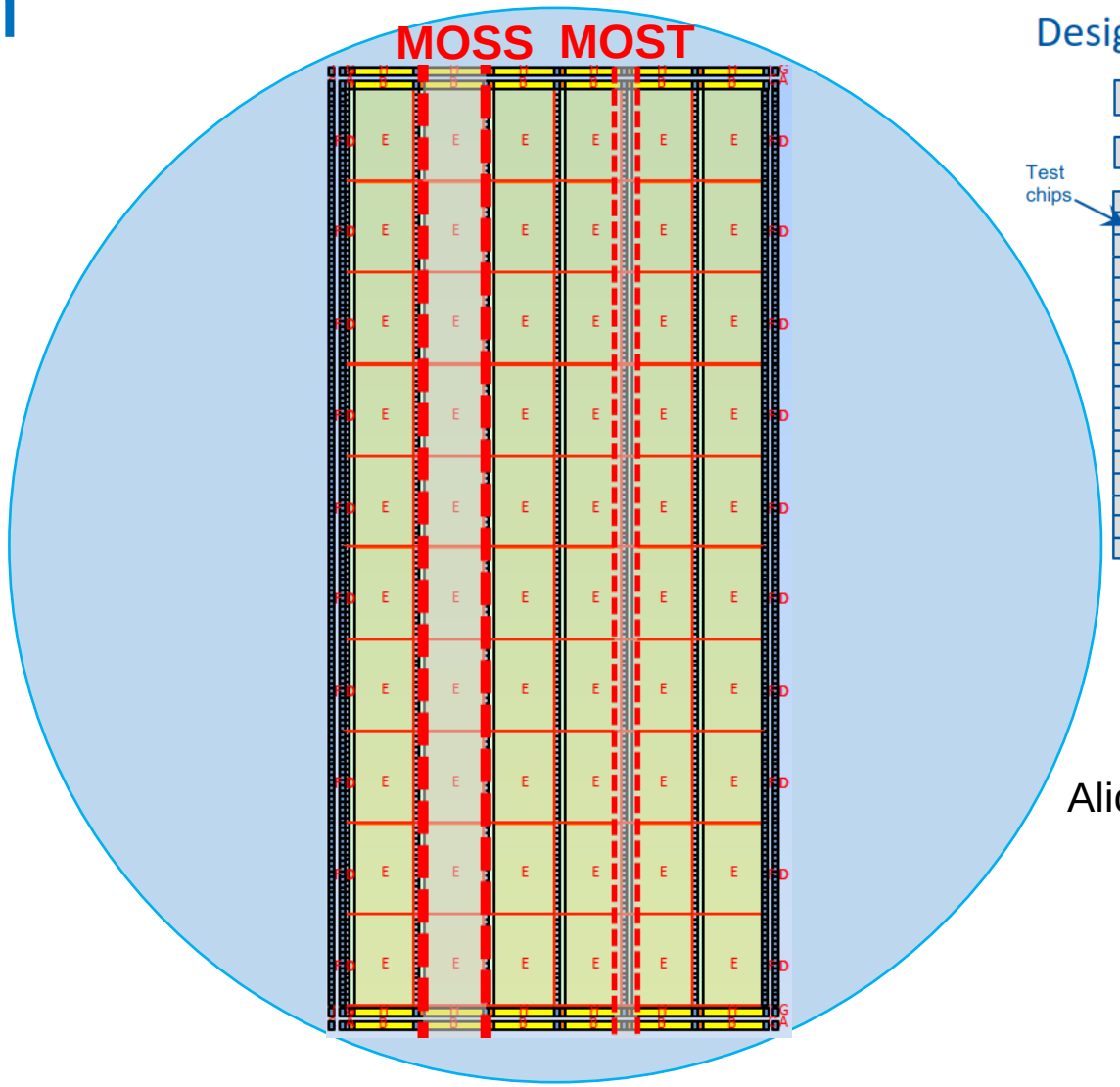


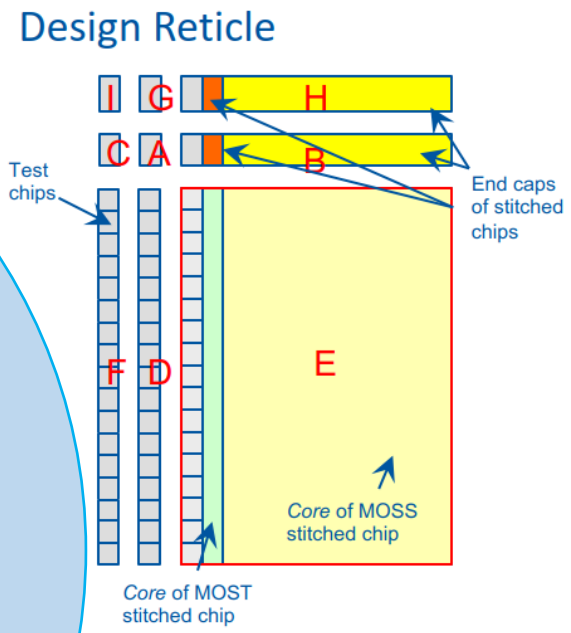
Motivation: Reduction of the material budget

Challenges: Power supply, cooling, and design/yield

ER1 Submission

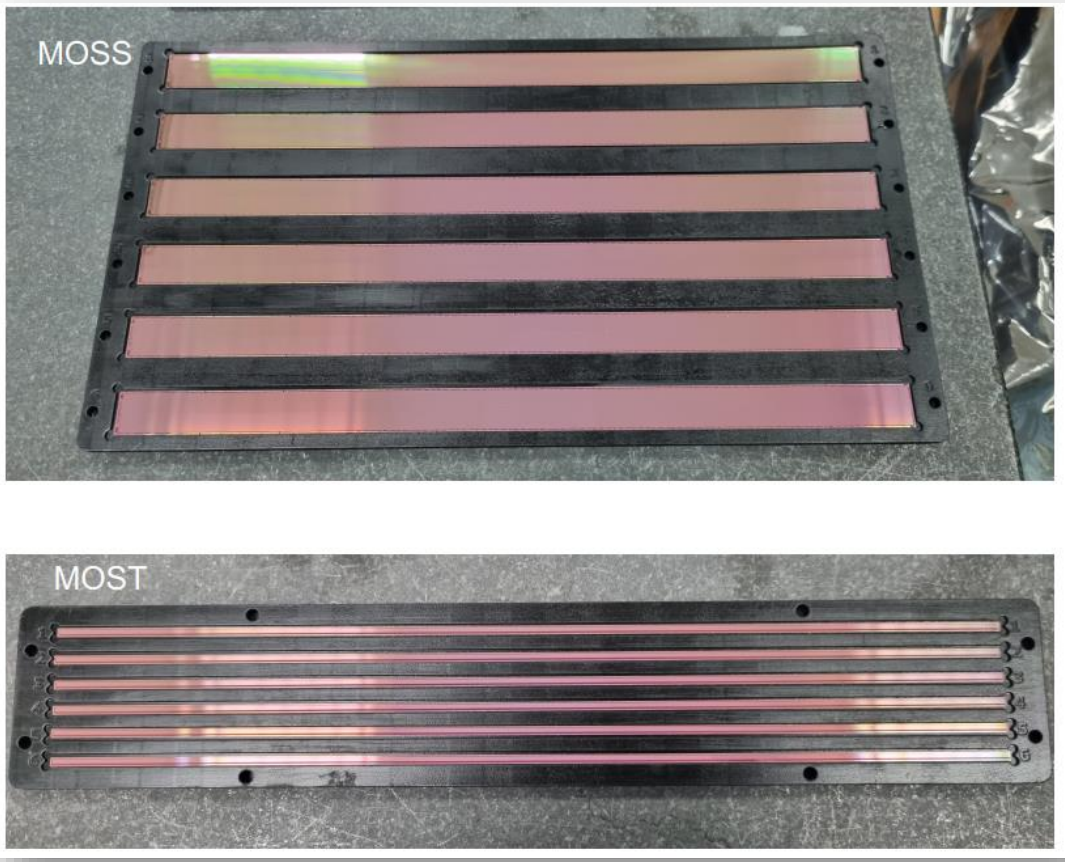
- Learn and prove stitching
- Two large stitched sensor chips (MOSS, MOST)
- Different approaches for resilience to manufacturing faults
- Small test chips (Pixel Prototypes)

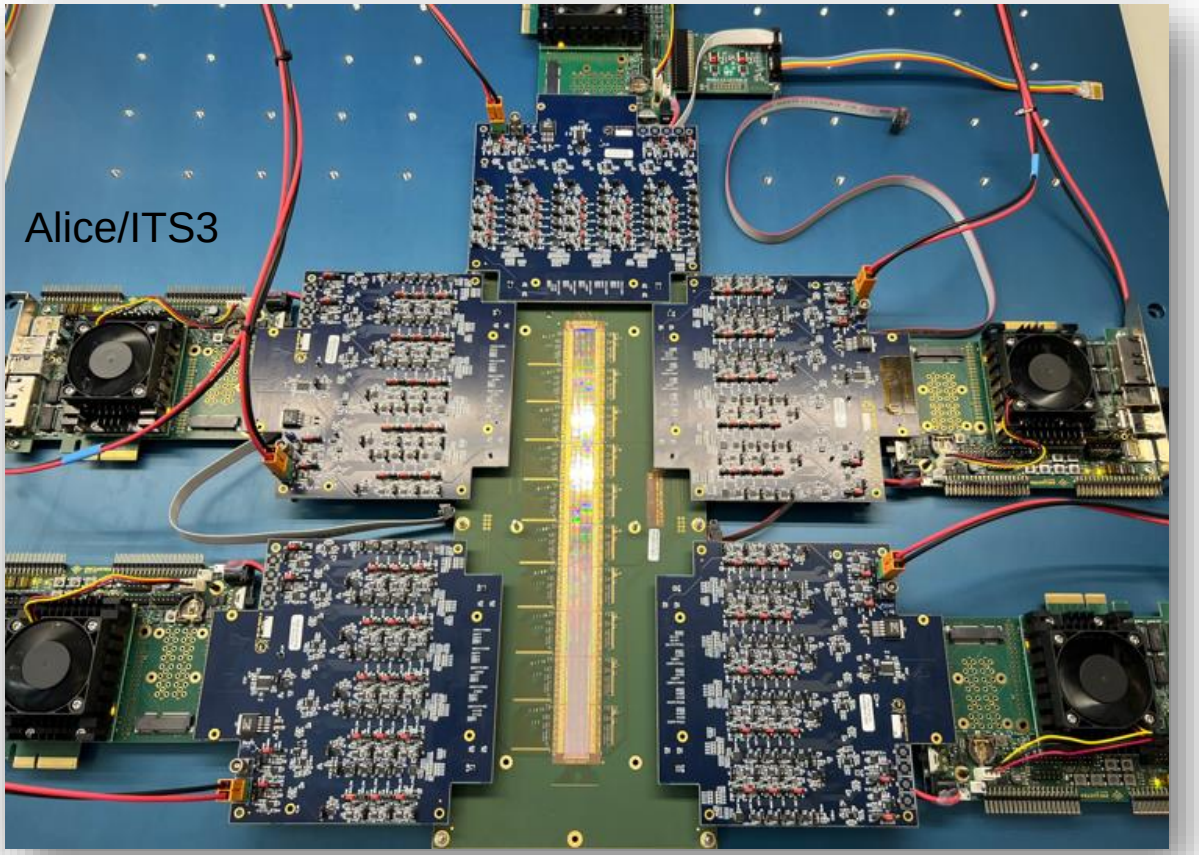




Alice/ITS3

ER1 Dicing and Test System

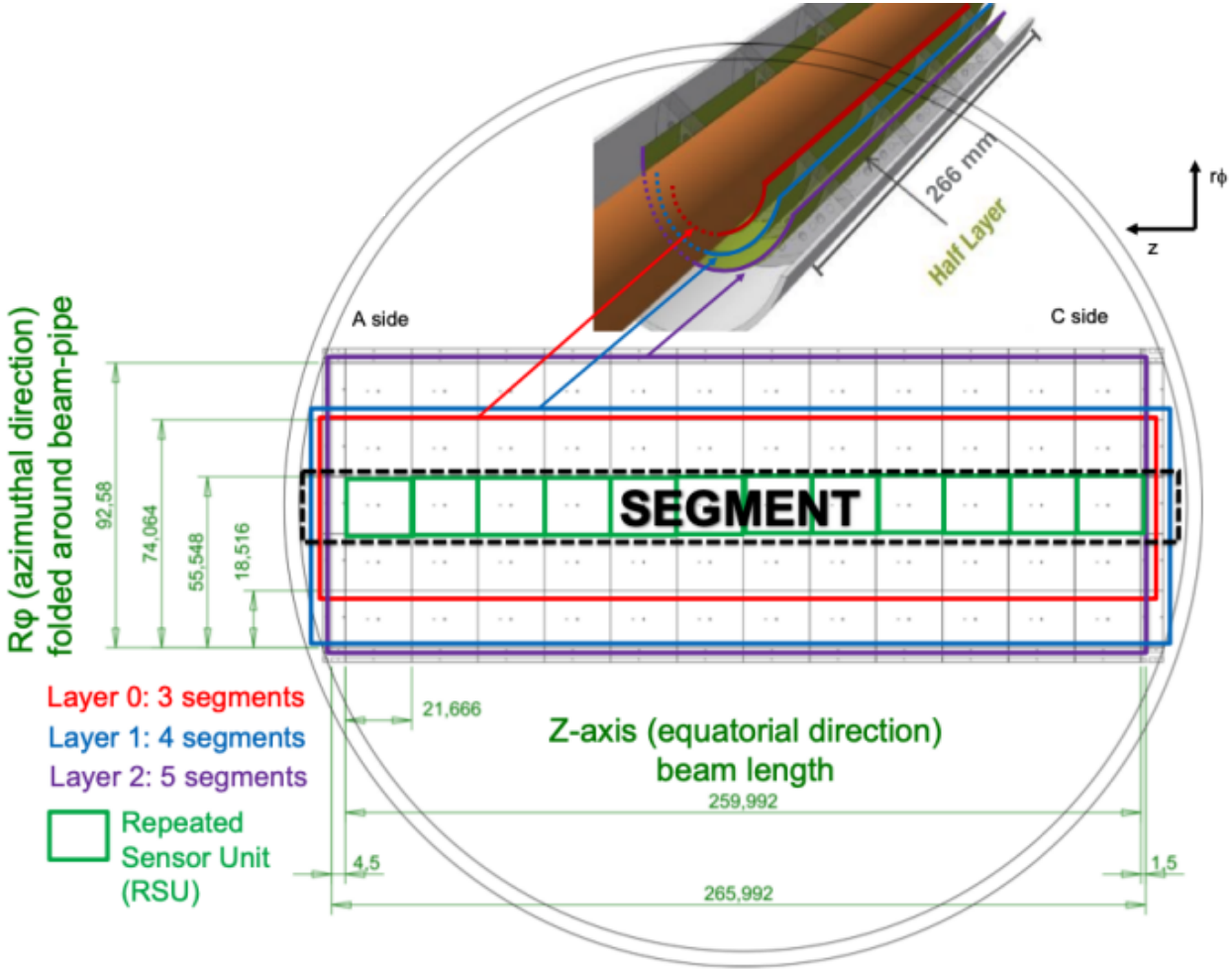




MOSAIX

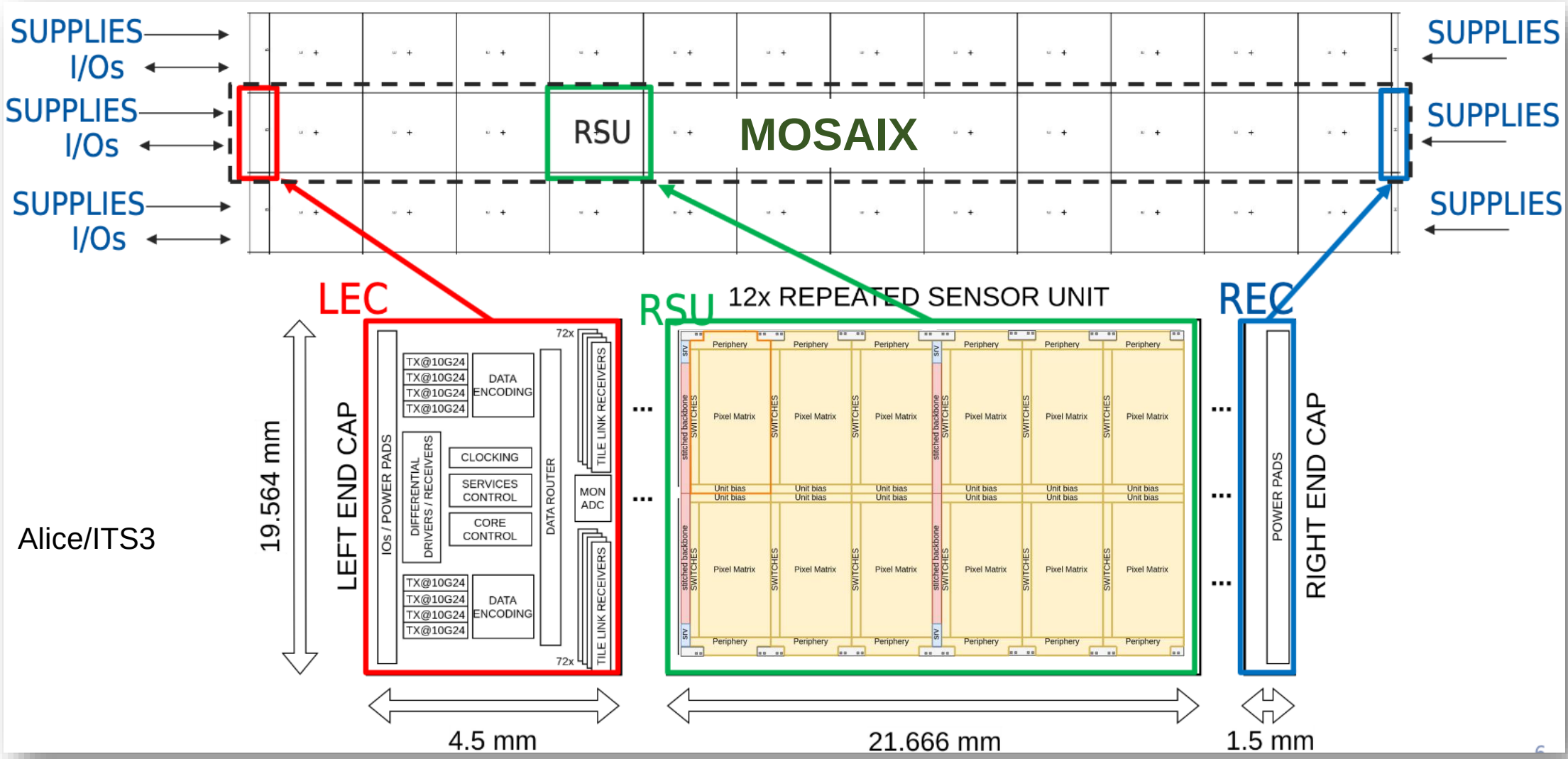
MOSAIX (ER2) - Sensor Dimensions

- MOSAIX is a full feature prototype of the sensor for ALICE ITS3
- Wafer scale sensor design using the stitching technique
- Process: TPSCo 65 nm CMOS Imaging Sensors(customized)



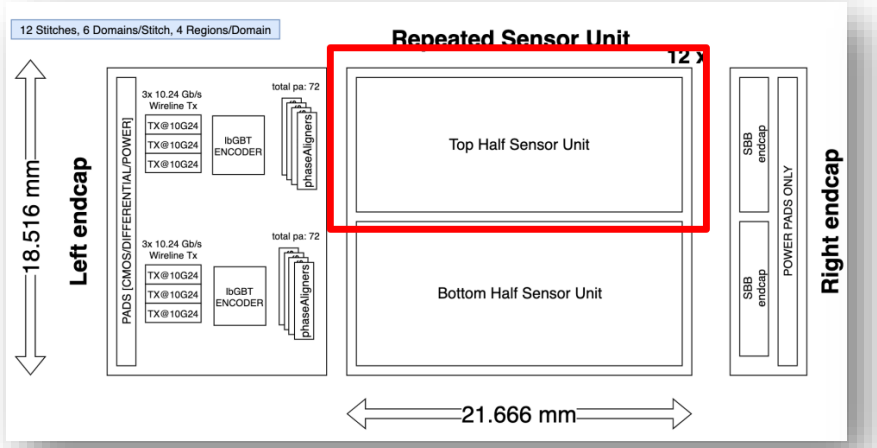
Alice/ITS3

MOSAIX (ER2) - Top Integration Diagram

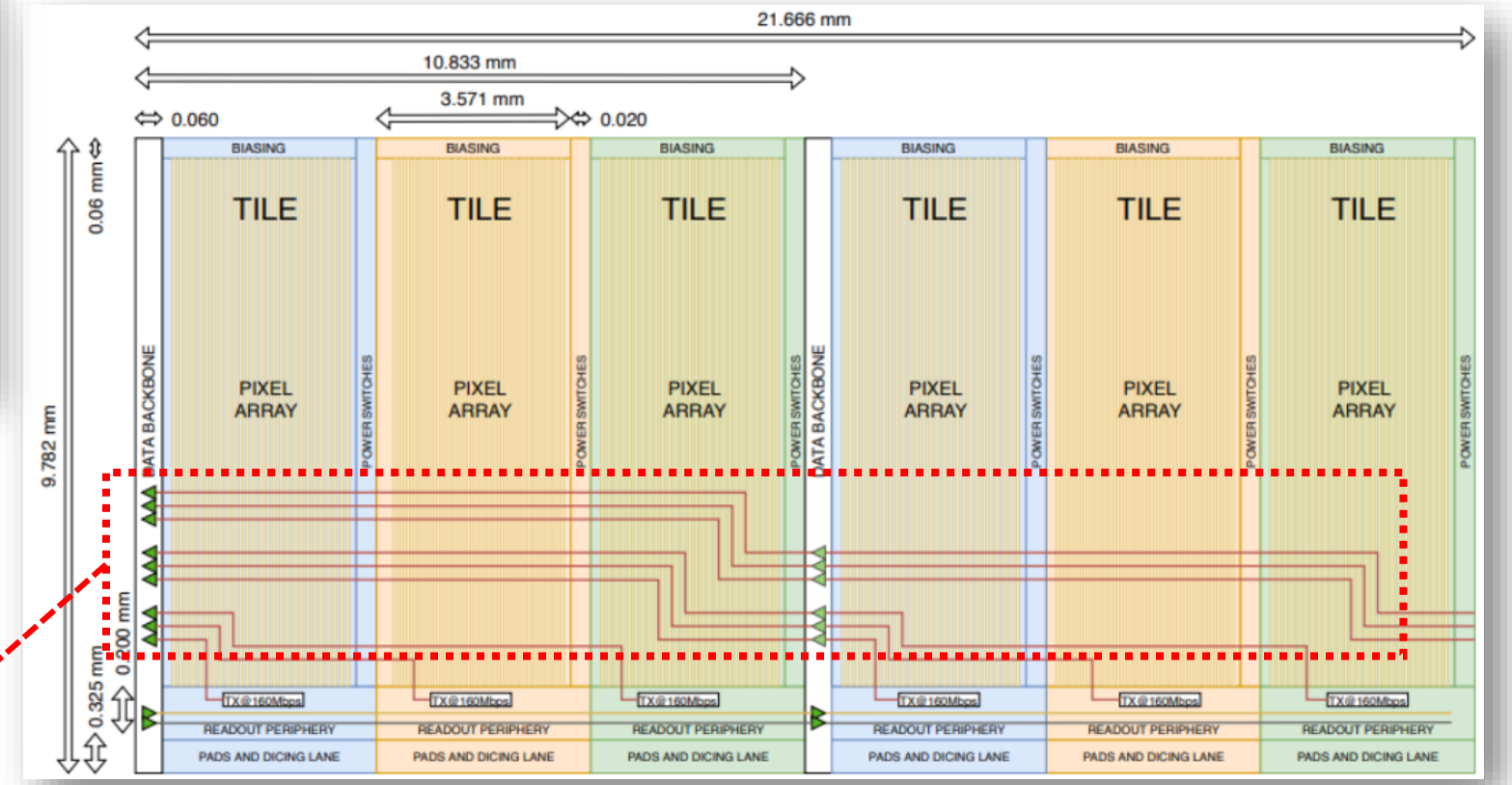


Alice/ITS3

ER2 Stitched Sensor (MOSAIX)



- **Fill factor ~93%**
- Depending on ER2 results, optional removal of test pads for final design would provide **~95.5%**

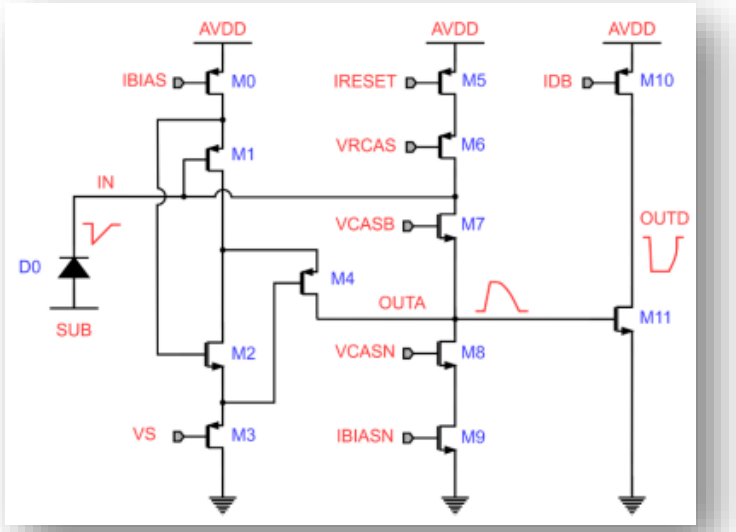


Alice/ITS3

- Redout Link @ 160Mb/s

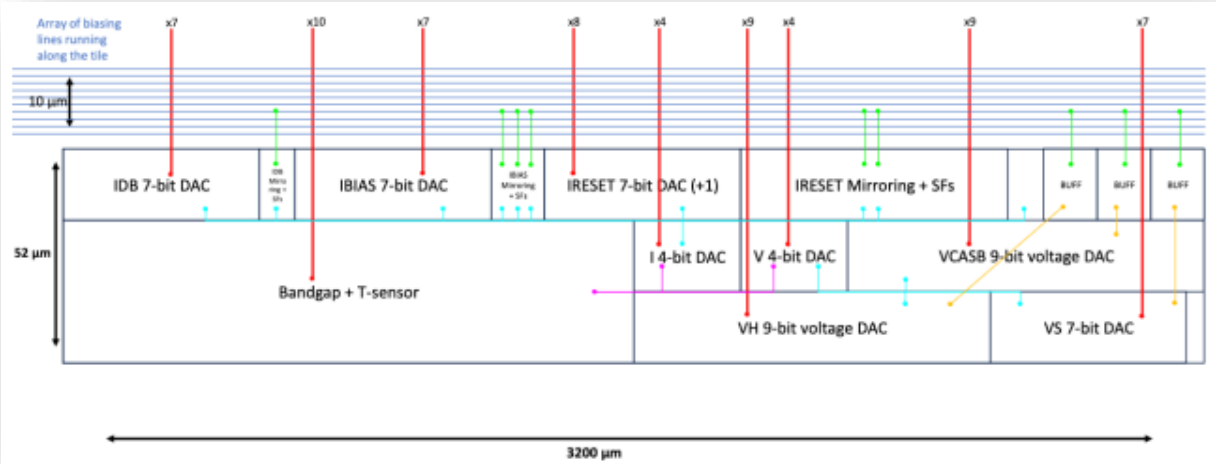
Front-End and Biasing

- **Evolution path**
  - DPTS -> MOSS -> MOSAIX
    - ✓ Improving transistor sizing and new layout



Alice/ITS3

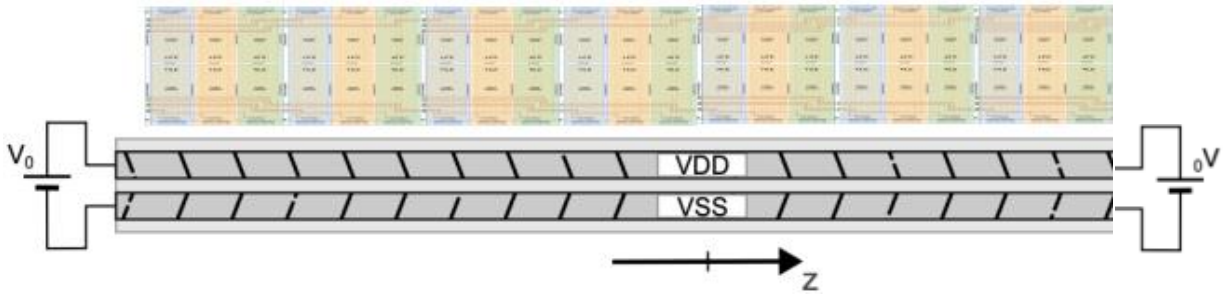
Unit Biasing (per Tile)



Specification	Value	Comment
Current consumption	$< 30\,\mathrm{nA}$	IBIAS + discriminator standby current
Dynamic energy (@ 600 e)	$\leq 10\,\mathrm{pJ}$	No hard spec. as negligible wrt total power
Nominal threshold	$\approx 150\,e$	¼ of MIP
Equivalent Noise Charge	$< 18\,e$	
Threshold mismatch	$< 18\,e$	
Gain (@ threshold)	$> 400\,\mu\mathrm{V}/e$	Simulated avoiding discriminator kick-back
Phase margin	$> 45°$	
Time of Arrival	$< 1\,\mu\mathrm{s}$	
Time over Threshold (@ 600 e)	$\ll 1\,\mathrm{ms}$	For lost hit probability $< 1\,\%$
Threshold sensitivity vs supply drop	$< 2\,e/\mathrm{mV}$	Supply drop on AVDD and AVSS
Detection efficiency	$> 99\,\%$	

Table 3.5: Analog front-end characteristics.

Power Domains, Currents and IR Drops



Supply purpose	Nets	Voltage [V]	Current [mA]	Pads on LEC	Pads on REC
Services	SDVDD-SDVSS	1.2 to 1.32	227	Yes	Yes
Global analog	GAVDD-GAVSS	1.2 to 1.32	540	Yes	Yes
Global digital	GDVDD-GDVSS	1.2 to 1.32	1369	Yes	Yes
Serializers	TXVDD-TXVSS	1.8	200	Yes	No
Substrate bias	PSUB	−1.2 to 0			

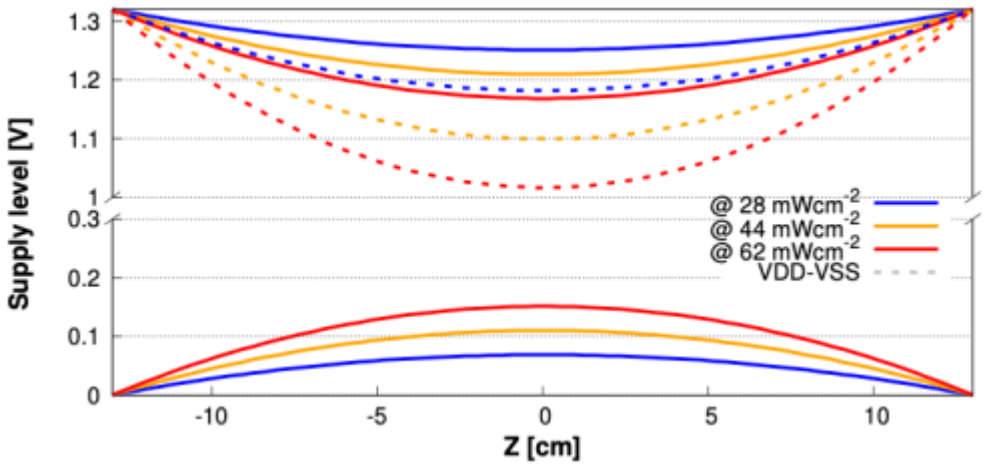
Alice/ITS3

❑On-chip LDOs?

- Increases complexity and power dissipation

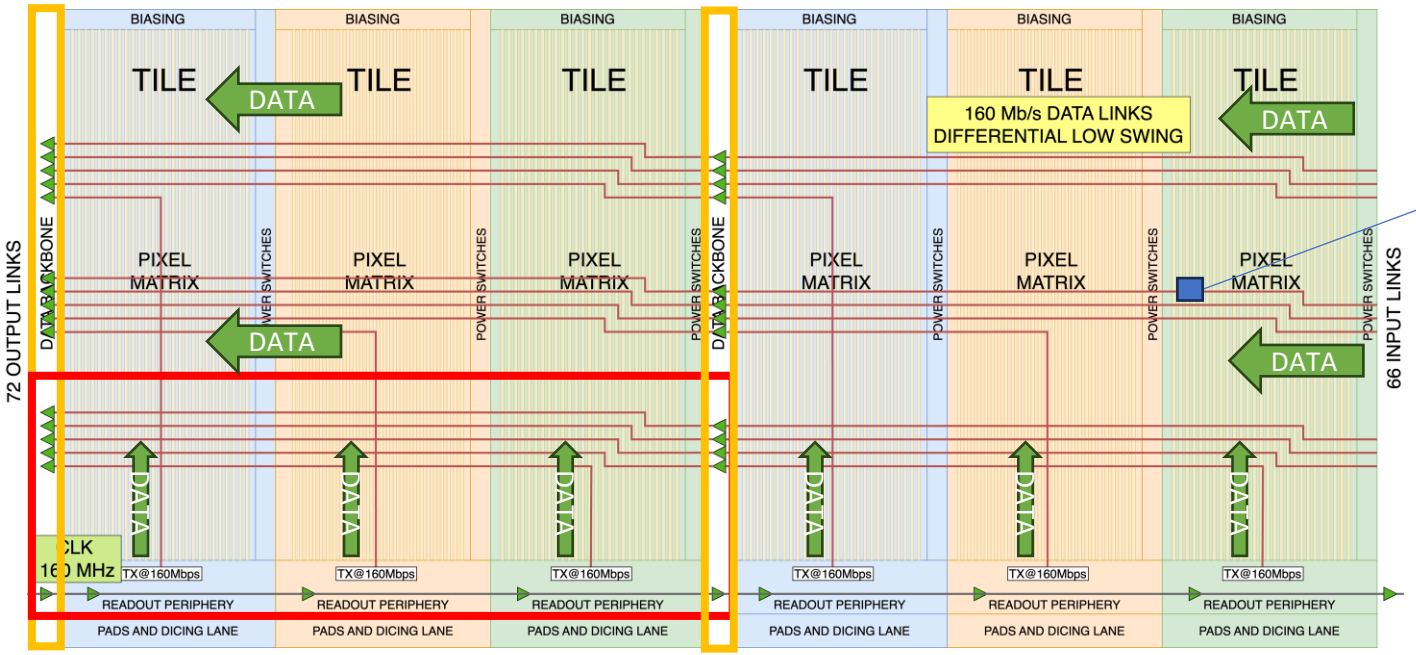
❑Estimates of IR drops

- Simple model, one global domain
- With the *new* metal stack (thick metal)

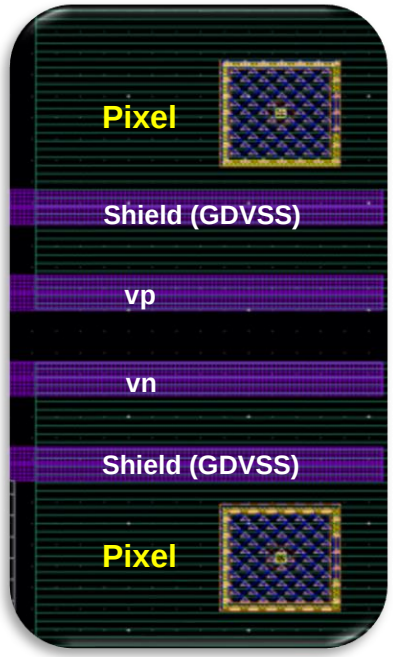


Data Readout / SBB

- Differential transmission scheme with low voltage swing
  - Power efficiency, immunity to supply noise, reduction of noise injection into sensing analog nodes



Alice/ITS3



- Distribute 160 MHz clock from LEC to TILES
- Long range (25 cm) on-chip 160 Mb/s point to point serial data links, clock synchronous

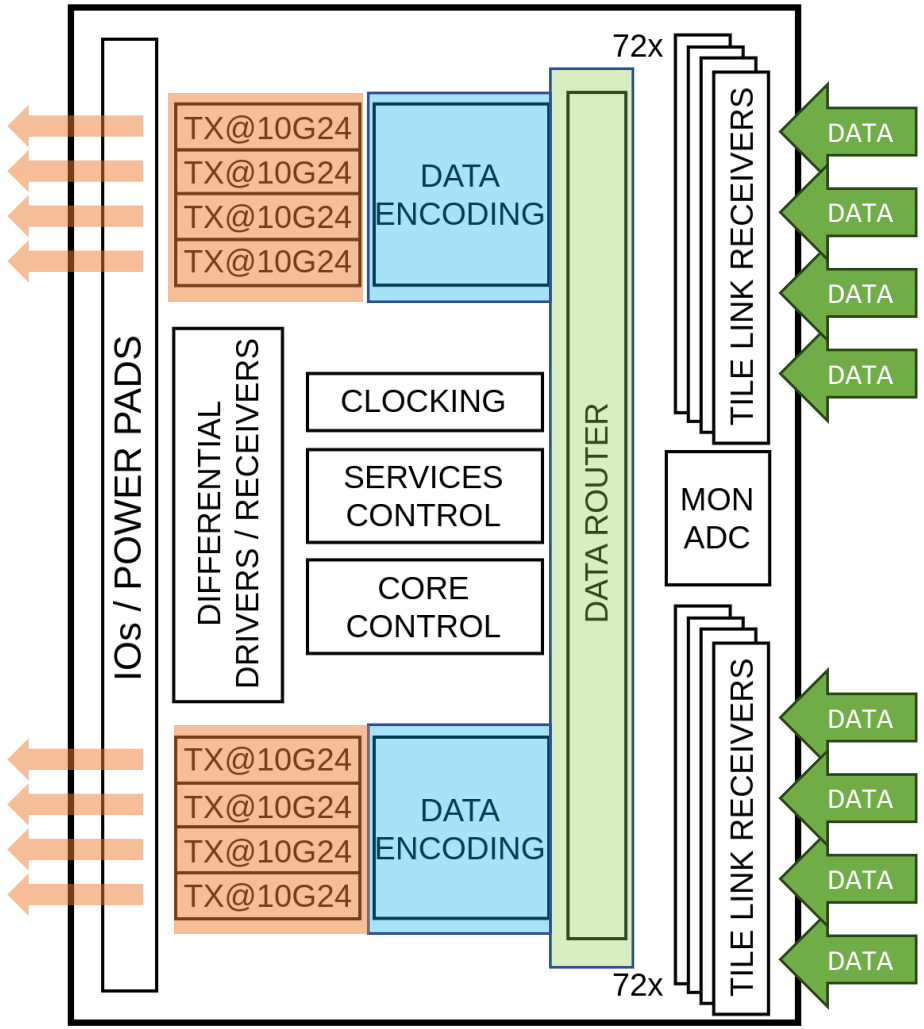
  From 144 tile peripheries to the data aggregation in the Left End Cap

LEC (Left End Cap) Architecture

- Interfaces and peripheral data hub
  - Input capacity 144×160 Mb/s = 23 Gb/s
  - No data processing in LEC
  - Data Router allows to reroute data from the 144 Tile Links to different serializers
- 8 High Speed Serializers
  - Redundancy to mitigate the risk of failures of off-chip optical link components
  - Two operating modes (digitally controlled)
    - **10.24 Gb/s** line rate: 3 serializers are used
    - **5.12 Gb/s** line rate: 6 serializers are used
    - Unused serializers can be switched off

MOSAIX shall drive directly electro-optical transceivers (VTRX+)

- Data Encoding logic ported from the lpGBT chip



Alice/ITS3 (Gianluca's slides)

MOSAIX Status

REC Design Status

L0	L1	L2	Type	Status 8 October	Status 1 Novembre	Next milestone (30 November)
REC				Correcting DRC violations		SIGN OFF
	Stitched Backbone REC		MIXED-SIGNAL	DONE	DONE	
	Pad Ring		ANALOG	DONE	DONE	
	Clock monitoring outputs		MIXED-SIGNAL	DONE	DONE	

Alice/ITS3 (Gianluca's slides)

RSU Design Status

L0	L1	L2	Type	Status 8 October	Status 1 Novembre	Next milestone (30 November)
RSU						
	Pixel Matrix		DIGITAL	CHECKING	CHECKING	FULL MATRIX SUBMISSION CANDIDATE
		Digital Pixel	DIGITAL	DONE	DONE	
		Digital Column Basic	DIGITAL	DONE	DONE	
		Digital Column Decoder	DIGITAL	DONE	DONE	
		Analog Pixel Baseline	ANALOG	DONE	DONE	
		Analog Pixel Variants	ANALOG	DONE	DONE	
	Biasing Unit DACs, Mon, Temp		ANALOG	DONE	DONE	
	Power Switches		ANALOG	DONE	DONE	
	Stitched Backbone RSU Block		ANALOG	SIGNOFF SIMS	DONE	
	Service Node		DIGITAL	POWER ANALYSIS	REDUCING POWER	
	Periphery		DIGITAL	TIMING CLOSURE	REDUCING POWER. TIMING SIGNOFF. BUG FIXES	
		SBB Tile (Pico Island)	MIXED-SIGNAL	DONE	DONE	
		Readout and Control	DIGITAL	DONE	REDUCING POWER	
	RSU Floorplan and Powerplan		DIGITAL	DONE	DONE	
	RSU Integration		DIGITAL	Routed, LVS OK. DRC fixes ongoing.	FULL FLOW. LVS OK. DRC and DFM fixes ongoing	FULL RSU SUBMISSION CANDIDATE

Alice/ITS3 (Gianluca's slides)

LEC

L0	L1	L2	Type	Status 8 October	Status 1 Novembre	Next milestone (30 November)
LEC						Complete design and implementation
	Stitched Backbone LEC		MIXED-SIGNAL	Integration waiting LEC floorplan	Integration waiting LEC floorplan	Integrated in LEC and validated
	Monitoring ADC		ANALOG	REVISITING COMPARATOR		SIGN OFF
		Analog Blocks Schematic	ANALOG	Revisiting comparator	DONE	
		Analog Blocks Layout	ANALOG	Revisit comparator	COMPLETING	
		Digital core	DIGITAL	DOING	COMPLETING	
		Top integration	ANALOG	Decoupling and filters added. Routing finished.	COMPLETING	
	Serializer GWT-PSI		MIXED-SIGNAL			Complete design and implementation
		Analog Blocks	ANALOG	Layout done. Setting-up signoff simulations		Timing signed-off
		Regulators	ANALOG	Revisited stability. DONE		Signed-off
		Digital Blocks	DIGITAL	Revisiting. Fixing timing.		Complete block level design
		Top Integration	MIXED-SIGNAL	Flow in-place		Full and clean implementation
	LEC Core		DIGITAL	Design and PnR ongoing	Design and PnR ongoing	Complete design and implementation
		Resetting and clocking	DIGITAL	To revise	To revise	
		Data Router	DIGITAL	RTL done. Needs PnR	RTL done. Needs PnR	
		High Speed Channel	DIGITAL	Revisiting, re-designing	DONE	
		Data Encoder	DIGITAL	RTL done. Needs PnR	DONE	
		GWT-PSI controller	DIGITAL	RTL done. Needs PnR	RTL done. Needs PnR	
		Slow Control	DIGITAL	RTL done. Needs PnR	RTL done. Needs PnR	
		Testability features	DIGITAL	Completing RTL entry	RTL done. Needs PnR	
	Differential Transceivers		MIXED-SIGNAL	DONE	DONE	SIGN OFF
	Pad Ring		ANALOG	DONE	DONE	SIGN OFF
	LEC Floorplan and Powerplan		DIGITAL	DOING	DOING	Complete design and implementation
	LEC Integration		DIGITAL	DOING	DOING	Complete design and implementation

Alice/ITS3
(Gianluca's slides)

MOSAIX: Work ahead

Tape-out date!?

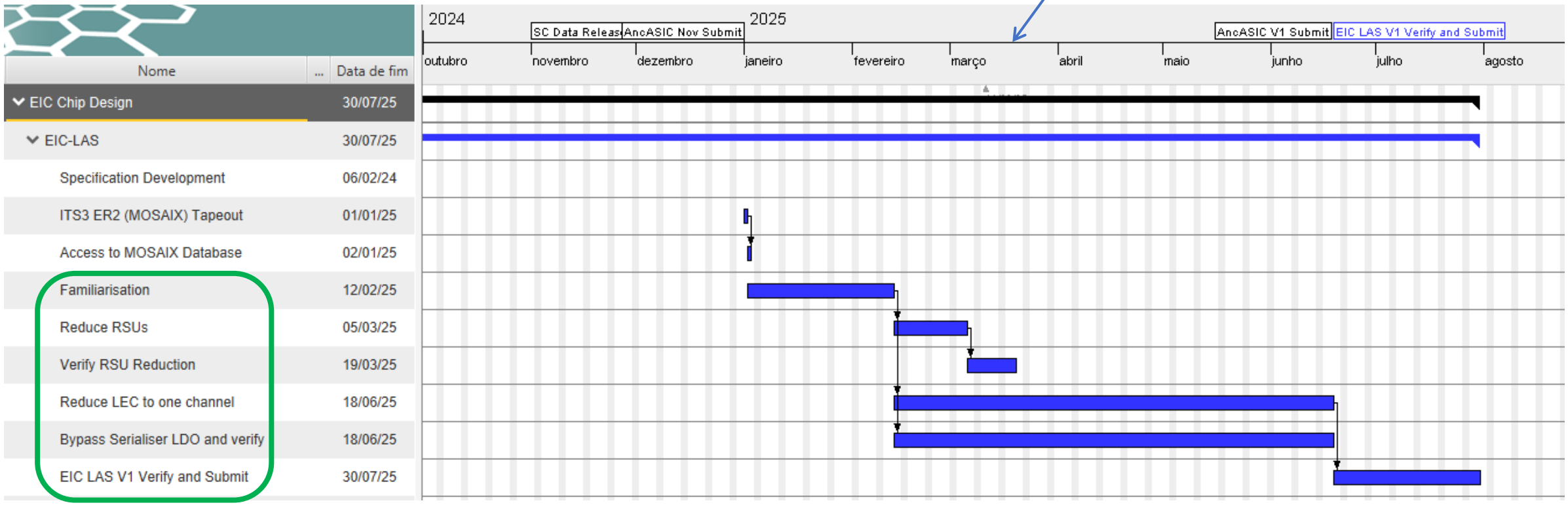
- DOING Completion of block level designs
  - Completion of the ADC imminent
  - Completion of the GWT-PSI Serializer, work needed
- DOING Completion of REC, RSU, LEC top designs
  - REC completed
  - RSU integration well advanced. Dependency on re-spin of components for bug fixes, power reduction, timing closure
  - LEC behind, work needed
- DOING Verification and validation phases of the integrated design
  - Execution of physical integrity and manufacturability checks (DRC, DFM) ongoing
  - Need of systematic block level power integrity analysis work needed
  - Functional verification by simulations work needed
- DOING Wafer scale integration ongoing

Alice/ITS3 (Gianluca's slides)

MOSAIX to EIC-LAS

Initial Plan

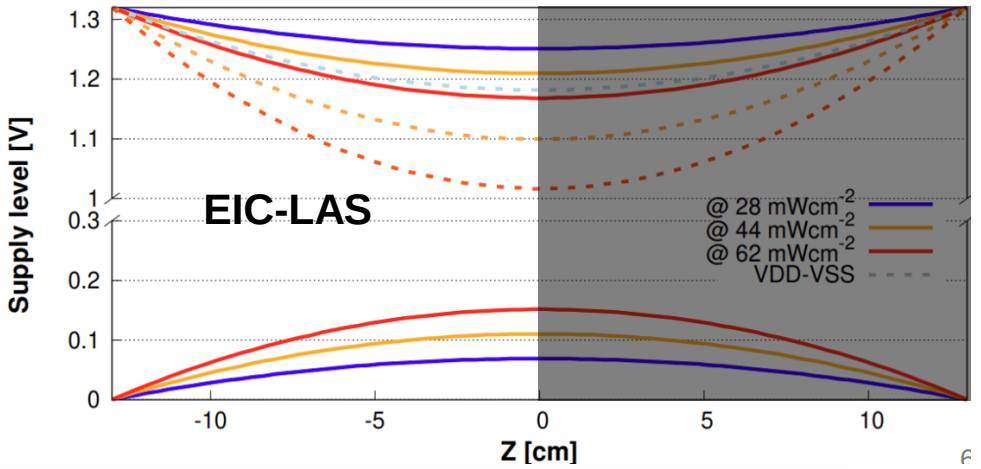
MOSAIX Tape-out (expected)



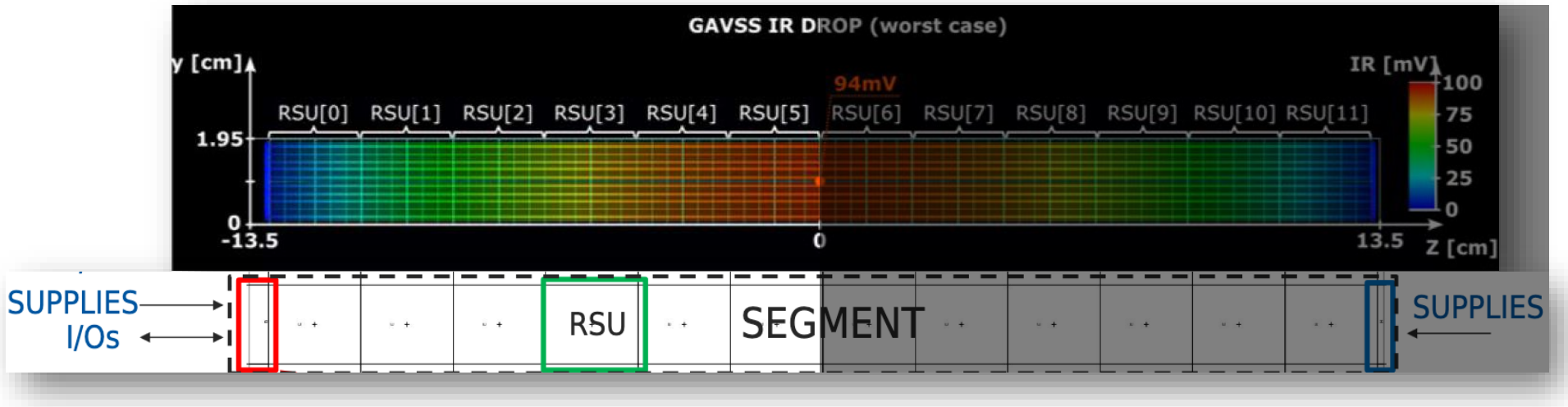
Main Tasks

EIC-LAS: Reducing from 12 to 5-6 RSUs

- EIC-LAS (SVT OB & Discs):
  - **Powering** applied **only** from the LEC.
  - Expected similar IR drop @RSU-5 ?

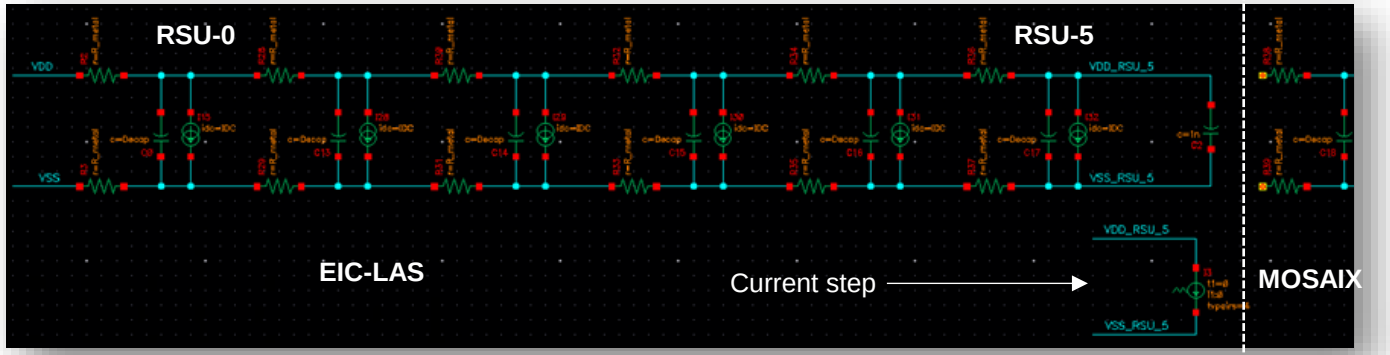


EIC-LAS



EIC-LAS vs MOSAIX: Same IR Drop?

Simple model including supply resistivity, constant DC current, and local decaps.

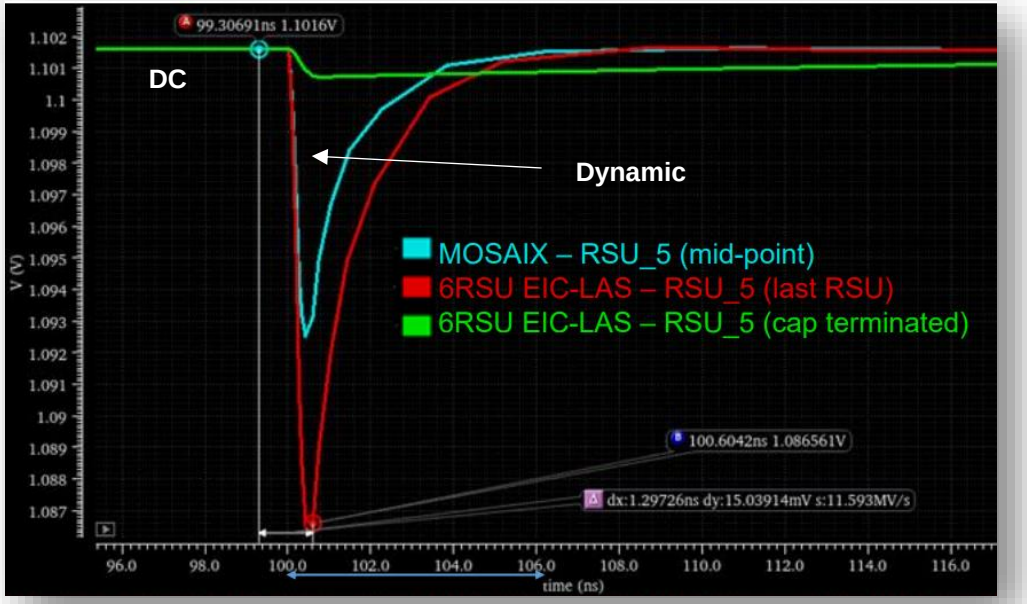


Clock propagation delay of about 2ns (in each RSU)

- Local supply drop/noise are expected to be worse in the case EIC-LAS (case of dynamic activity).

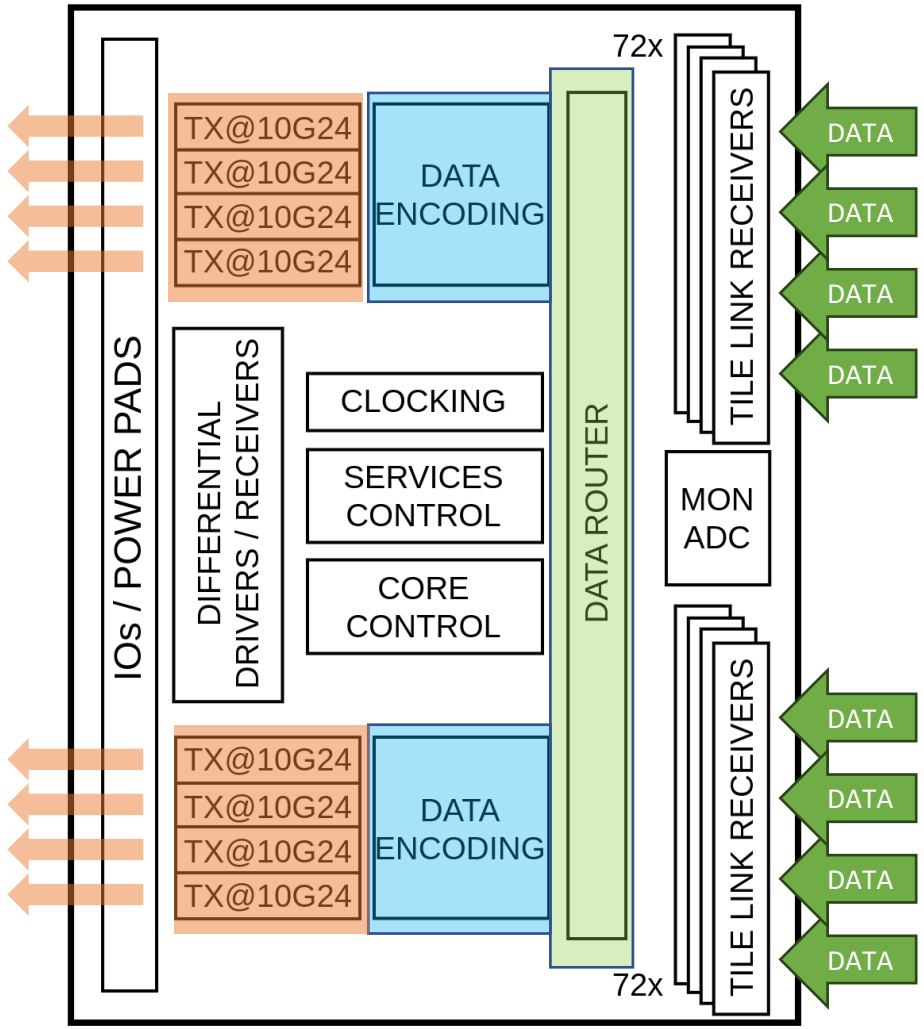
- Possible improvements:
  I. REC internal decaps (limited area and REC modification).
  II. REC external decaps.
  III. Also powered from the REC.

VDD-VSS Local drops @ RSU-5 after a current step



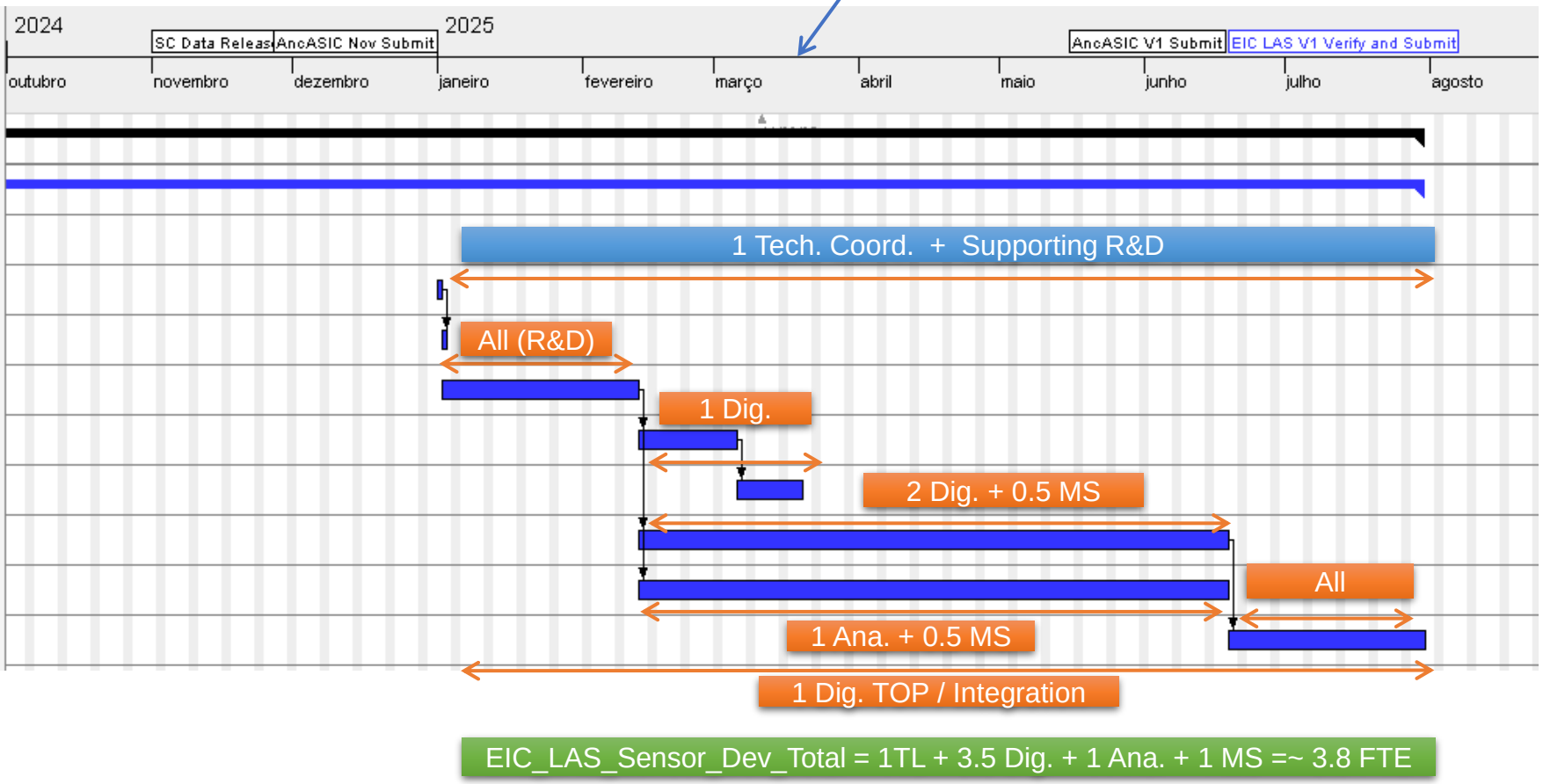
MOSAIX to EIC-LAS : LEC Modifications

- Reduce LEC to one channel
  - Bypass Serializer LDOs
    - Study on the performance before and after removing LDOs.
    - Dedicated decap cells, star routing (supply), and functional adjustments (no LDO controls).
  - Data **Encoding** and **Router** (serialization of the data to a single channel)
    - Challenge to adapt/change
    - SC control needs to be modified



Preliminary Resources

Nome	...	Data de fim
EIC Chip Design		30/07/25
EIC-LAS		30/07/25
Specification Development		06/02/24
ITS3 ER2 (MOSAIX) Tapeout		01/01/25
Access to MOSAIX Database		02/01/25
Familiarisation		12/02/25
Reduce RSUs		05/03/25
Verify RSU Reduction		19/03/25
Reduce LEC to one channel		18/06/25
Bypass Serialiser LDO and verify		18/06/25
EIC LAS V1 Verify and Submit		30/07/25



Preliminary Resources and Tasks

- EIC-LAS Senor Development (~7 months)
  - 1 Technical Lead that also supports R&D / Design
  - 1 Digital engineer for Top / Integration
  - Reduce the number of RSUs
    - 1 Digital engineer (half period) to reduce RSUs and to validate the signal/data integrity (of each RSU).
  - Reduce LEC to one channel
    - 2 Digital engineers plus 0.5 mixed signal engineer. SC control needs to be modified as well as the serialization of the data to a single channel.
  - Bypass Serializer LDOs
    - 1 Analog engineer plus 0.5 mixed signal engineer. Study on the performance before and after removing LDOs. Dedicated decap cells, star routing (supply), and functional adjustments (no LDO controls).
  - Final checks and tap-out
    - All team. Functionality, filling, final DRC checks, and submission.

MOSAIX to EIC-LAS

Further Modifications?

Timing Improvement!?

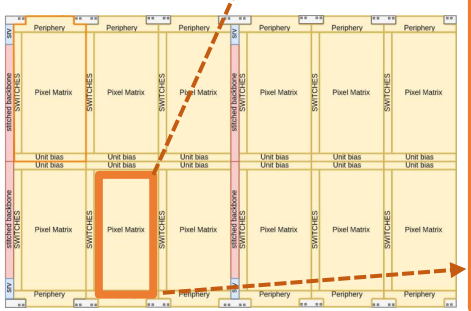
MOSAIX to EIC-LAS: Timing Improvement

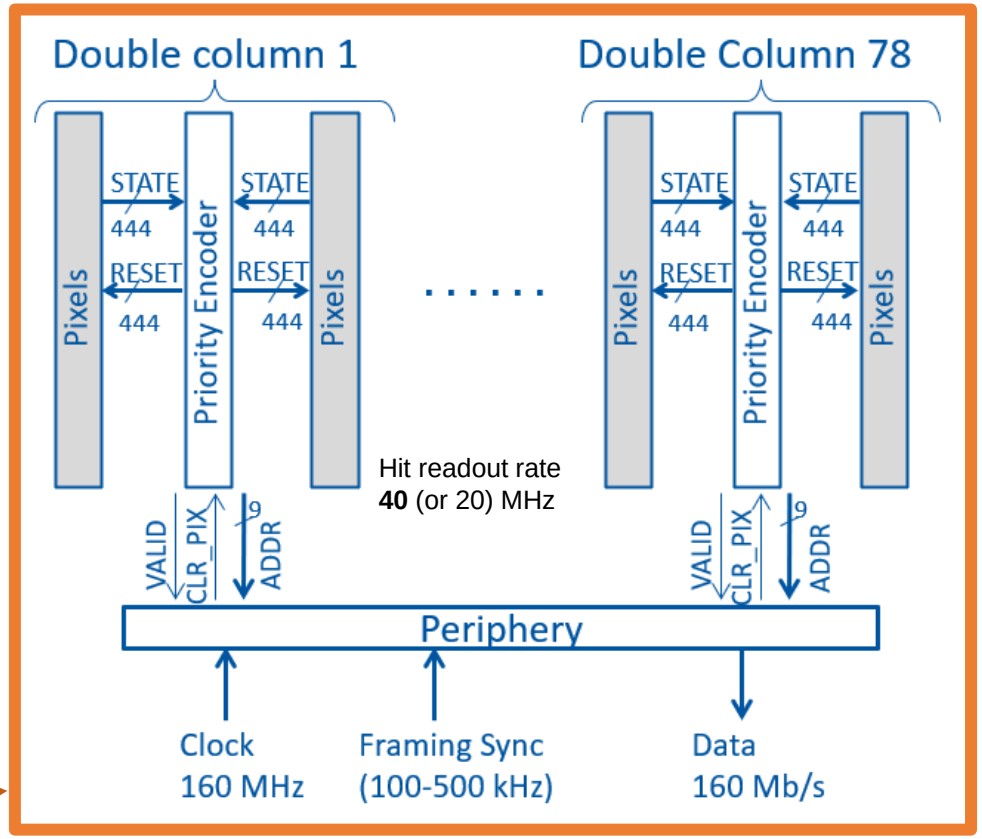
❑Pixel Array Readout

- ➢ Serial transmission of tile packet to LEC
  - ➢ Tile periphery builds and transmits one data packet for each framing interval (2-10 μs)
  - ➢ Global SYNC signal aligns in time the integration intervals across all the tiles

@ 40MHz (25ns) for a 2μs interval, capable of **80 hits** per Tile

For **EIC-LAS**, less hits per Tile?

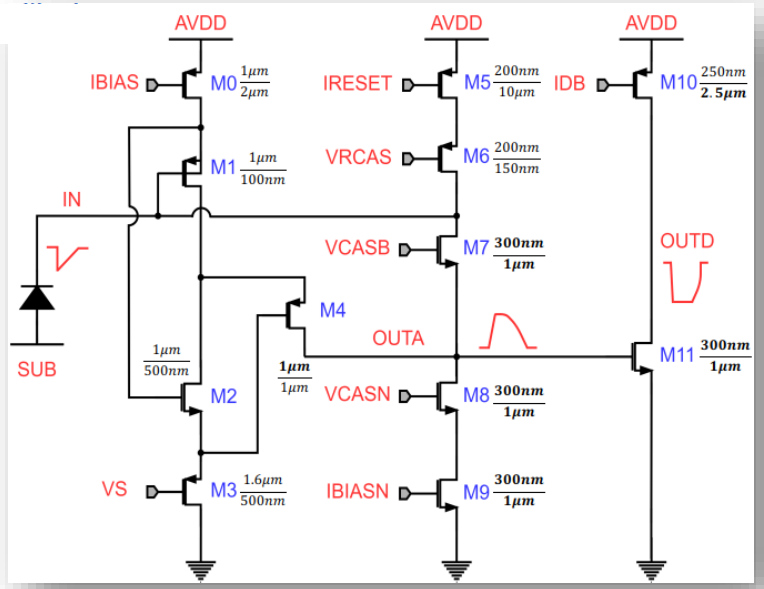




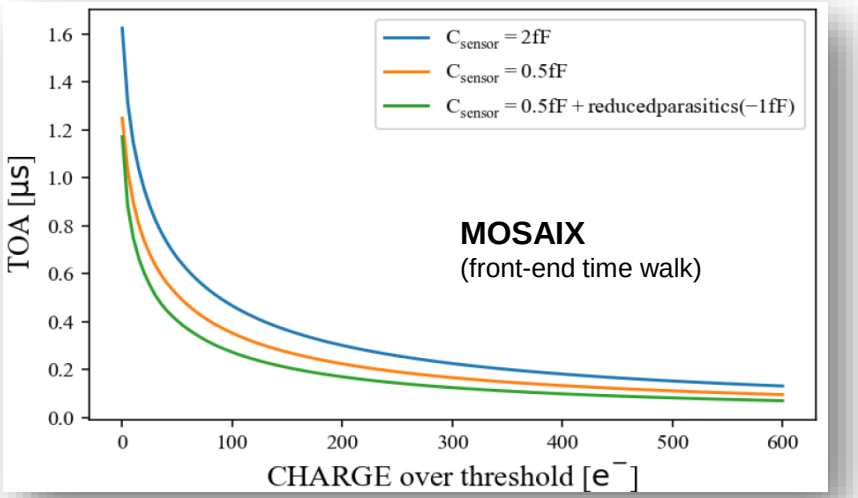
Alice/ITS3

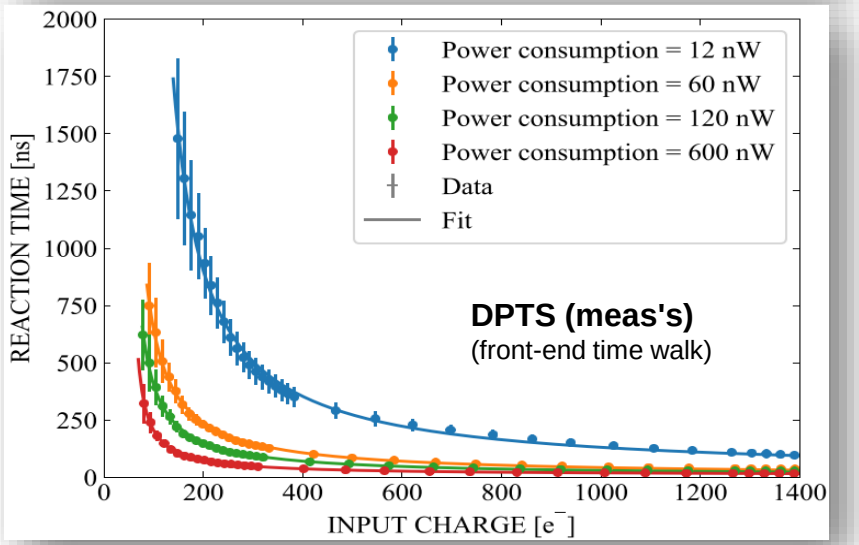
MOSAIX to EIC-LAS: Timing Improvement

- Front-end Improvements
  - Decreasing sensor's capacitance
  - Increasing the power consumption (adjusting the BIAS)



Alice/ITS3
(Walter's slides)





Thanks!