Electronics developments for the μRWELL Endcap Tracker: Frontend and Readout Emulation Platform

Roberto Ammendola

INFN Roma Tor Vergata

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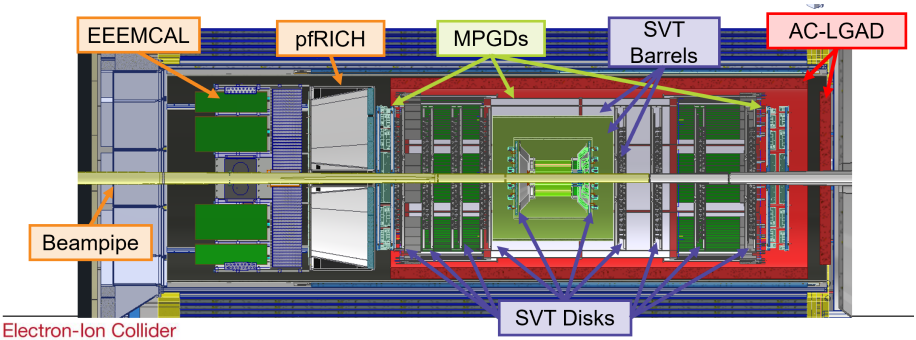
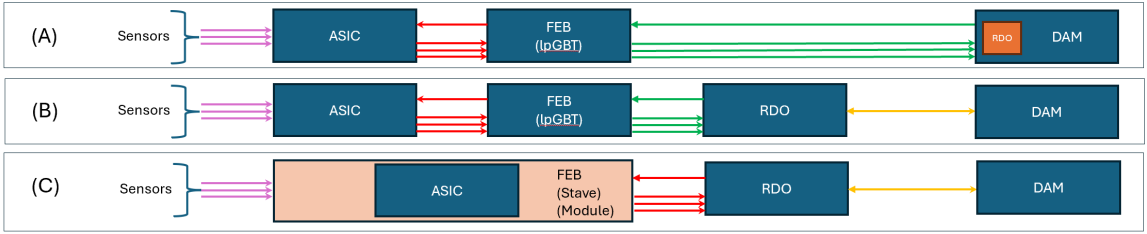
Introduction to Endcap Tracker electronics development

- At Roma Tor Vergata we are developing Endcap Tracker detector.
- It consists of two pairs of disks placed at the sides of the inner barrel.
- Front End ASIC and board design will be in common with the other MPGDs.
- Front End board will require specific form factor in order to adapt to space constraint.
- More details on detector and geometry in Annalisa and Stefano talks later on.

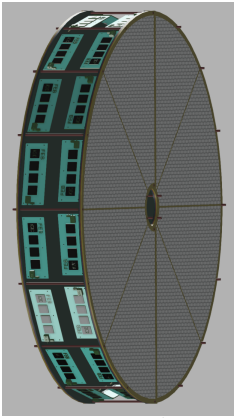


Readout Scheme



- lpGBT and VTRX+ will be the protocol and media used to transmit data
- discussion on-going wether use RDO boards or not

EndCap Tracker Figures



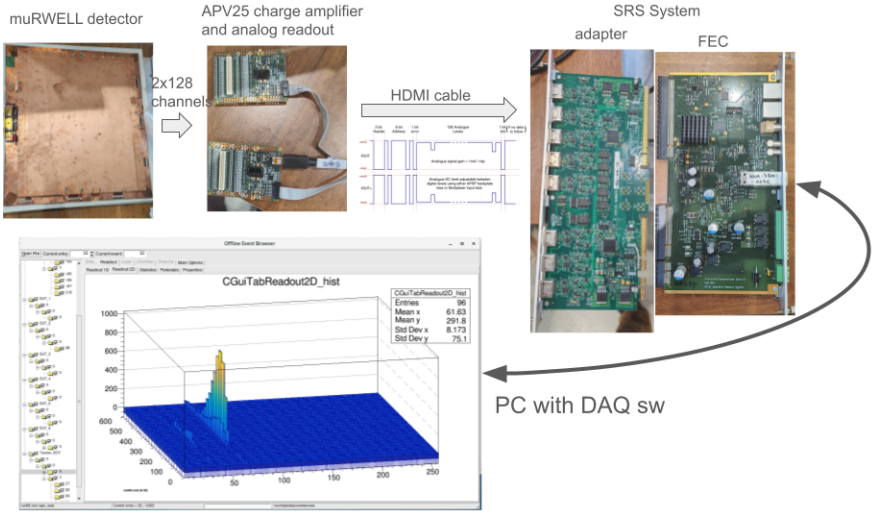
constants	
number of urwell strips per quadrant per dimension	768
number of channels per SALSA ASIC	64
number of SALSA ASICs per FEB	4
number of quadrants per disk	4
number of disks	4
number of FEBs per RDO	6
number of RDOs per DAM	48

scheme with RDOs	per quadrant	per disk	ECT total
number of SALSA ASICs	24	96	384
number of FEBs	6	24	96
number of RDOs	1	4	16
number of DAMs			1
scheme without RDOs			
number of DAMs			2

data bandwidth (Mbit/s) outputs with estimated hitrate 10kHz	per ASIC	per FEB	per RDO	ECT total
calibration	6	24	144	2304
peak finding (nominal mode)	40	160	960	15360
signal shape (on demand mode)	265	1060	6360	101760

Actual Experimental Setup

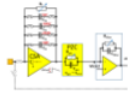
Current setup used for testbeam is based on APV25 technology and is working up to 256 channels.

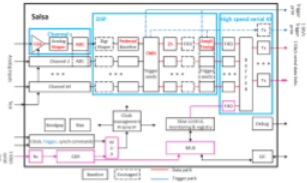


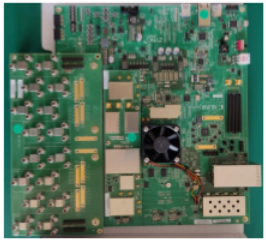
FrontEnd and Readout chain Emulation

- SALSA chip could be available in 2027 for first integration in Front-End boards
- Interfacing with detector could happen even later
- Saclay group has already though to emulate (part of) SALSA logic on low-cost FPGAs, to perform design verification
- At Roma Tor Vergata we can prepare a testbed to extend this activity in order to connect the detector to a multi-channel, high sampling rate integrated ADCs FPGAs (ZCU216 board)
- there is some glue logic needed (charge amplifier) we can think to develop in very short time eventually in a simplified version
- having a single box with 16 channels readout complete with charge amplifier, ADC, SALSA ASIC logic and instrumented readout through the on-chip Processing System can be a good solution to both test the detector in development and test the SALSA ASIC features directly on real detector data.
- by adding a VLDB+ board (available from CERN in 3 months) to exercise lpGBT + VTRX+ functionality
- complete Readout chain can be exercised with a FLX-182

Platform for complete readout chain







Custom CSA

ZCU216 with internal 2.5GSPS ADCs

VLDB+ (lpGBT+VTRX+)

RDO? (sfp+ + AXAU15)

DAM (FLX-182)

Summary of next activities

- complete readout chain to be assembled in several steps
- custom CSA should be designed to mimic SALSA performances
- filtering and signal shaping to be performed using high sampling rate ADCs
- other SALSA logic can be ported into the platform
- VLDB+ kit can be ordered to add lpGBT and VTRX+ in the readout chain
- in case we decide to have RDO boards we can start using COTS such as ALINX AXAU15 with SFP+ connectors mezzanine
- we can profit of a FLX-182 board in collaboration with Roma1 group to start develop DAQ firmware