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Status of SALSA ASIC design

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EPIC Collaboration meeting

24/01/2025

SALSA specifications and architecture

Timeline foreseen for the project

Recent achievements and results

Current developments

Prospects

SALSA CHIP TARGET SPECIFICATIONS, COMPARED TO EPIC MPGD REQUIREMENTS

Versatile front-end characteristics → EPIC MPGD needs

- 64 channels
- Large input capacitance range, optimized for 50-200 pF, reasonable gain up to 1 nF → **200 pF**
- Large range of peaking times: 50-500 ns → **100-200 ns**
- Large choice of gain ranges: 0-50, 0-250, 0-500 fC or 0-5 pC → **0-250 fC**
- Large range of input rates, up to 100 kHz/ch with fast CSA reset → **< 25 kHz**
- Both polarities (depends on kind of detector) → **negative**

Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s → **50 MS/s**
- Integrated DSP for internal data processing and size reduction, configurable treatment processes → **all processes**
- Continuous readout, triggered readout → **continuous readout**
- Four 1 Gb/s output data links → **1 (or 2) gigabit link used at EPIC**

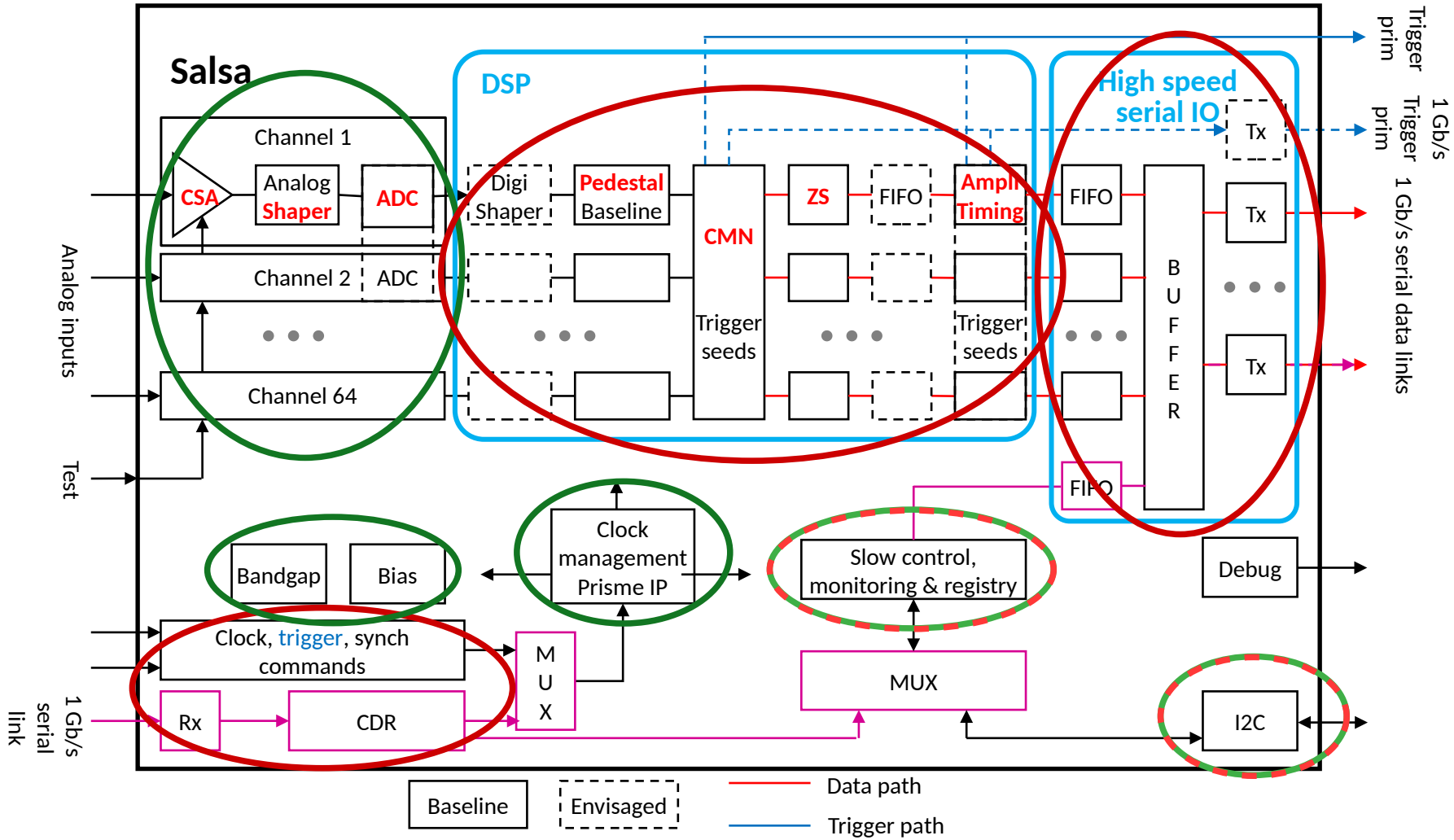
General characteristics

- ~1 cm^2 die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, > 300 Mrad, > 10^{13} n_{eq}/cm^2) → **10 krad, 10^{11} n_{eq}/cm^2**

SALSA CHIP PRELIMINARY ARCHITECTURE

Exists in prototype

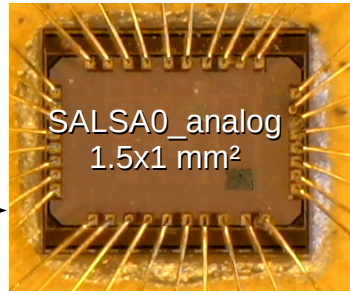
Development in progress

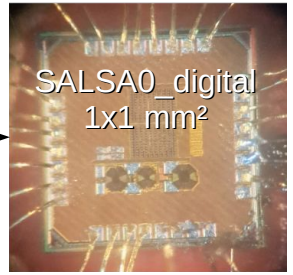


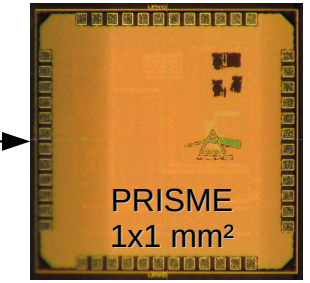
TIMELINE OF THE SALSA PROJECT

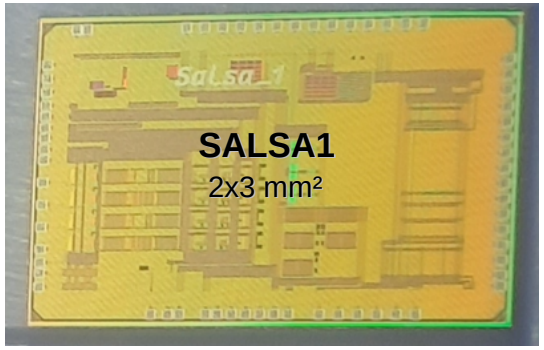
Steps of SALSA development

- 2020-22: Discussions and reflections on the project
- 2022-23: **SALSA0** prototypes to study first designs
  - **SALSA0_analog** featuring 4 front-end channels
  - **SALSA0_digital** featuring an ADC block
- 2023: **PRISME** prototype to test PLL block + first version of general services (blocks partly from CERN)
- 2023-24: **SALSA1** prototype to test full front-end + ADC chains
- 2023-25: **SALSA2** prototype to test ASIC including DSP (most of features), but with smaller number of channels (≤ 32)
- 2026-27: **SALSA3** as pre-serial prototype with 64 channels



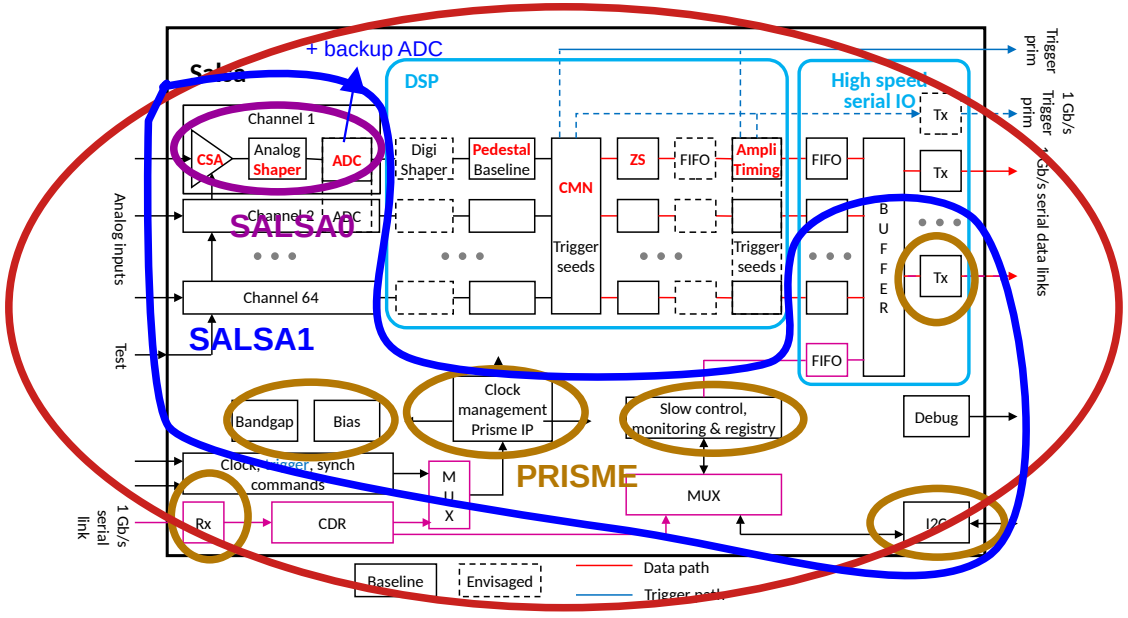






SALSA2 (mostly)

SALSA3



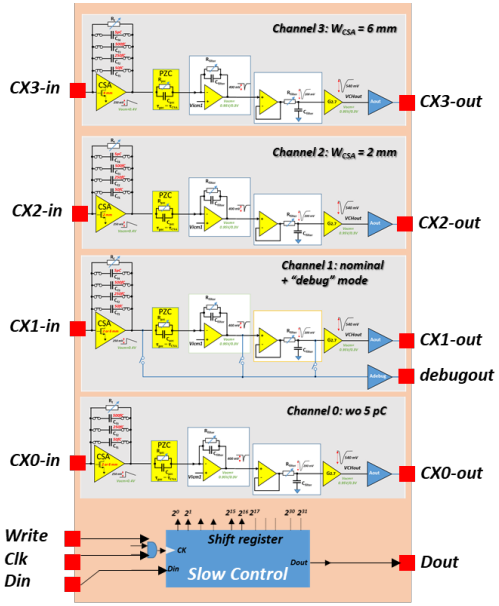
CURRENT STATUS: SALSA0

SALSA0 prototypes

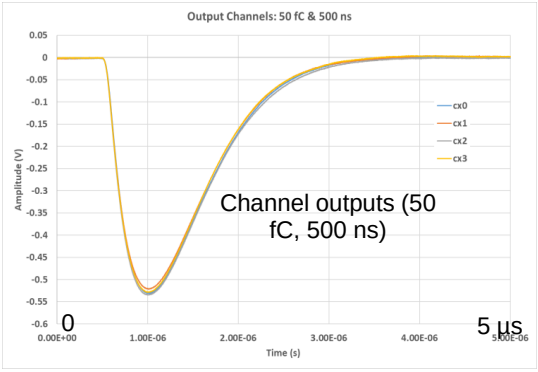
- Tested in 2023-2024
- Performance evaluation and bug fixes of frontend and ADC blocks

Frontend

- Measurements in agreement with simulations
- However some discrepancies concerning transfer functions and noise levels especially at 50 fC gain range, oscillations with specific configurations
- Origin found to be to parasitic resistances in the chip, corrected in the CSA design for SALSA1

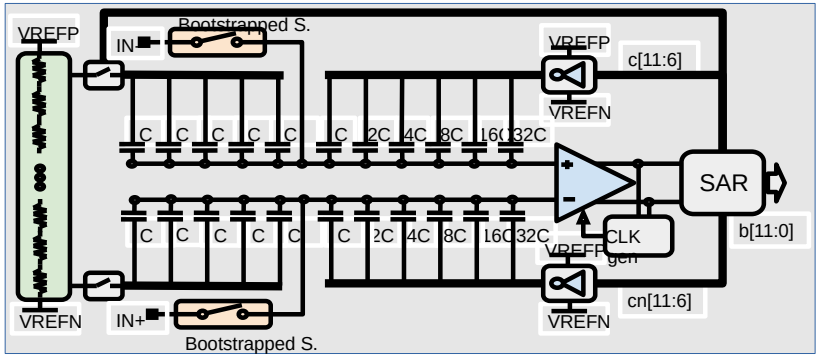


- Charge Sensitive Amplifier + Pole-Zero Cancellation + shaper
- 4 gain ranges: 0-50 fC, 0-250 fC, 0-500 fC and 0-5 pC
- 8 peaking times 50 to 500ns
- Integrated anti-saturation circuit
- Integrated test pulses



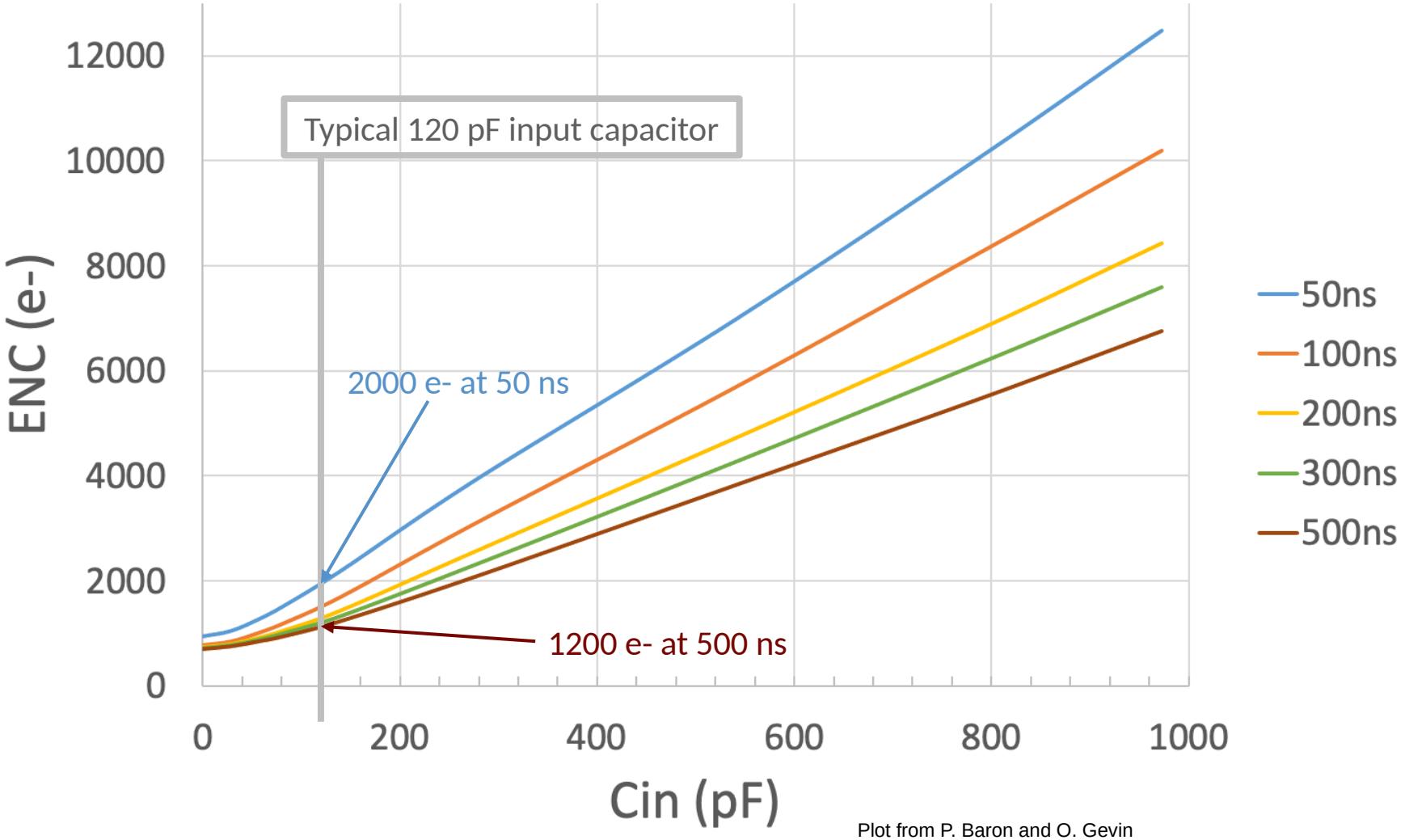
ADC block

- 12 bits 5-50 MS/s SAR ADC
- Expected 10-11 ENOB bits
- Debugging of ADC block



MAIN NOISE RESULTS ON SALSA0_ANALOG: TYPICAL CASE

Equivalent Noise Charge in the **250 fC range** at different peaking times



Plot from P. Baron and O. Gevin

CURRENT STATUS: PRISME

PRISME block

- PLL IP block in TSMC 65nm technology for clock generation, 4 clock outputs
- Large frequency ranges for input (40-120 MHz) and outputs (up to 1.6 GHz)
- Very low internal time jitter: ~3 ps RMS up to 1 GHz

PRISME prototype

- Tested from early 2024: PLL block, I2C, high speed I/O, bandgap, probes
- PLL ok with random jitter as low as 2.5 ps RMS, other blocks ok
- But large deterministic jitter, up to 50 ps RMS
- Origin of noise sources understood, fixed in PLL design

Radiation tests

- X-ray radiation tests at CERN in November 24
- Up to 300 Mrad reached, all blocks except PLL ok
- PLL working nominally up to 160 Mrad, reduced internal frequency above
- Cause of degradation understood, improved transistor sizes

Nest steps

- New PRISMEv1 prototype submitted in December 24
- Several modifications: deterministic jitter, radiation hardness, lower internal frequency, inclusion of CDR for unified input interface, compatibility with lpGBT input frequency
- To be tested before summer

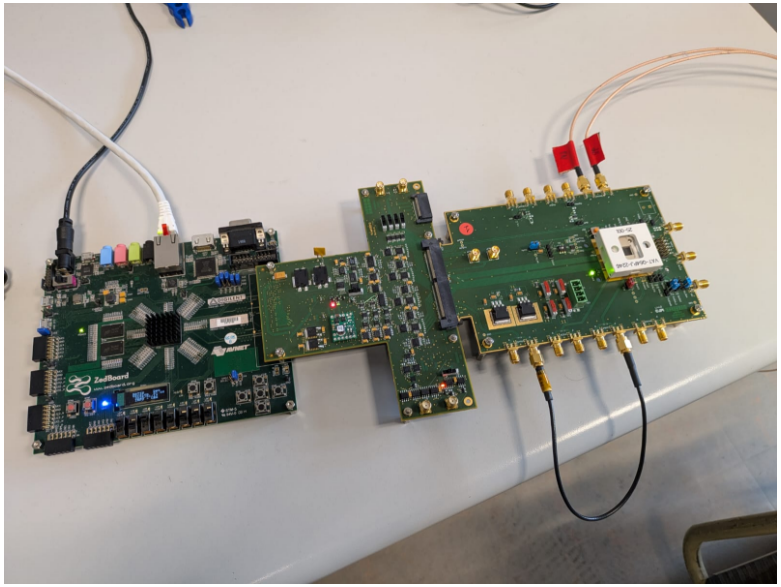
Technology	CMOS 65 nm
Power voltage	1.2V
Input reference frequency range	50, 80, 100, 320 MHz ±20%
VCO frequency	1.6-2 GHz
Number of output clocks	4
Output frequency	Programmable fractions of VCO frequency, up to 1 GHz
Phase shifter step	< 300 ps
Time interval jitter: analog path only	< 10 ps RMS up to 1 GHz with graceful degradation beyond
Time interval jitter: with digital paths	~3 ps RMS up to 1 GHz with graceful degradation beyond
Power consumption	< 9 mW, < 12 mW with digital regulation
Size	~0.1 mm²
Radiation mitigation	TMR, SEL free, TID up to 4 MGy

CURRENT STATUS: SALSA1

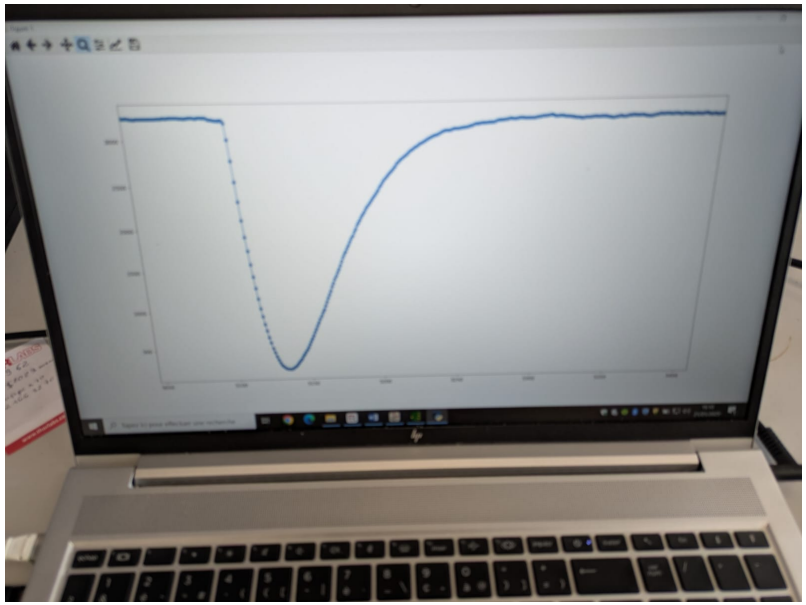
SALSA1 prototype

- 1st prototype with frontend + ADC chained, 4 channels + 2 ADC only
- Naked dies received beginning of October 24, packaged ones beginning of November
- Test cards delivered in December
- Tests started right before Christmas break, just very preliminary results so far
- Chip powered on without problem, nominal power current (78 mA)
- I2C interface working, slow-control registers responding correctly
- Frontend channels ok, no oscillation as observed with SALSA0 in specific cases
- Digital part including ADC delivering test data correctly

SALSA1 test setup



ADC output



CURRENT STATUS: SALSA2

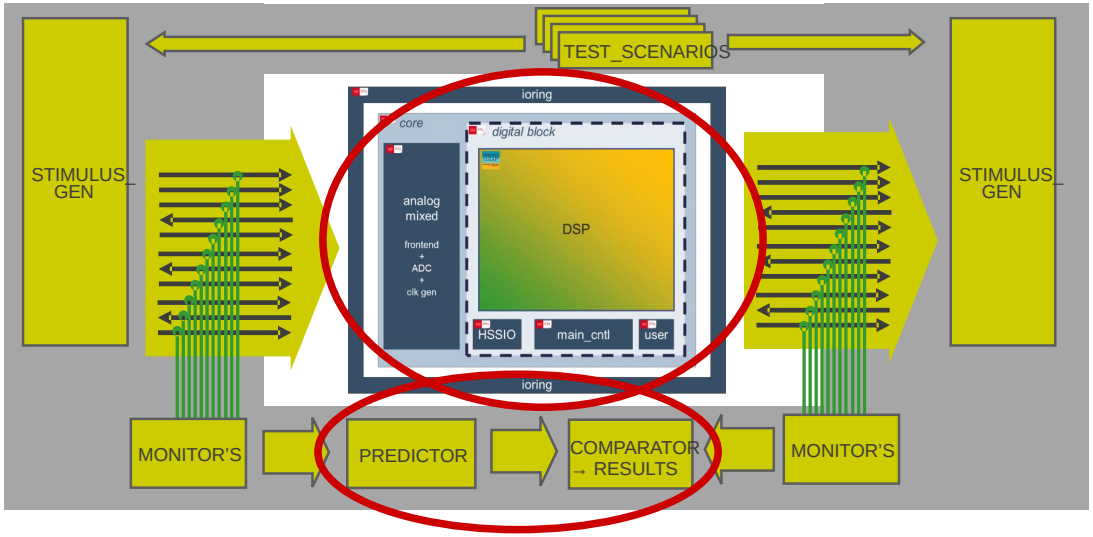
SALSA2 development status

- Main DSP modules and associated algorithms defined, study still ongoing for peak finding algo
- Work ongoing on HDL code of DSP modules, progresses on several modules: pedestal equalization, common mode correction, baseline following algorithm, zero suppression algorithm, packet building, data formatting, data serialization, serial input and output links
- New PLL version including CDR produced and integrated, to be checked with PRISMEv1
- UVM environment under definition for high level verifications
- Packaging under study, planed to be identical to the final SALSA one

Timeline

- Still a lot of works ahead:
  - code development of missing modules
  - code verification and validation
  - integration of all modules, validation
  - DSP layout generation and validation
  - assembly of all blocks
  - simulations of the whole chip
- Chip submission not expected before October 2025 (last MPW sub slot of the year)
- Tests in 2026
- Distribution to users before end 26

UVM environment



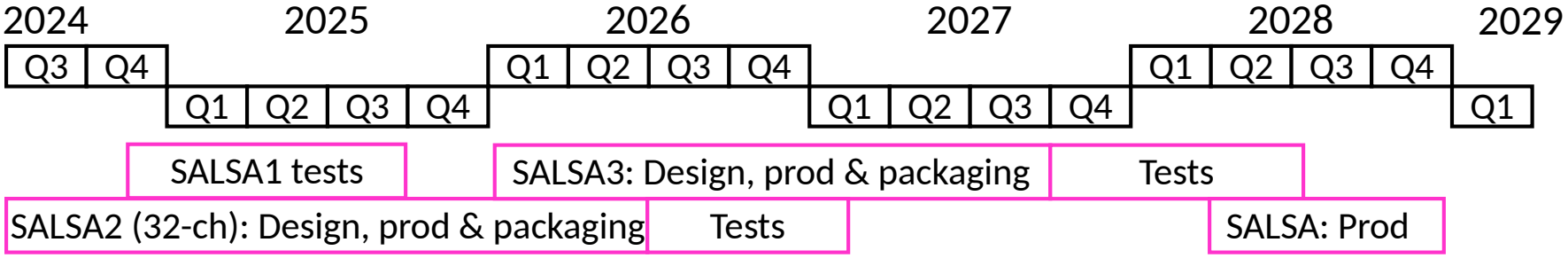
CONCLUSIONS AND PROSPECTS

Present status

- SALSA0 and PRISME prototypes with promising performance measurements
- SALSA1 prototype tests just started, ok so far
- SALSA2 prototype (with DSP, reduced number of channels) development ongoing; major part: digital architecture and data processing

Next steps

- Completion of tests on SALSA1 prototype
- Development of SALSA2, submission expected in October 2025
- Tests of SALSA2 in 2026
- Design of SALSA3 (pre-serial) to be started beginning of 2026: development of missing DSP features, 32 to 64 channels, bug corrections from SALSA2 tests
- Submission of SALSA3 end 2026 or beginning 2027, tests from 2027
- Full production in 2028, 5000 ASICs foreseen for EPIC, probably more produced for other projects



Spares

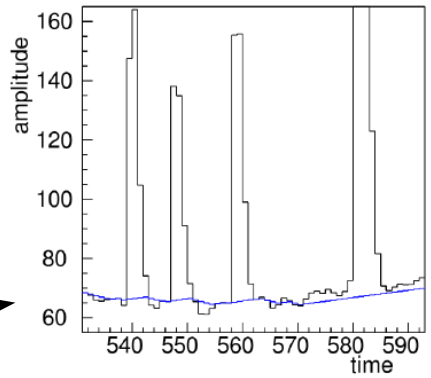
DSP DATA PROCESSING

General remarks

- Data processing, reduction and formatting from ADC values to output links
- Each process can be deactivated individually by user
- Process parameters through ASIC registers
- Part of codes from SAMPA chip
- Most of DSP features determined, details still under study

Baseline corrections

- Pedestal subtraction with fixed value per channel
- Common mode correction to reduce common noise impact, based on median value of samples of all channels for each sample time
- Baseline slope following algorithm



Plot from SAMPA doc

Digital shaping

- Cancellation of signal tail or peaking time correction with cascade of 4 first order IIR filters
- Algorithm from SAMPA, 2 x 4 parameters

$$y[n] = a_1 y[n-1] + b_0 x[n]$$

DSP DATA PROCESSING

Zero suppression

- Keep samples above fixed thresholds
- Tunable algorithm (add neighbor samples, drop too short set of samples, keep 1 sample over N, etc...)

Feature reconstruction

- To further reduce data flux by extracting reconstructed data → peak finding algorithm, with extraction of amplitude + time + width
- Peak finding and data extraction algorithms under study

External trigger management

- Samples kept when trigger signals received, configurable latency
- Associated or not with zero suppression, feature reconstruction, etc…

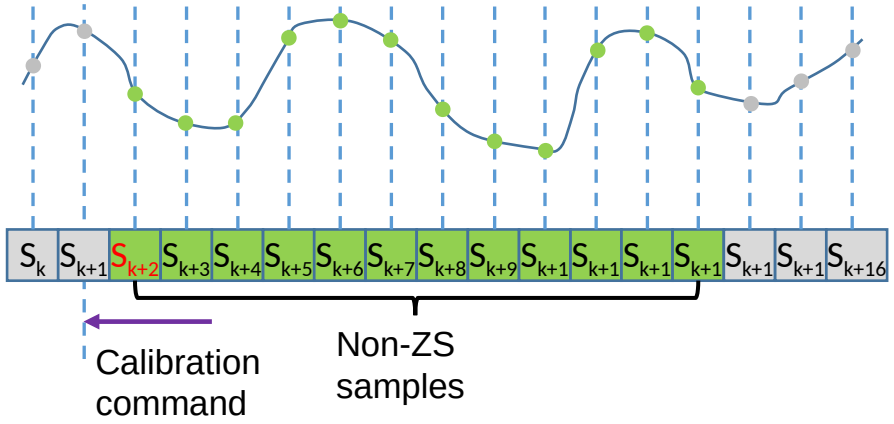
Trigger generation

- Trigger primitives generated when samples above threshold, with conditions on number of samples, multiplicity, etc...
- Latency reduction by placing trigger generation early in the processing chain
- Trigger primitives to be defined (logic signal, data on specific fast link, etc…)

DSP DATA PROCESSING

Calibration data

- Generated on demand with specific synchronous commands
- Calibration data of several types
  - non-ZS data
  - test pulses injected at front-end on one or several channels



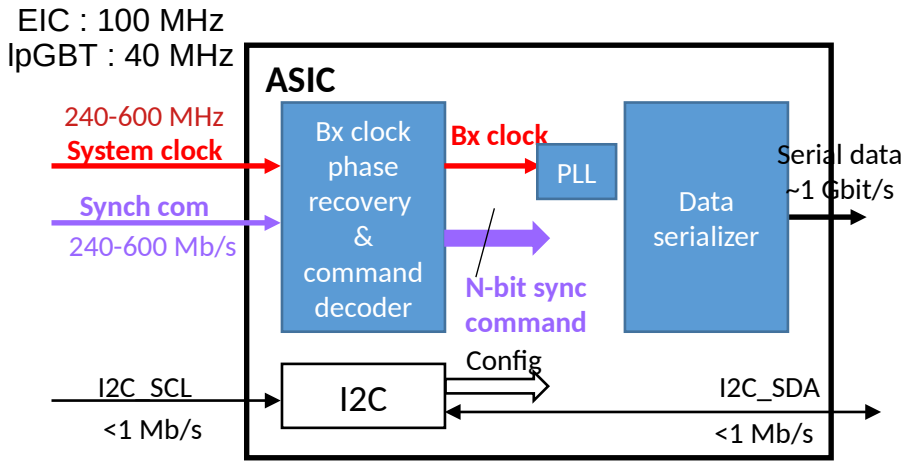
Information data

- Monitoring data: chip configuration, internal chip status (currents, voltages), environmental data (temperature, radiation, etc...)
- Slow-control responses
- Software scaler histogram to evaluate occupancy per channel
- Generated on specific synchronous commands and/or slow-control

CLOCK, FAST COMMAND AND SLOW CONTROL INPUTS

Traditional way

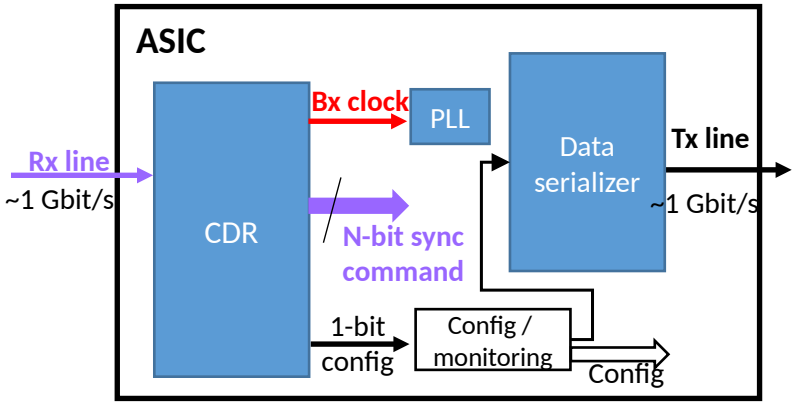
- 1 differential input for clock
- 1 differential input for fast commands
- 1 SDA + SDC I2C input for slow control and configurations
- Implemented in SALSA
- Interface can be used with lpGBT

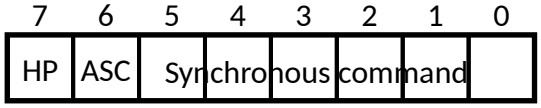


Single encoded line grouping all inputs

- High speed 1Gb/s differential input which carry clock + fast commands + slow-control
- Internal CDR in SALSA to extract the different parts
- 8 bits every 10 ns (EIC): 6 bits for fast command ID, 1 bit for slow-control, 1 parity bit
- Simplify connectivity: 1 diff input for everything instead of 4
- Slow control output through output data stream
- Implementation in SALSA in parallel with the traditional way

Schemes from I. Mandjavidze

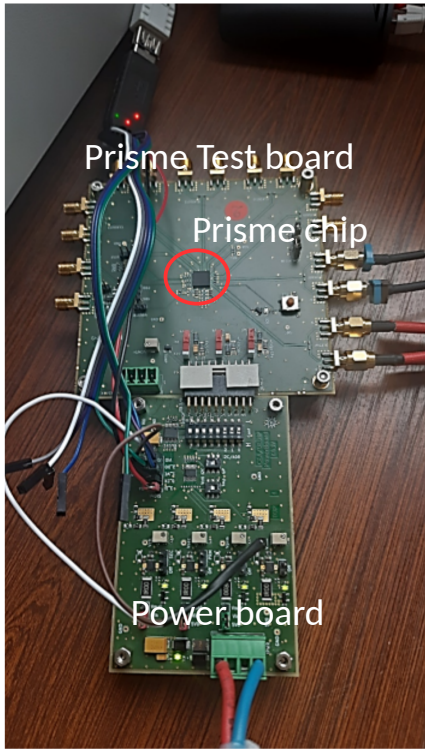




STATUS OF PRISME PLL PROTOTYPE

Test bench

- Power boards + PRISME test boards
- Low jitter clock generator from CERN + high precision signal generator, high end 80GS/s scope and phase noise analyzer

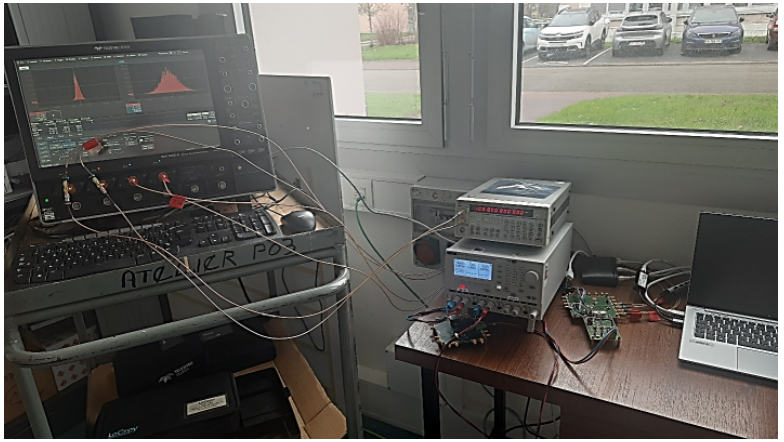


Generic results

- I2C working to read and write registers
- Temperature probe ok, radiation probe ok
- LVDS high speed I/O interface ok up to 1.2 Gb/s
- Clock outputs with adjustable phase and frequencies ok
- Radiation TID tests foreseen in November

Tests on PLL block

- PLL block functional with digital branch working as expected
- Nominal internal 3.2 GHz reached
- Wide input frequency range achieved 80-105 MHz
- Random jitter component as low as 2.5 ps RMS
- But deterministic component larger than expected, up to 50 ps RMS
- Origin identified in simulation from low frequency noise of 3 GHz oscillator
- Solution found, design corrected
- Possible updated chip to be submitted end of 2024



SALSA SYNCHRONOUS COMMANDS, PRELIMINARY VERSION

Context

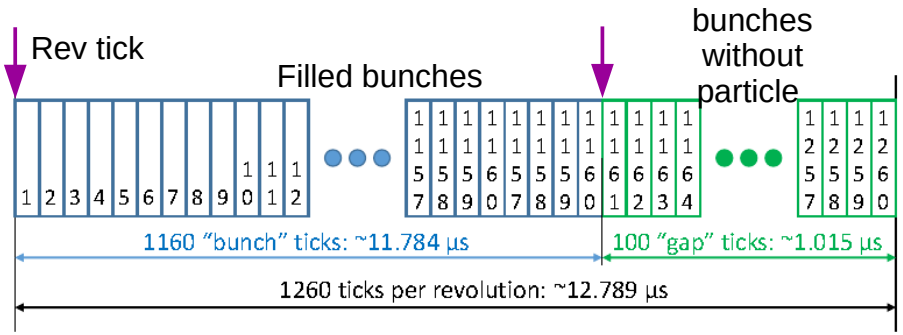
- Commands received from DAQ in synchronization with system clock (98.5 MHz) on 6 bits
- Can be received at each clock with embedded signals, but not in case of split signals

Data taking management commands (those useful for EPIC)

- **T0SYNC**: new time frame → reset packet and clock counters, realign clock phases, and make chip ready to read data in a new time frame
- **STARTREAD**: activate sample data generation in DSP
- **ENDREAD**: deactivate sample data generation in DSP, finish to process remaining samples in FIFOs, then send a specific packet when no more sample is remaining
- **CALIB0...N**: generate calibration data of type N
- **INFO0...N**: generate information packet of type N

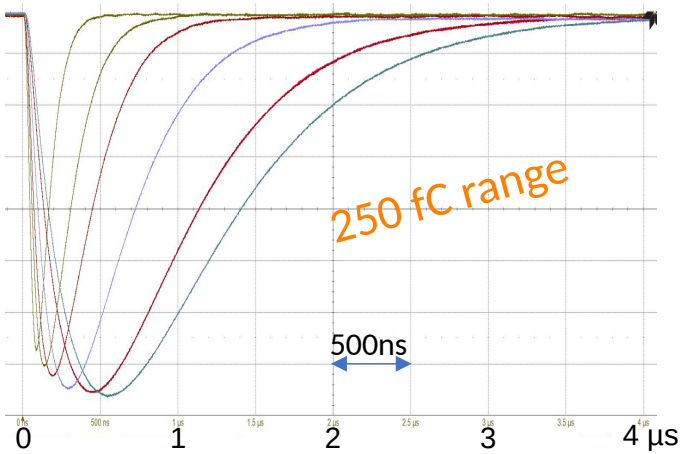
Correspondence with EIC time structure ?

- When do we do T0SYNC ?
  - Each Rev tick ? One over N ?
  - Or do we follow DAQ time frames ?
- Do we read bunches without particle ?
  - We can always get calibration data from that gap even if not reading

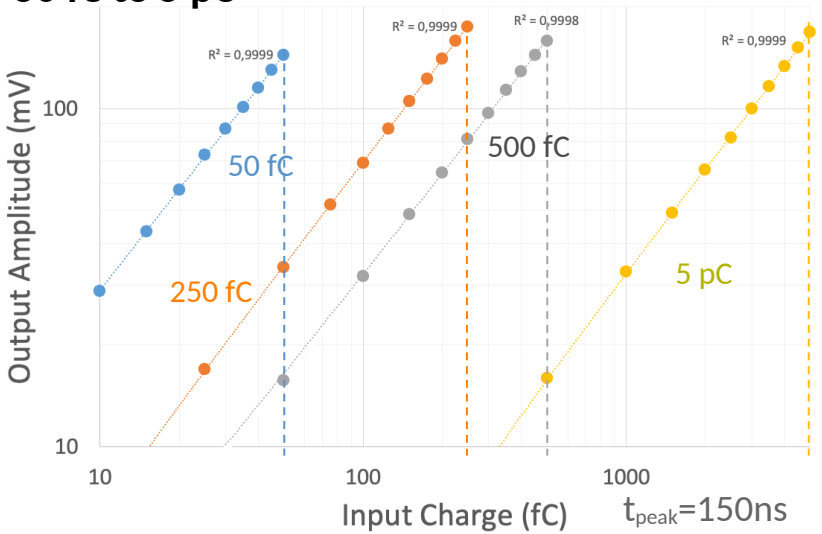


MAIN RESULTS ON SALSA0_ANALOG WITH 120 PF INPUT CAPACITANCE

Peaking time programmable from **50 ns to 500 ns** with no tail

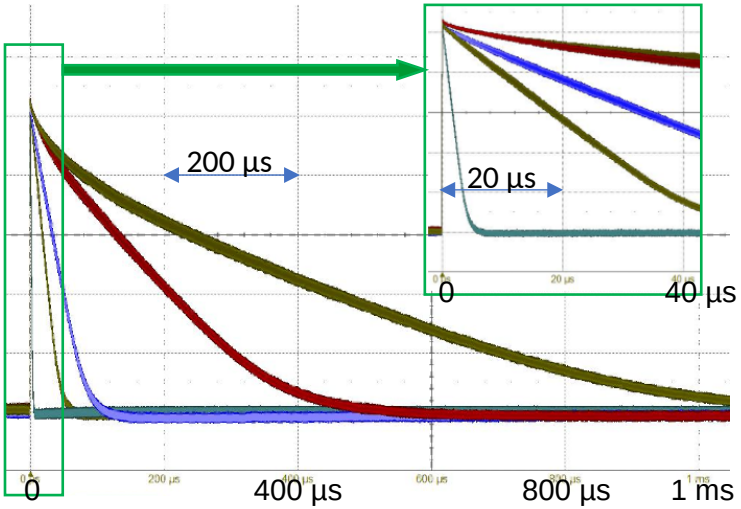


Gain programmable => dynamic range from **50 fC to 5 pC**

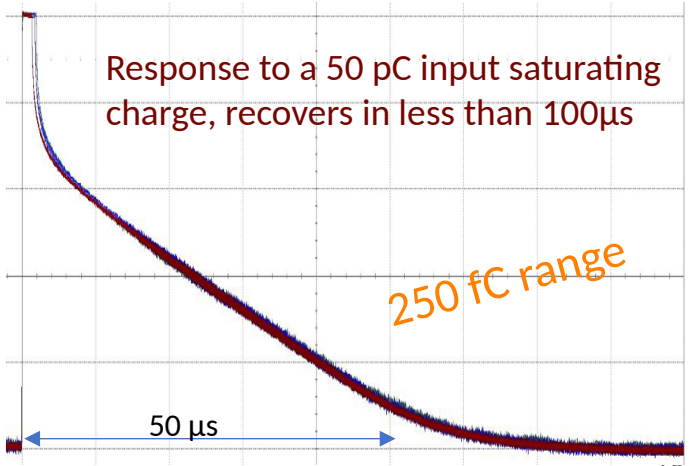


Preliminary

T_{fall} CSA programmable from 5 µs for high rate to 1 ms for low noise



CSA anti-saturation circuit => **fast recovering**

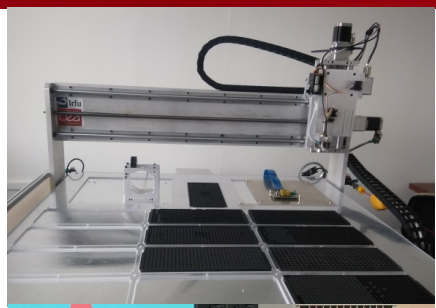


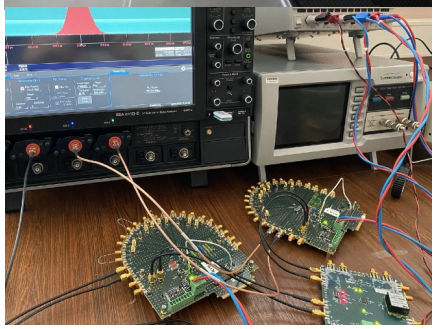
Plots from P. Baron and O. Gevin

QUALITY ASSURANCE

Expertise in ASIC development

- System-level design, production and commissioning
- Readout electronics, acquisition software, analysis (CLAS12, T2K TPC, Asakusa tracker, ALICE TPC)
- Respect of ES&H regulations of host laboratories (BNL, CERN, JLab, J-PARC)





Expertise in large scale ASIC production

- In-house at Saclay: automated ASIC tester robot, test-benches
- In industry: development of turn-key test-benches
- Recent experience: 40k Rafael and 80k Catia ASICs produced and tested for CMS Ph2 upgrade

Test equipment used for SALSA development

- At Saclay: high-end LeCroy and Textronic oscilloscopes
- High performance phase noise analyzer
- Low jitter precision clock sources
- Climate chamber
- Bonding machine

Test facilities to be used for SALSA

- Radiation facilities at Saclay, Sao Paulo, CERN and in Europe
- High magnetic field facilities at Saclay and CERN