sPHENIX TPC grounding

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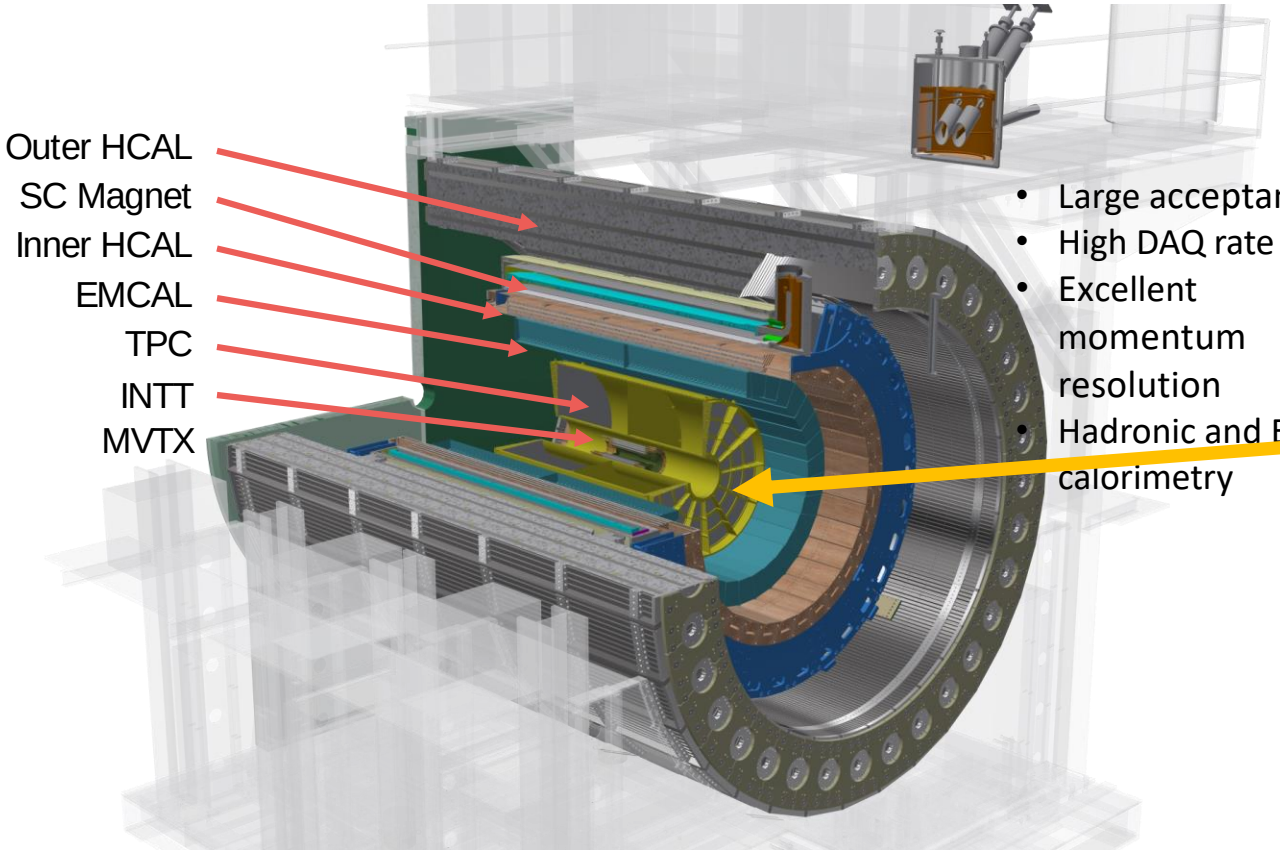
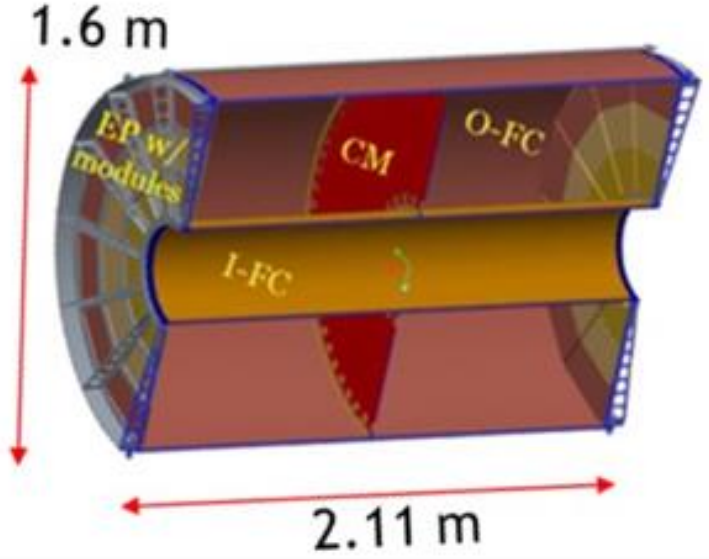
sPHENIX and TPC

- TPC is the primary tracker in sPHENIX at RHIC



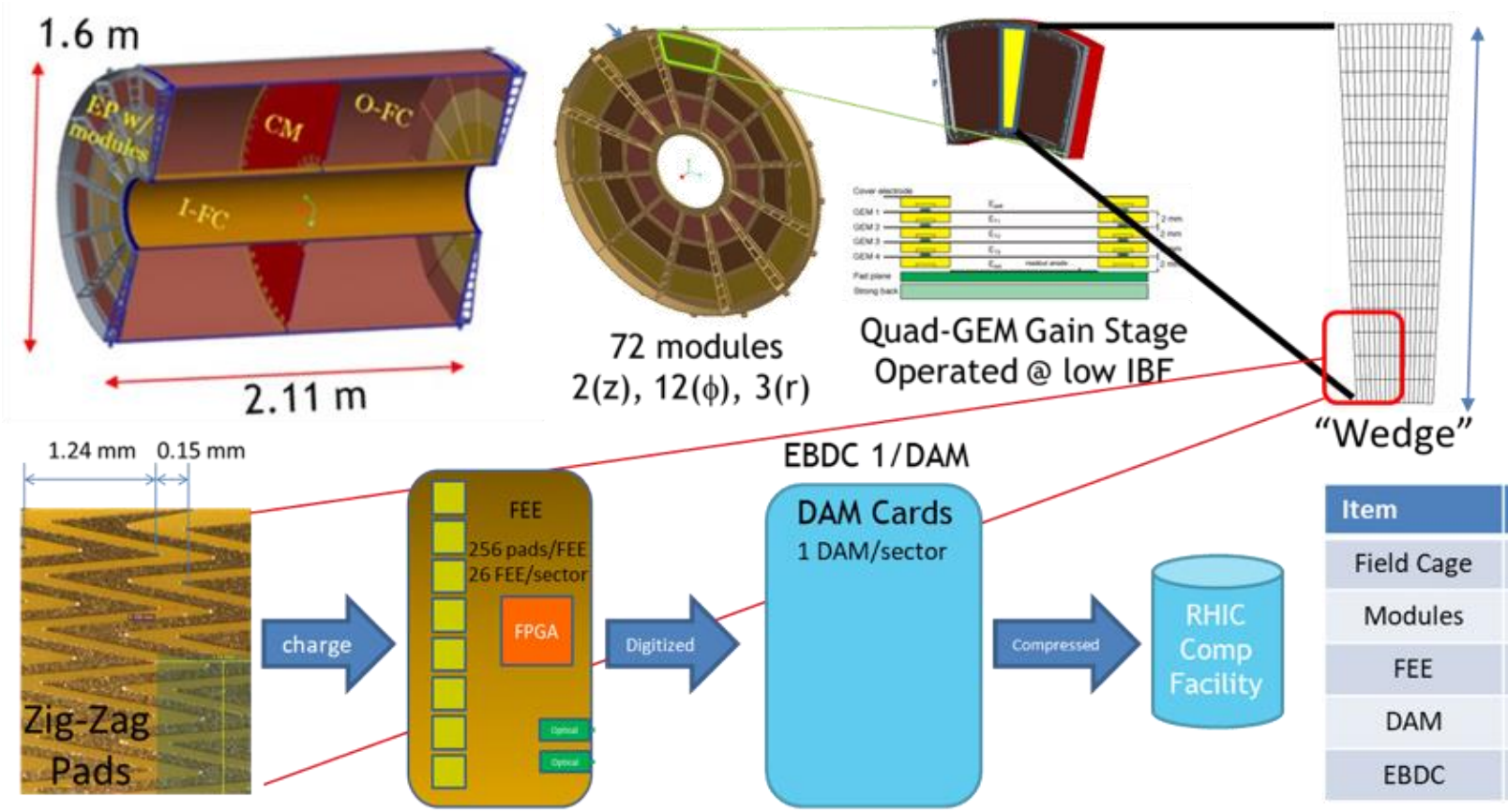
- Large acceptance
- High DAQ rate
- Excellent momentum resolution
- Hadronic and EM calorimetry



sPHENIX and TPC

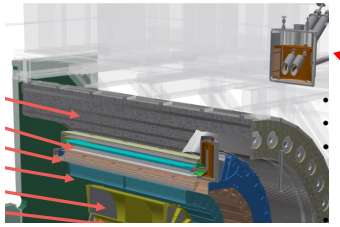
- ~1/30 of ALICE TPC Volume. It allows ~100KHz collision rate. No gating grid.
- Gas: Ne+CF_4 → Ar+CF_4 → Ar+CF4 +isobutane

FEE: Front-End Electronics

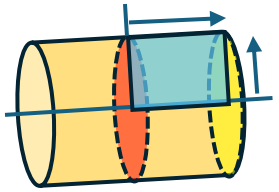


Item	Count
Field Cage	1
Modules	72
FEE	624
DAM	24
EBDC	24

TPC connection diagram (1/2 of one side)



MPOD HV1 and HV2 are set to be the same voltage as the top of the first GEM



sPHENIX carriage

Power Racks (on the third floor in IR)

CM HV (-42kV)

MPOD HV1,2 return

MPOD HV1

Endcap (tied to sPHENIX frame)

DG: digital GND
AG: analog GND

Outer radius field stripe

pads

AG

DG

FEE

LV PS (to LV rack)

FEE

FEE

FEEs use 4V(dig), 2V(dig), and 2V(ana)

GEMs

FEE

GEM HV dist. card

GEM HV PS

Inner radius field stripe

Safety ground shell

MPOD HV2

Padplane GND

Beam pipe

HV PS rack 1

CM HV

GND

MPOD HV

GND

HV PS rack 2

GEM HV

GND

LV PS rack

FEE 4V (dig)

GND

FEE 2V (dig)

GND

FEE 2V (ana)

GND

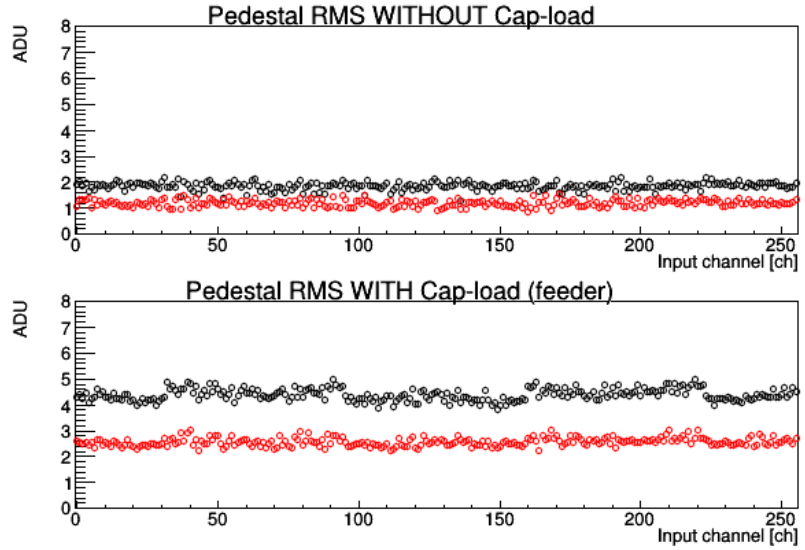
220V GND

Noise situation of the sPHENIX TPC

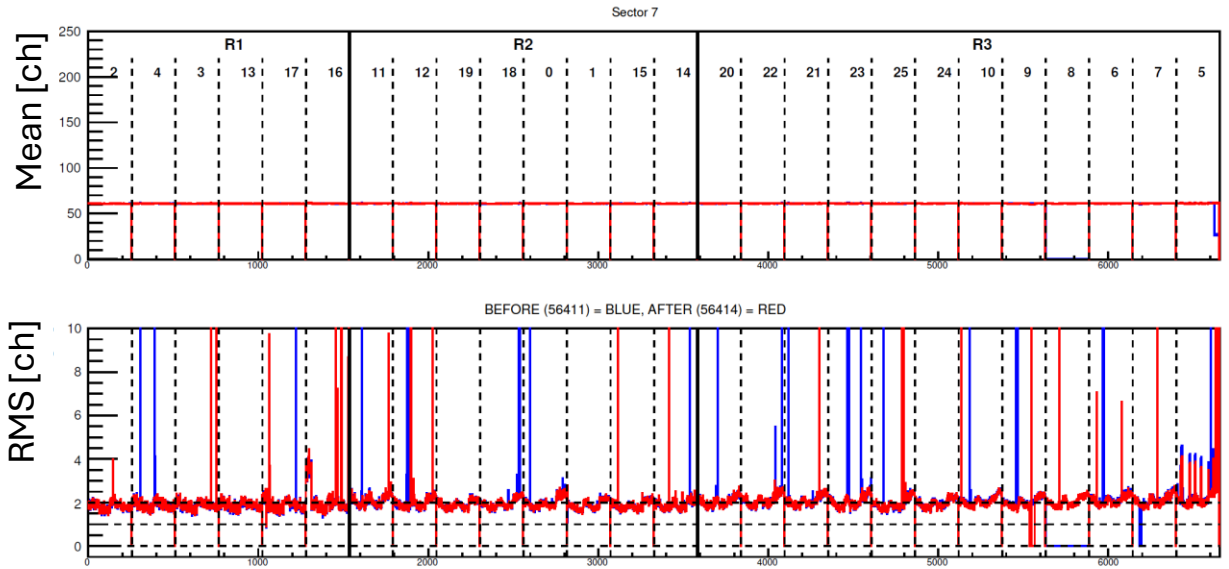
- Noise level of the FEEs measured at the testbench is on or close to the theoretical limit
  - σ_{ADC} = ~2ch at the gain of 20mV/fC, with a detector-equivalent cap-load (~18pF)
  - Simulation of the SAMPA chips showed the similar level.

- Noise level of the FEEs on the TPC is comparable (or even better?)
  - We will walk though the components that we think contributed to the low noise.

One FEE result at testbench, Black: 30mV/fC, Red: 20mV/fC

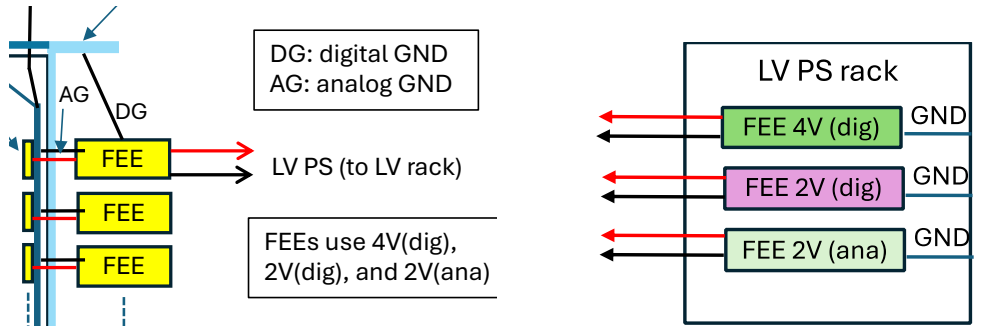


One-sector FEE result on the TPC, 20mV/fC. Look at only Red



1: Strong grounding of the FEEs

- A FEE consists of eight SAMPA chips, FPGA, and optical transceivers (+some peripheral).
  - 32 ch * 8 = 256 channels
  - JTAG communication over optical fiber is also implemented
- A FEE uses 4V(dig), 2V(dig), and 2V(ana).
  - 4V (dig), 1A, for FPGA running
  - 2V (dig), 3A, for FPGA and SAMPA digital (ADC and DSP)
  - 2V (ana), 3A for SAMPA analog (pre-amp, shaping and ADC reference)
- For minimizing power and heat dissipation, we decided not to make 2Vs by regulating from 4V, instead to provide them separately.
- LV powers sit on the third floor of sPHENIX carriage
  - ~15m from LV power supplies to the ends of the TPC
  - Needs careful design of distribution to minimize power dissipation on the cables, too



LV power distribution

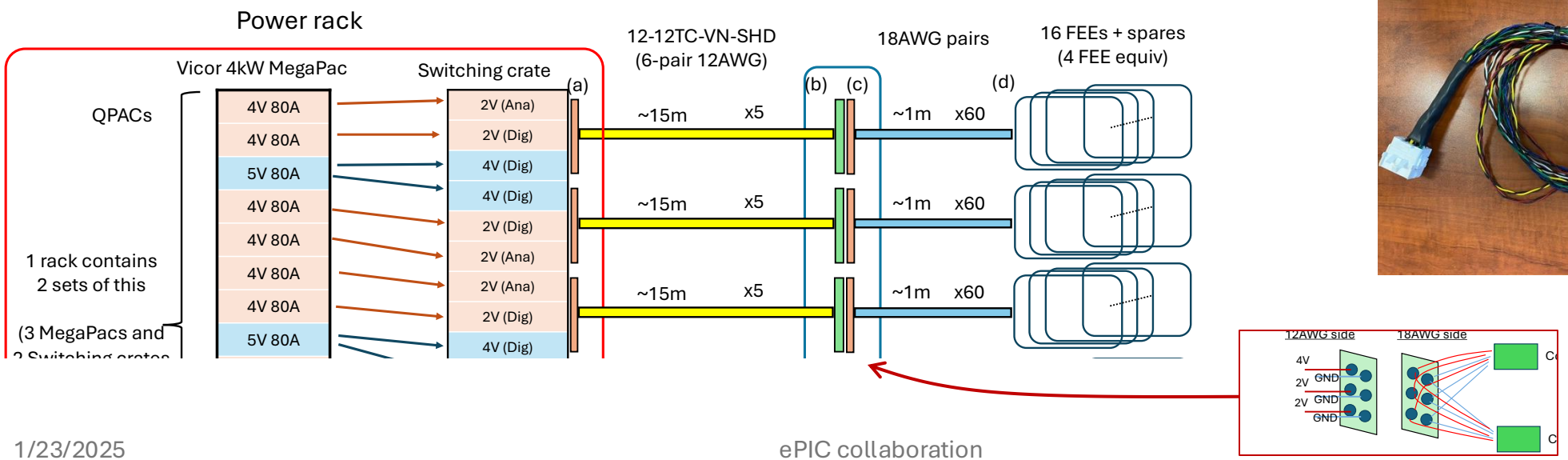
- Cables from the PS to the FEE are long.
  - If the cable impedances are large, there will be large voltage drops
  - This results in instability of FEE supply voltages which contributes to noise.

- 5V PS for 4V, 4V PSs for 2V, followed by thick cables.
  - 12AWG cables up to the ends of TPC, 18 AWG from the ends to FEEs
  - With 3A current, V drop is 1.2V for round-trip of 15m from PS to FEEs

- Power lines and their returns became strong AC and DC grounds
  - We have 312 FEEs per side → 936 thick ground lines running to the FEEs

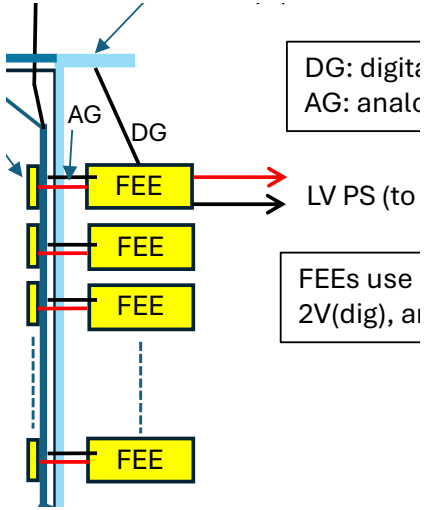
12AWG cable

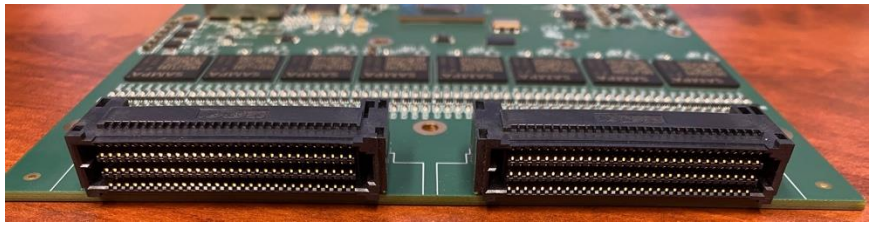
18AWG cable

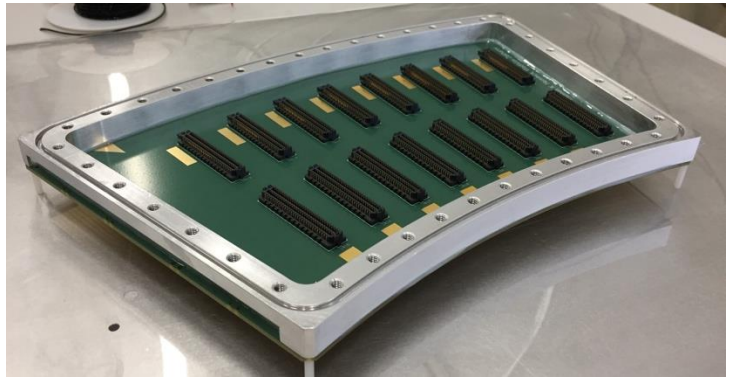


2: Padplane grounds connected to FEE grounds

- FEE has very solid grounds for 4V (dig), 2V (dig) and 2V (ana).
- FEE employed two 180-pin connectors to interface padplanes
  - Number of pins needed is 256 (signal) + 1 (control). Other 103 pins are connected to analog ground of the FEE.
  - 180 pins = 6 rows of 30 pins. One whole row is dedicated to ground.
- Analog grounds of the FEEs are connected to pad plane ground through the 103 pins
  - Thus, the padplane ground is very tightly connected to the (multiple)-FEE analog grounds
  - 6 FEEs on R1, 8 FEEs on R2, and 12 FEEs on R3.

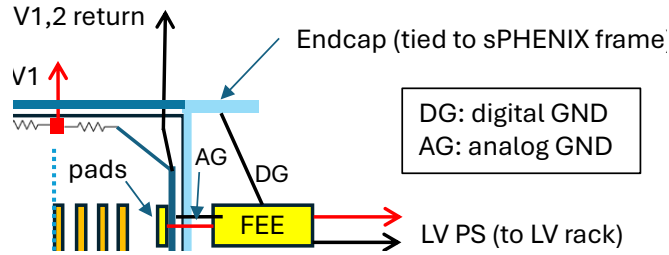


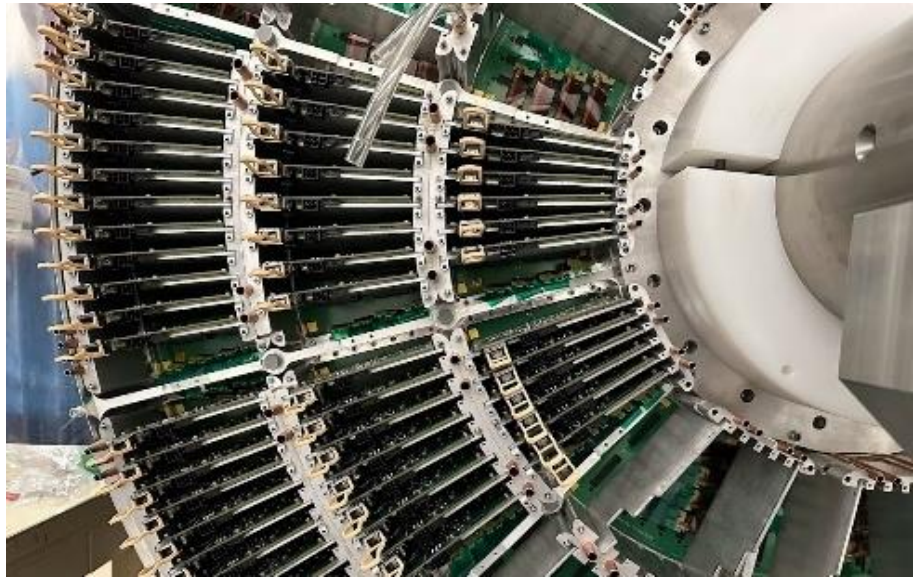


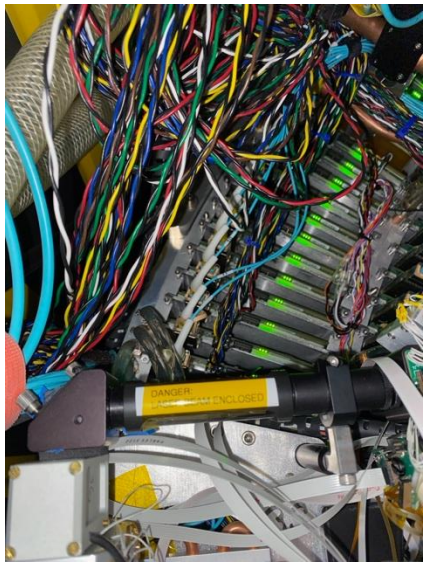


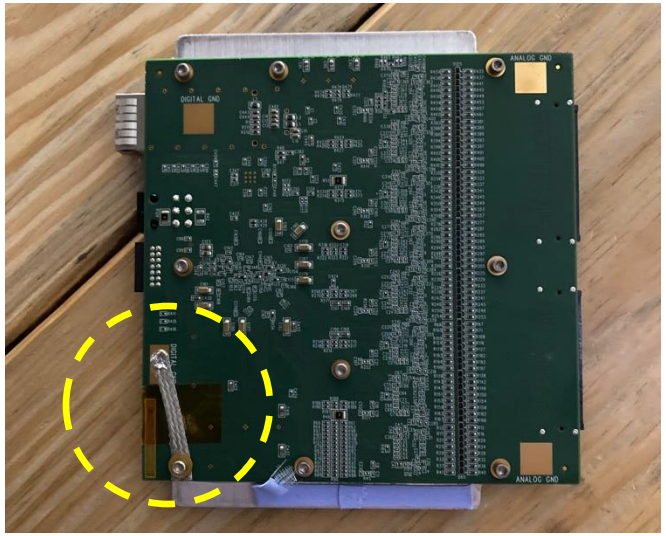
3: TPC frame connected to FEE GND

- TPC endcaps hold FEEs and cooling blocks (for FEE cooling).
- Cooling blocks/ endcaps as a good shielding against outer noise
  - The endcaps are connected to the sPHENIX carriage (and earth ground)
  - We thought the endcaps are ground ground, but it was not.
- Connecting FEE dig-GND to cooling blocks significantly reduced noise.



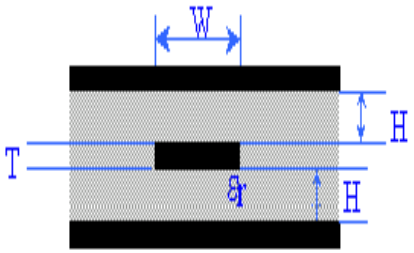


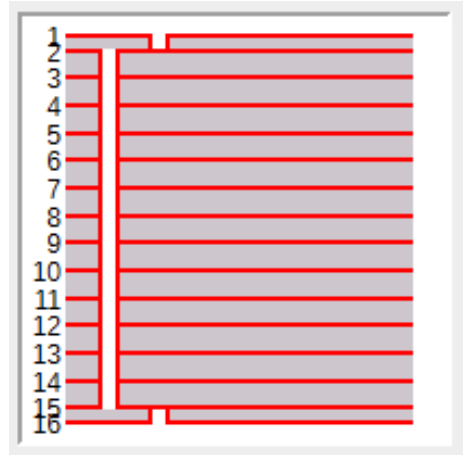


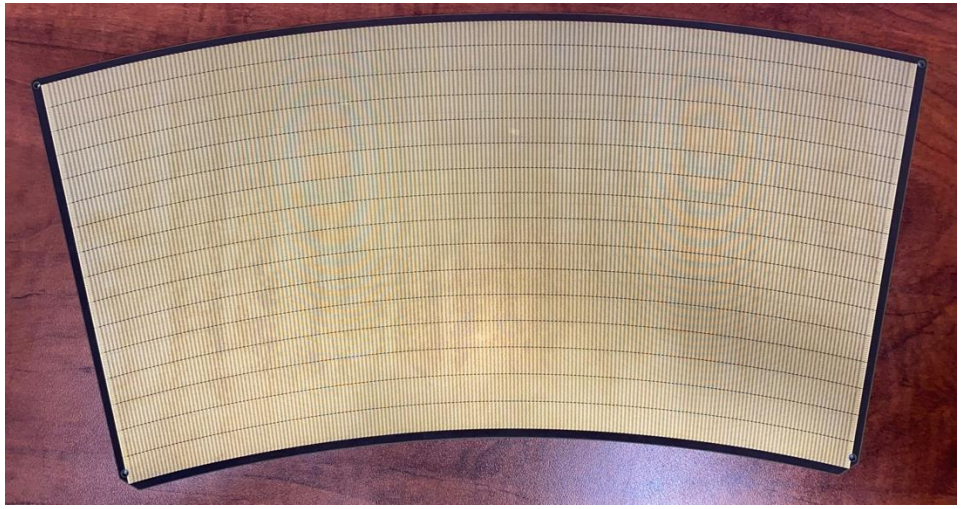


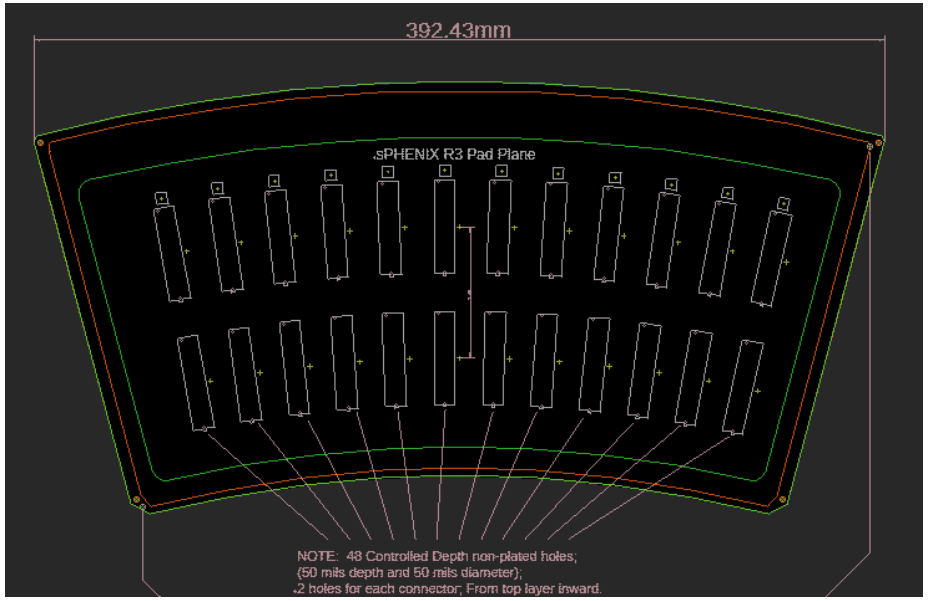
4: AC grounding at padplane

- Padplane has 16 layers
- Traces from pads to FEE conn. pins are sandwiched by ground planes
  - Strongly AC-coupled to grounds
  - Capacitance between pads and the ground is already considered in designing electronics
  - Ground planes are connected by ~250 micro-vias
- AC-coupling is so strong that the traces and pads don't pick radiated noise from outside TPC.









sPHENIX TPC experience summary

- People realizes the importance of the grounding and usually takes decent time to design carefully.
- However, the grounding is very complicated. It often results in unexpected poor performance.
  - People then starts playing with grounding by connecting one to another.
  - “Connecting everything everywhere” is a typical end-result of grounding.
- It is important to realize that the playing ground is successful when there is a “golden strong ground” around the detector.
  - If the ground is weak, it just ends up with many ground loops which would worsen the situation.
- sPHENIX TPC benefited from the very strong grounds of the FEEs.
- Strong power lines for signal readout electronics is most straightforward and useful
  - Good performance of analog/digital circuit requires descent power current, to begin with.
  - Large current means large voltage drop of the supplied voltage at the FEE.
  - Voltage drops result in poor performance and instability of the electronics.
- Good designing of the LV power distribution solves most of the readout problems and helps reducing noise from other sources, too.