



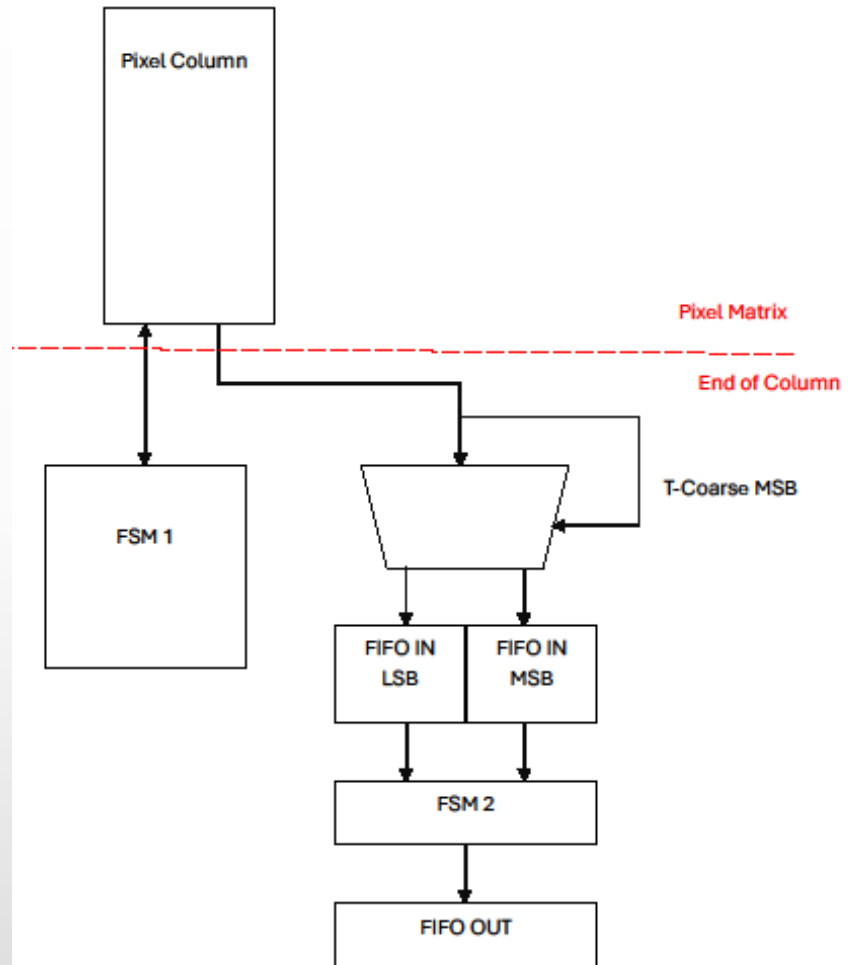
Torino ALCOR DAY

18-09-2024

Giulio Dellacasa



EoC



- Enable:
 - Start Frame counter
 - Start State Machines
 - Write Header 0x1C1C1C1C
 - Write Frame Number
- Read LSB FIFO until half-frame (MSB Coarse = 1) and FIFO LSB not Empty
- Half-Frame:
 - Read LSB FIFO until not empty
 - Wait for timeout (9-bit counter 2060 ns, it was 3200 ns in Alcor 0-1-2)
- Read MSB FIFO until frame rollover and FIFO MSB not empty
 - Wait for timeout
- Write Status Header / Status / CRC / Trailer

Comments

- Soft Reset acts on the Coarse Counter (both in Pixels and End of Column) but it has no effect on the Frame Counter
- To avoid rollovers during configuration a burst of soft reset can be sent
- Coarse counter reset: special cases
 - The same frame contains data before and after the reset. Can be impossible to distinguish them from each other (more evident at low rates)
 - Soft reset changes MSB Coarse Counter (from 1 to 0). FSM is reading the wrong FIFO while new data are stored in the other FIFO (FIFO full, events sent at the net frame)
 - The frame number can't be used to recover an absolute time from data (maybe not an issue)
- What if Soft Reset acts on Frame Counter and Coarse Counter?
 - A sort of “rollover” mechanism should be implemented to avoid problems showed above
 - Carefully understand to treat incoming data in the while
- What if Soft Reset acts on data and State Machines too?
 - TDC reset
 - Pixel FSM reset
 - EoC input data reset?
 - EoC trailers and new header
 - New header only? (Previous frame is truncated). Fastest solution
- Both solutions require changes to the FSM and the operation can't be done in few clocks (if you want to have frames with full trailers)