Frame (counter) misalignment

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Frame counter alignment issues

- *Frame counter* is reset only with **HARD RESET**
- **SOFT RESET** only resets *Coarse counter*
- *Frame counter* incremented at every *Coarse counter* rollover
- *Coarse counter* starts with ECCR configuration → process not synced, can take more than one *Coarse counter* rollover (102.4 μs)

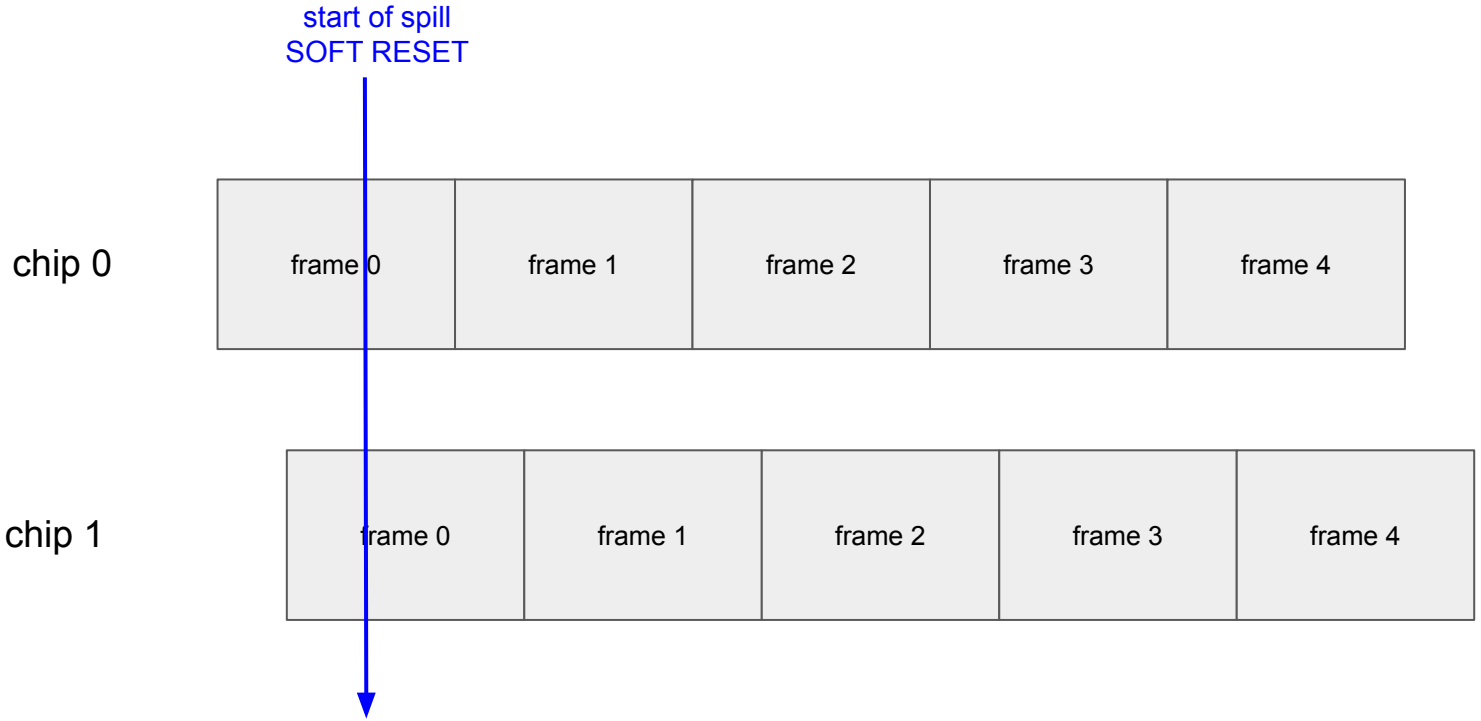
When we perform ECCR configuration we start *Coarse counters* for each sector/chip at different times → these *Coarse counters* are not aligned and they can increment the *Frame counters* at different times as well

Coarse counters will be synced afterwards (by START of SPILL SOFT RESET), **but misalignment on *Frame counters* will be not recovered!!!**

❑ ***Frame counters*** misalignment or ***Frames*** misalignment ?

Frames misalignment

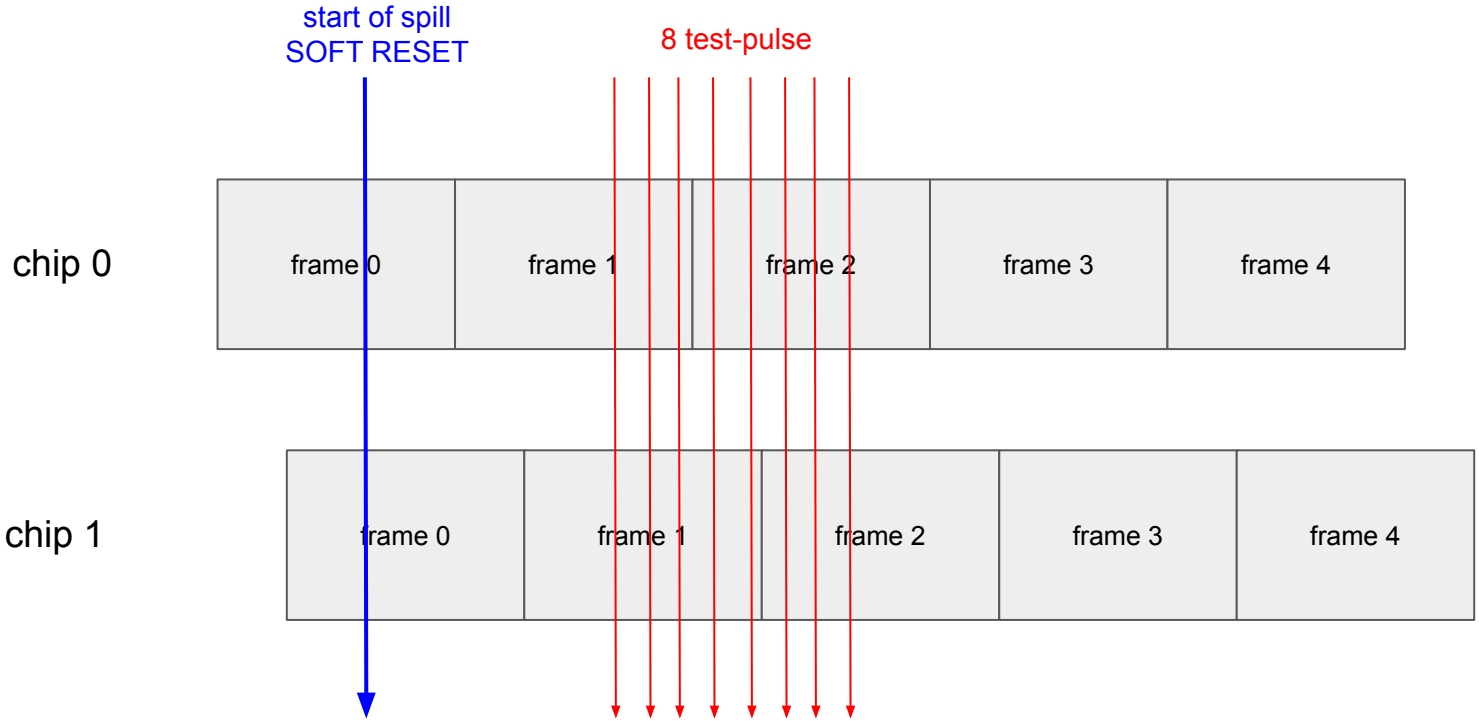
frame numbers just as a reference, number misalignment can be much higher (according to ECCR programming sequence delays)



1. SOFT RESET does not align frames: misalignment not only on Frame counters but also on Frames

Frames misalignment

frame numbers just as a reference, number misalignment can be much higher (according to ECCR programming sequence delays)

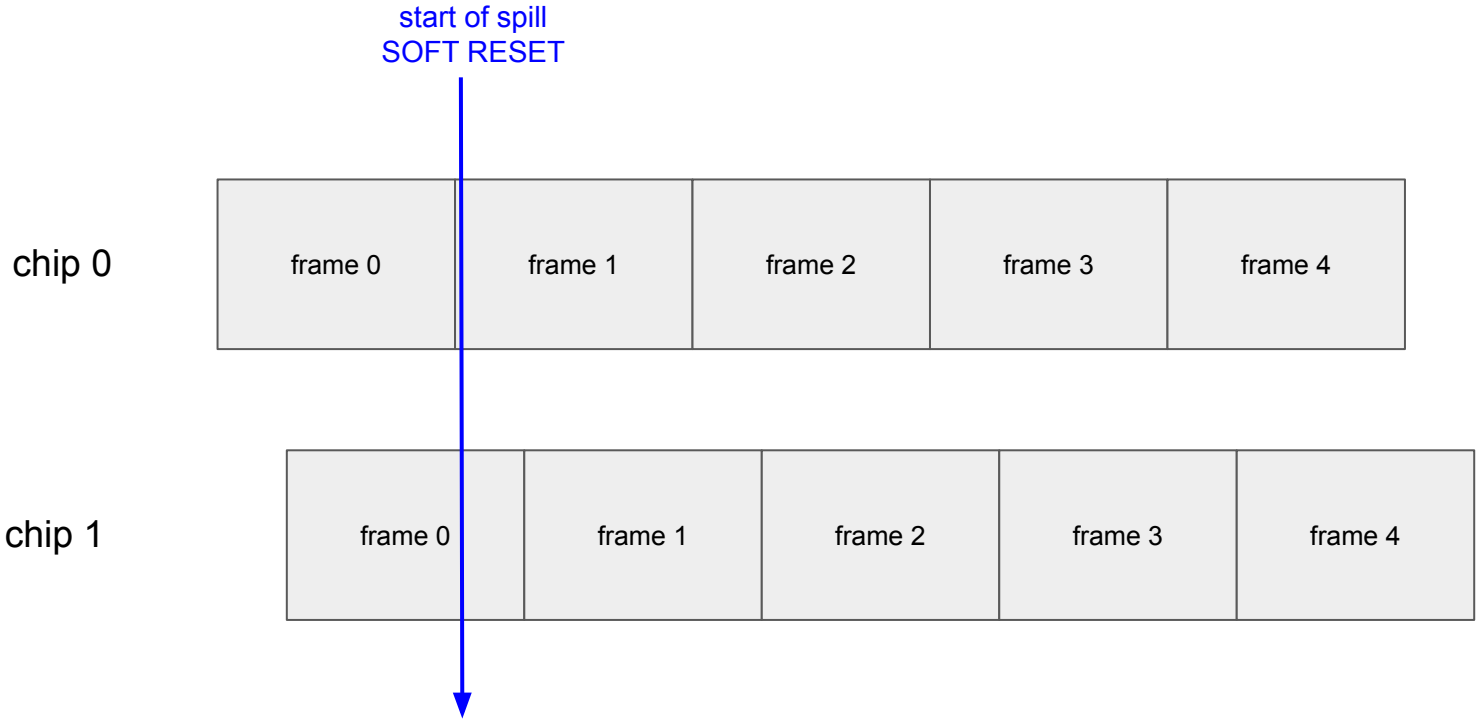


Expected output:

- chip 0: 3 tp from frame 1, 5 tp from frame 2
- chip 1: 5 tp from frame 1, 3 tp from frame 2

→ frames are **not aligned**: cannot reconstruct test-pulse timestamps with correct frame reference

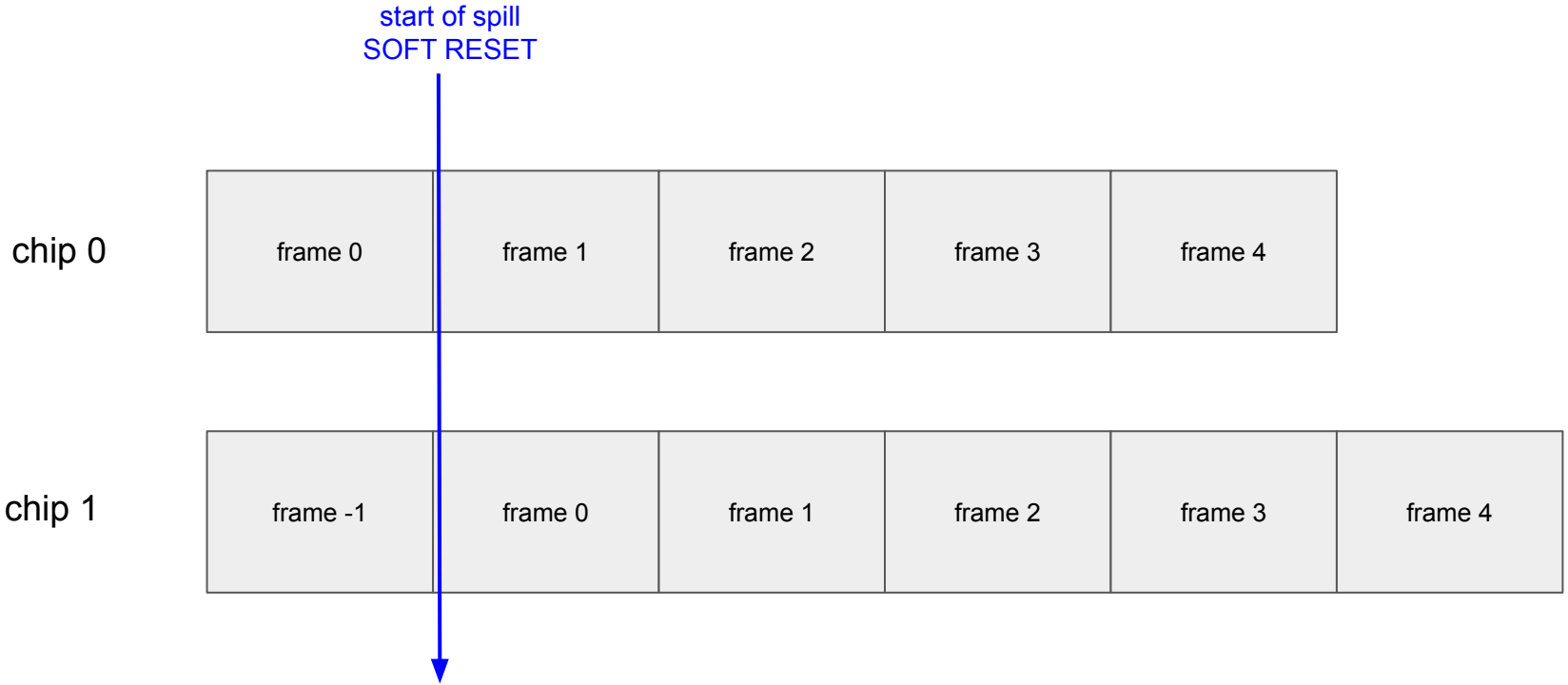
frame numbers just as a reference, number misalignment can be much higher (according to ECCR programming sequence delays)



After “start of spill” SOFT RESET the frames are coming out synchronized

Frame counters misalignment

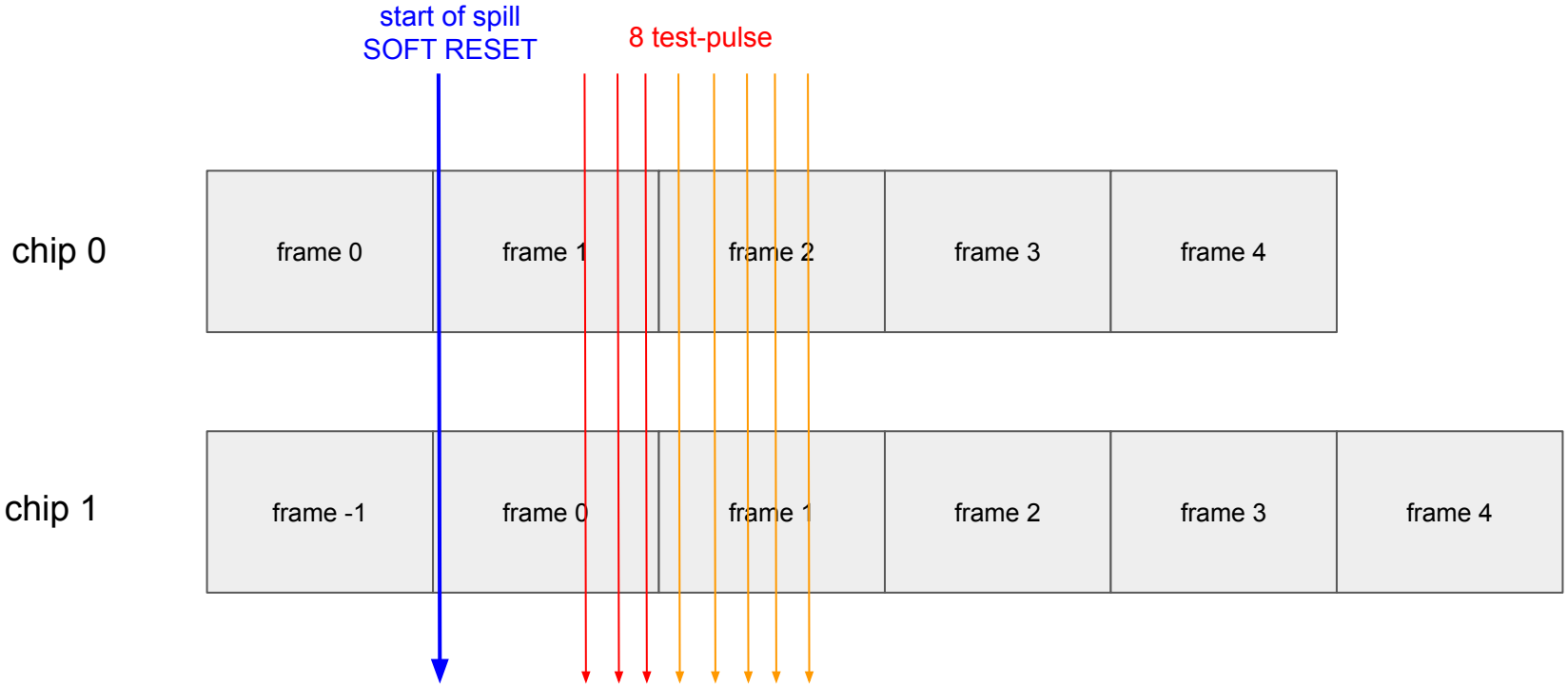
frame numbers just as a reference, number misalignment can be much higher (according to ECCR programming sequence delays)



2. SOFT RESET does align frames: misalignment only on Frame counters but Frames are ok

Frame counters misalignment

frame numbers just as a reference, number misalignment can be much higher (according to ECCR programming sequence delays)



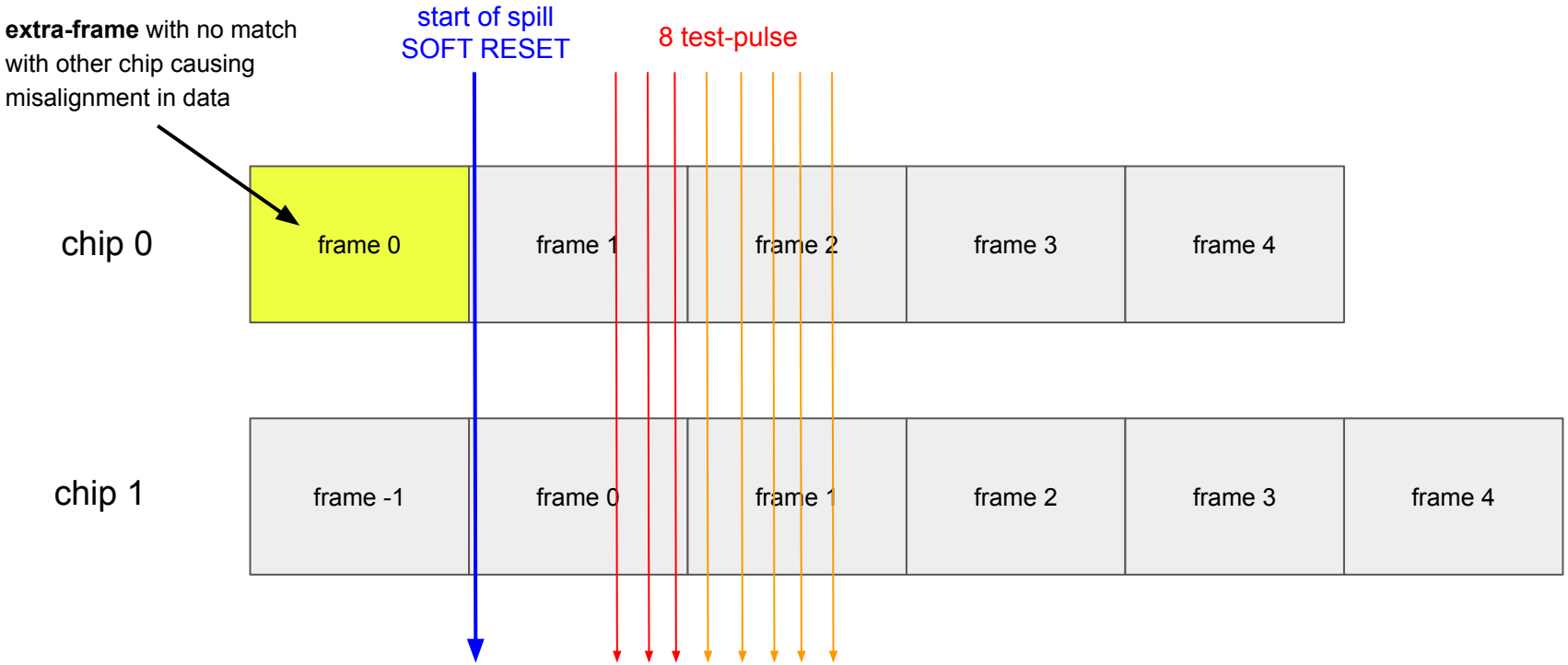
Expected output:

- chip 0: 3 tp from frame 1, 5 tp from frame 2
- chip 1: 3 tp from frame 0, 5 tp from frame 1

→ frames are **aligned**, only frame number is misaligned

Frame counters misalignment

frame numbers just as a reference, number misalignment can be much higher (according to ECCR programming sequence delays)



Expected output:

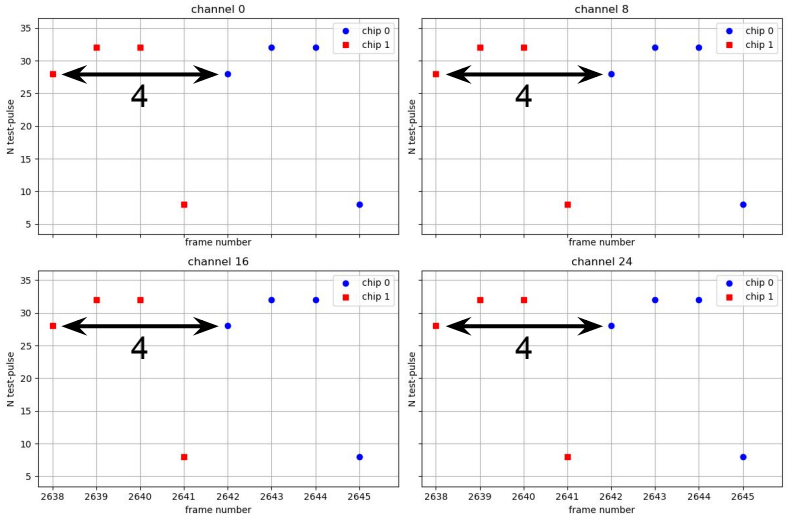
- chip 0: 3 tp from frame 1, 5 tp from frame 2
- chip 1: 3 tp from frame 0, 5 tp from frame 1

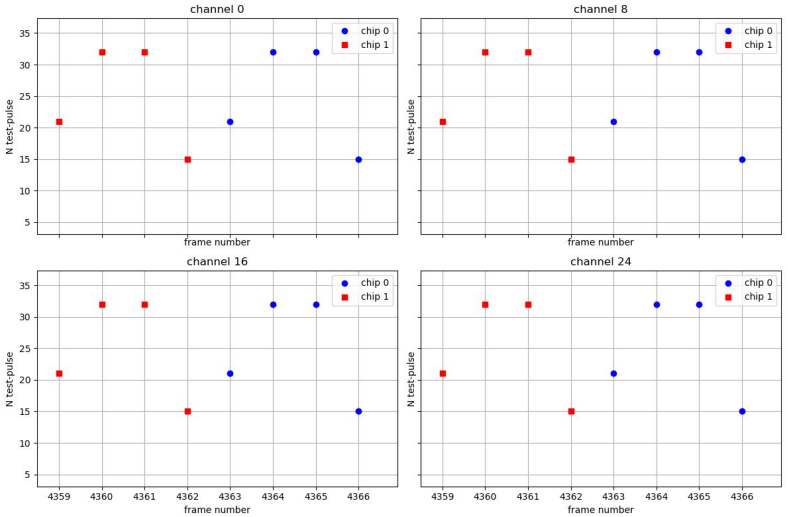
→ frames are **aligned**, only frame number is misaligned

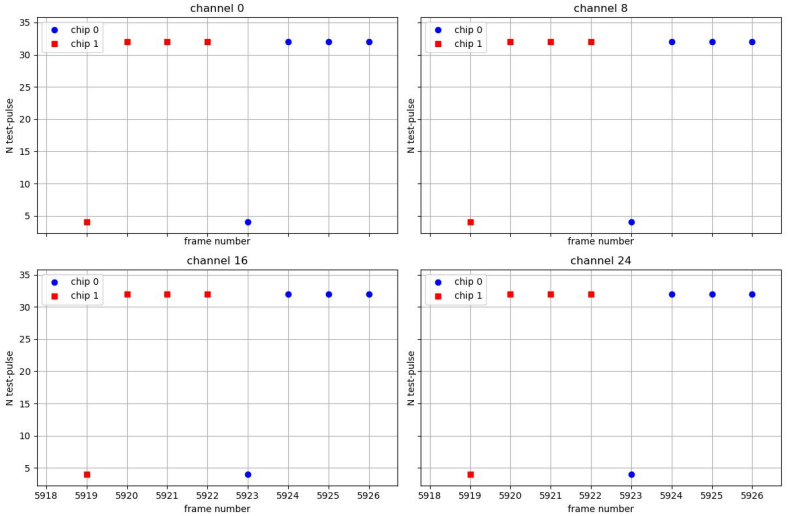
Study frame misalignment with test-pulse

- 1 FE DUAL (2 chips), bursts with 100 test-pulses each to both chips, on 4 channels (0, 8, 16, 24, one for each lane)
- Test-pulse separated by 1024 clock cycles → distributed in more than one frame (1 frame is 2^{15}=32768 clock cycles): $1024 \cdot 100 = 102400$ clock cycles → 4-5 frame (according to when first tp occurs w.r.t. frame), 32 tp in a full frame

1. SOFT RESET does not reset ALCOR EoC Coarse counters → Frames come out not synced for the 4 lanes and 2 chips → Expect to have 2 chips and 4 lanes with different number of test-pulses distributed in the 4-5 frames
2. SOFT RESET does reset ALCOR EoC Coarse counters → Frames come out not synced for the 4 lanes and 2 chips (with “only” frame number misaligned) → Expect to have 2 chips and 4 lanes with same number of test-pulses distributed in the 4-5 frames (with “only” frame number misaligned)



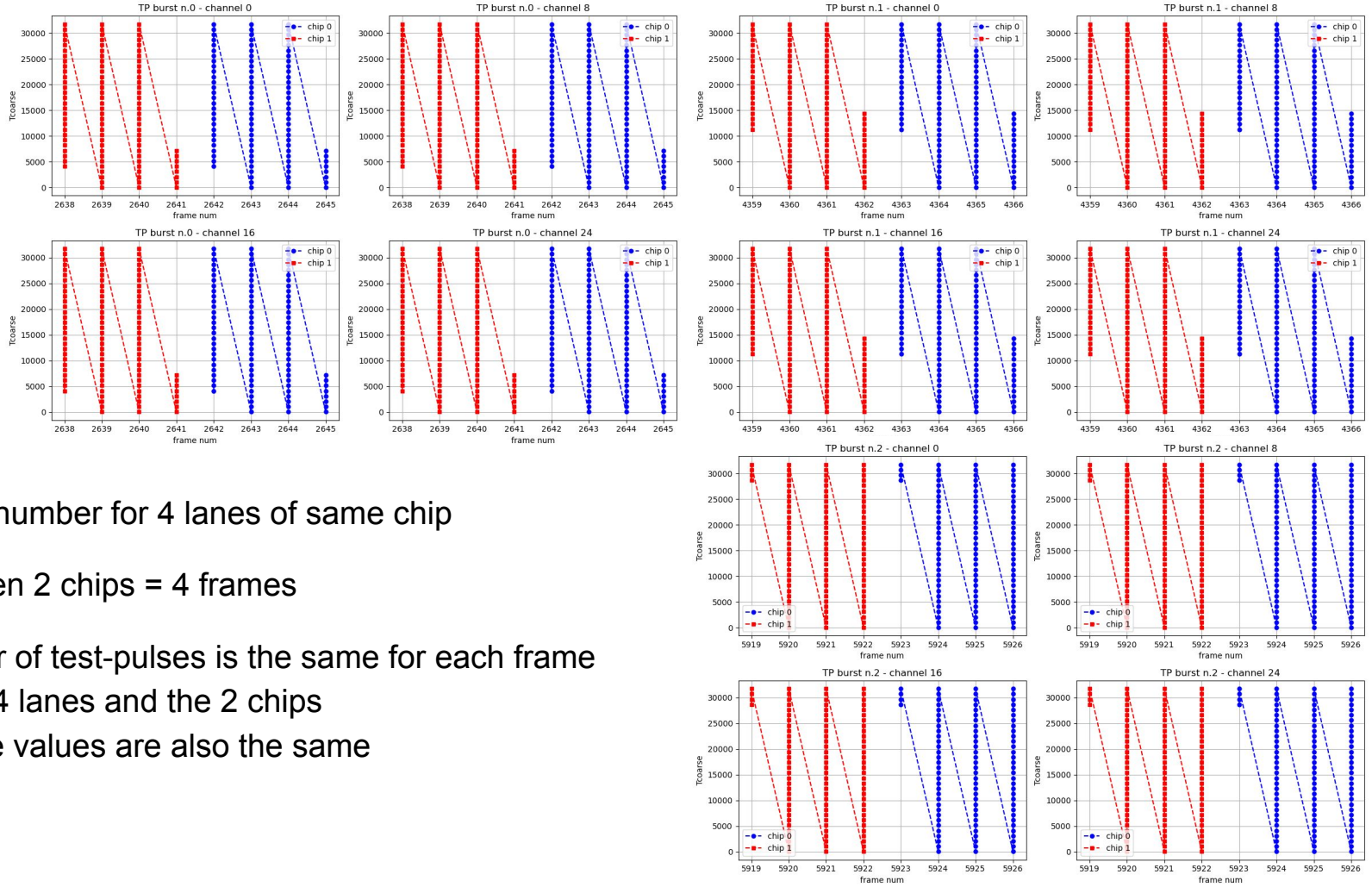




Same frame number for 4 lanes of same chip

Offset between 2 chips = 4 frames

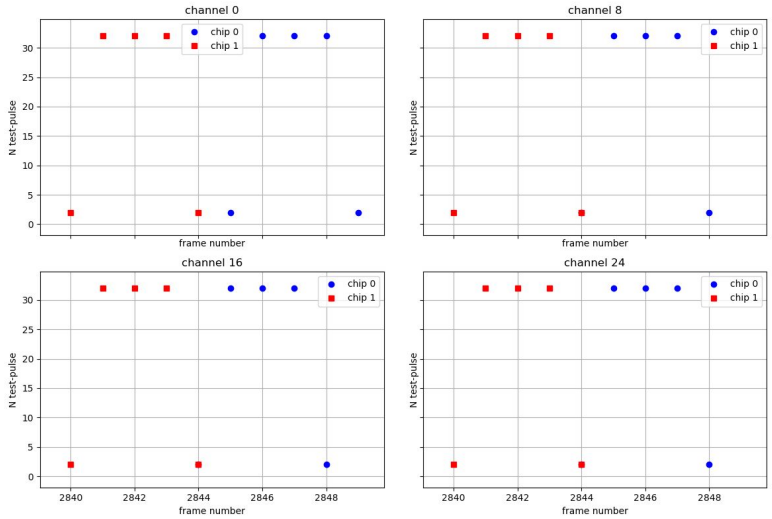
- Number of test-pulses is the same for each frame for the 4 lanes and the 2 chips

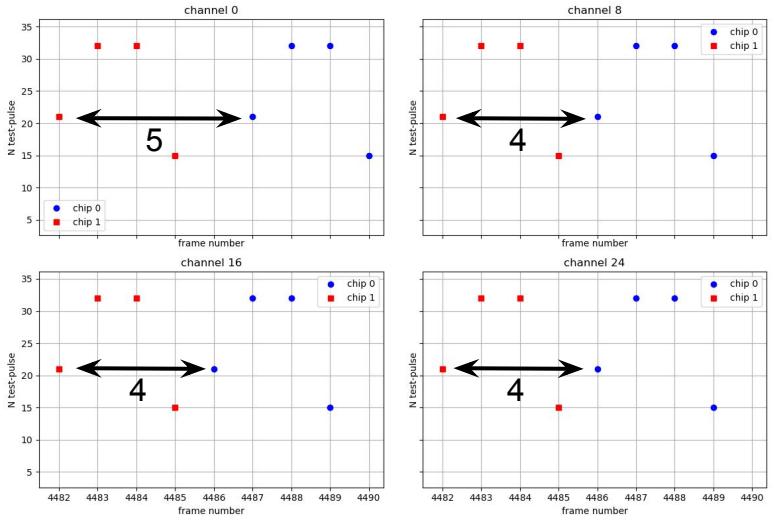


Same frame number for 4 lanes of same chip

Offset between 2 chips = 4 frames

- Number of test-pulses is the same for each frame for the 4 lanes and the 2 chips
- Tcoarse values are also the same



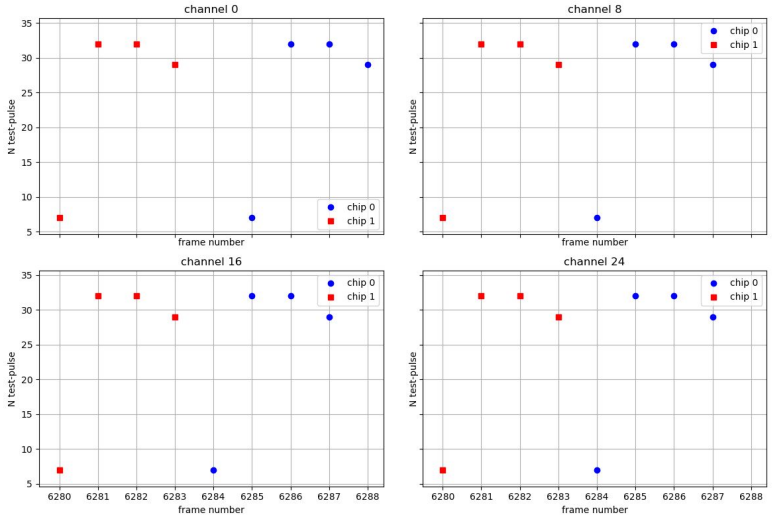


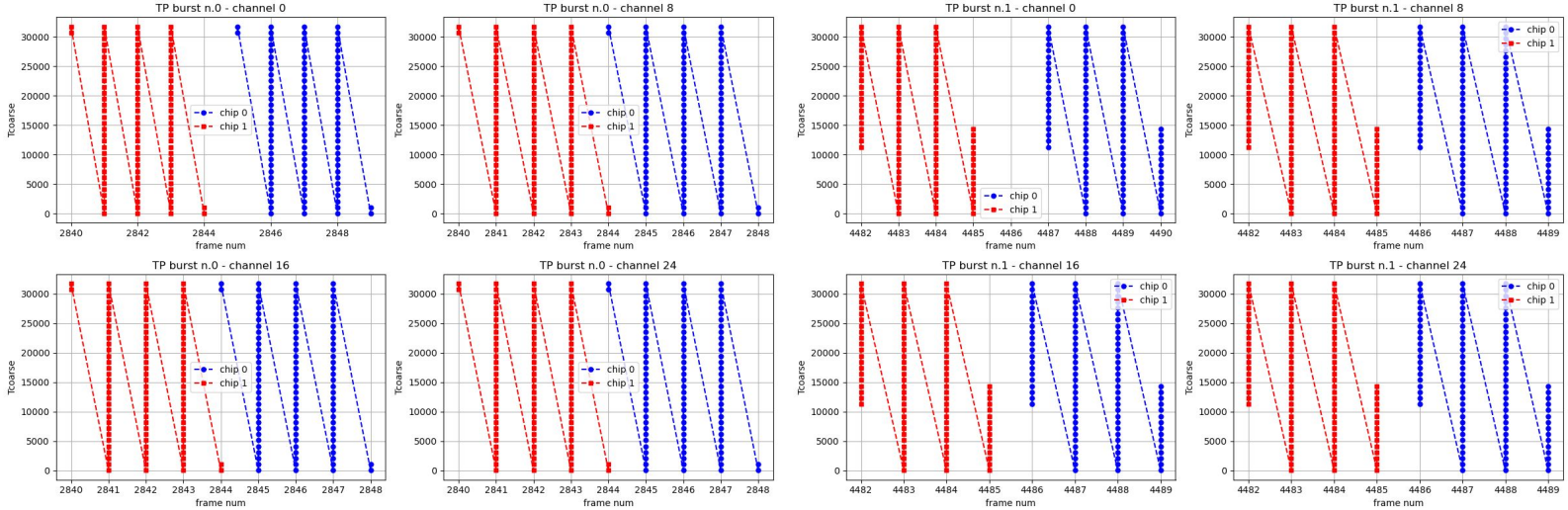
Chip 0, lane 0 has one additional frame offset

- Offset between 2 chips = 5 frames (lane 0)
- Offset between 2 chips = 4 frames (lanes 1,2,3)

Still

- Number of test-pulses is the same for each frame for the 4 lanes and the 2 chips





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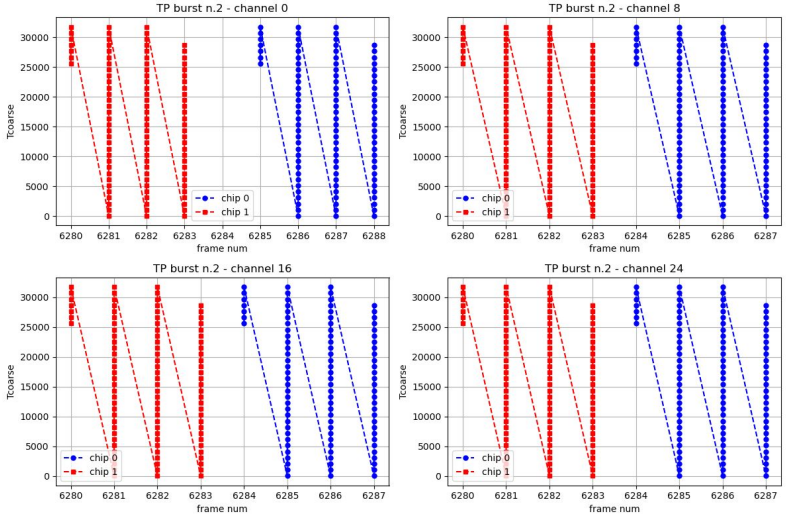


Frame misalignment ?

What is this frame additional offset occurring sometimes?

- Small time offset in start of data readout from DAQ FPGA or different delay in data transmission from 2 ALCOR chips → sometimes, some lanes have one more frame at the start which does not match with anything from other lanes/chips

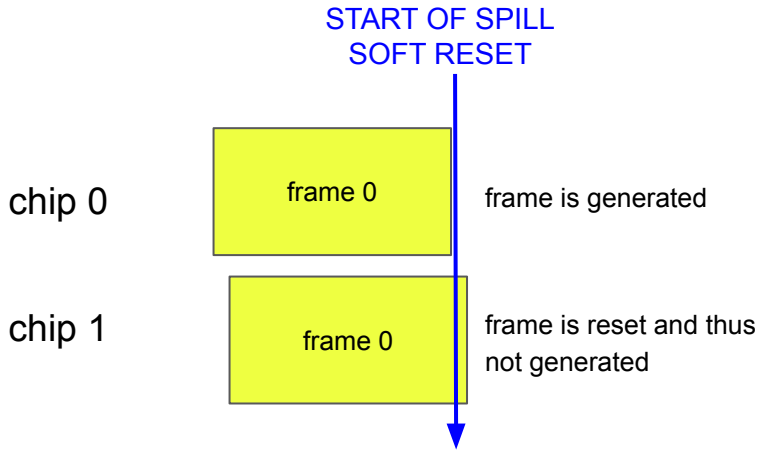
With correct numbering from ALCOR Frame counter this will not be a problem → Align frames from Frame number

I assume Start of Spill signal is not synced with ALCOR

- Try to put Start of Spill signal well separated from frame/rollover words (they are synced by SOFT RESET) → SYNCED SOFT RESET …… wait …… Start of Spill

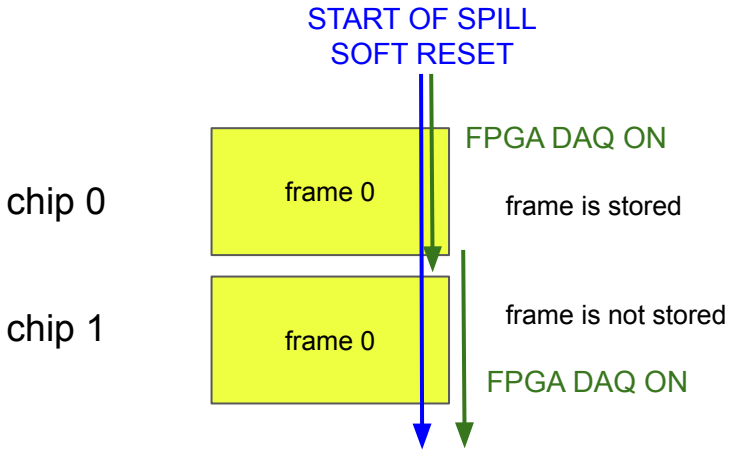
START OF SPILL - SOFT RESET interplay

- START OF SPILL defines when we start to save data from ALCOR into the FPGA ?
- SOFT RESET defines timing frame/rollover output from ALCOR ? Yes (99%)
- If these 2 signals are close in time, one ALCOR chip/lane could have one extra frame slipping inside the FPGA memory



small offset in frame transmission from ALCOR

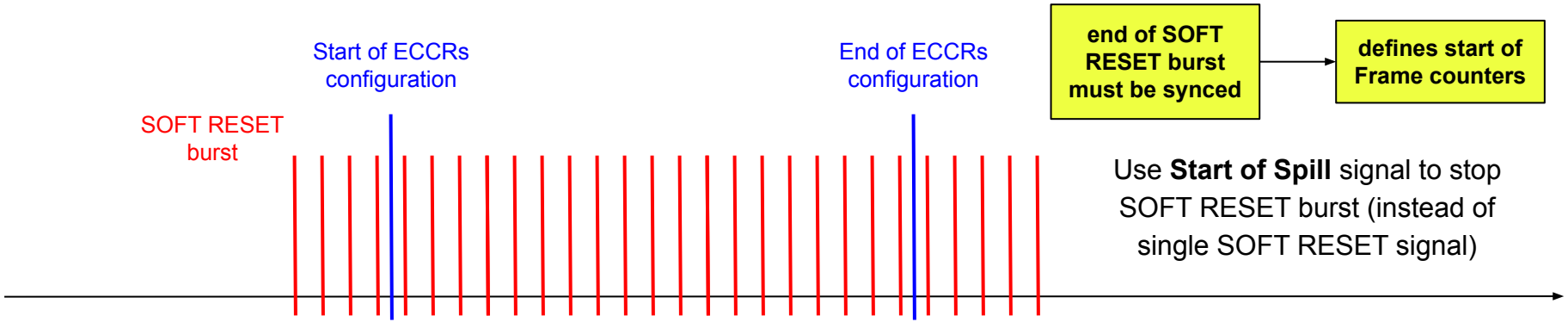
data is still synched wrt SOFT RESET



small offset in data acquisition window opening from FPGA

How to solve misalignment

- 🤨 Separate **synced SOFT RESET** from **START OF SPILL** → should avoid small timing offsets
- 😟 Generate **frames inside FPGA**, replacing ALCOR frames → debug orphan frame at the start
- 😐 Acquire **1 test-pulse** to **sync frames** of all lanes and chips → correct frame offset offline should be ok
- 🌝 Send SOFT RESET burst during ECCR configuration to keep all frame counters to 0
  - ➢ frame period = 102.4 μs → SOFT RESET period = 50 μs < frame period



Be aware of reset glitch!!!