



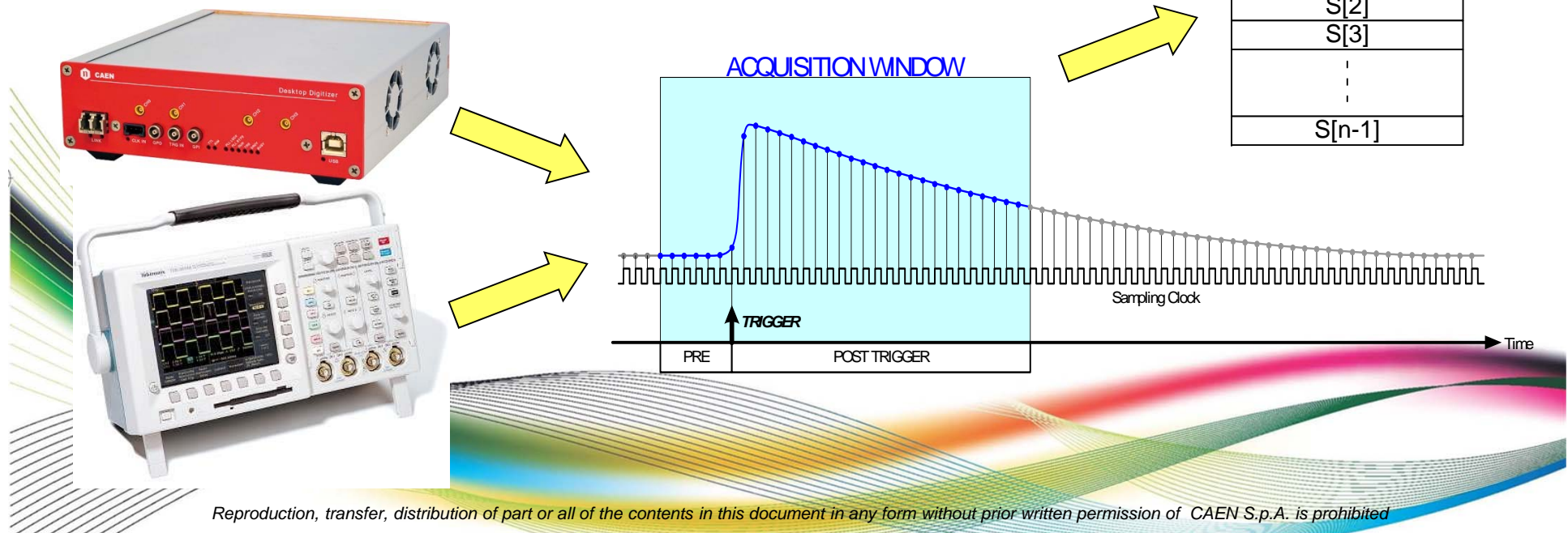
Digital Pulse Processing For Physics Applications

May 29th 2012, Vulcano

Giuliano Mini

Digitizers vs Oscilloscopes

- The principle of operation of a waveform digitizer is the same as the digital oscilloscope: when the trigger occurs, a certain number of samples (acquisition window) is saved into one memory buffer
- However, there are important differences:
 - no dead-time between triggers (Multi Event Memory)
 - multi-board synchronization for system scalability
 - high bandwidth data readout links
 - on-line data processing (FPGA or DSP)



CAEN Digitizers Highlights

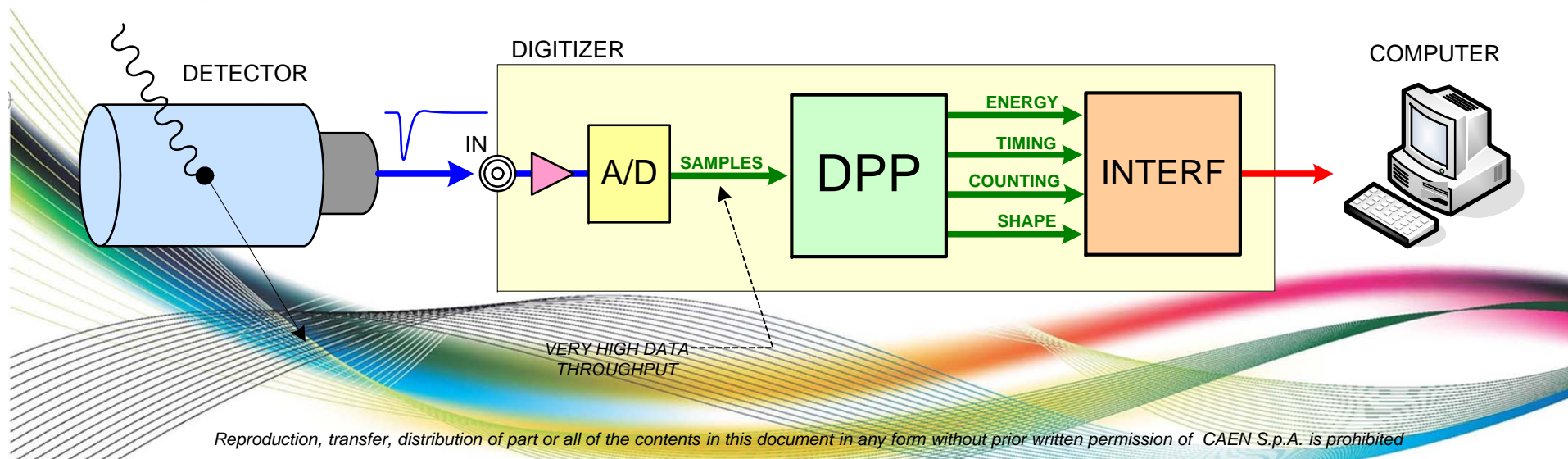


- VME, NIM, Desktop form factors
- VME64X, Optical Link (CONET), USB 2.0
- Memory buffer: up to 10MB/ch (max. 1024 events)
- Multi-board synchronization and trigger distribution
- Programmable PLL for clock synthesis
- Programmable digital I/Os
- Analog output with majority or linear sum
- FPGA firmware for Digital Pulse Processing
- Software for Windows and Linux

- **From 2 to 64 channels**
- **Up to 5 GS/s sampling rate - Up to 14 bit**
- **FPGA firmware for Digital Pulse Processing**

Benefits of the digital approach

- One single board can do the job of several analog modules
- Full information preserved: *A/D conversion as early as possible, data reduction as late as possible*
- Reduction in size, cabling, power consumption and cost per channel
- High reliability and reproducibility
- Flexibility (different digital algorithms can be designed and loaded at any time into the same hardware)



Raw waveform mode: Limits

- Using digitizers as **waveform recorders** can produce a large amount of data to be transferred from the acquisition board to a mass storage devices
- The **data throughput** can be extremely high: it may be no possible to transfer raw data to computers and make the analysis off-line!
- **On-line Digital Pulse Processing** is needed to extract only the information of interest reducing the data throughput
- The aim of the DPP is to provide FPGA algorithms able to make in digital the same functions of analog modules such as Shaping Amplifiers, Discriminators, QDCs, etc.
- Three main DPP firmware have been developed so far:
 - DPP-PHA (Pulse Height Analysis)**
 - DPP-CI (Charge Integration)**
 - DPP-PSD (Pulse Shape Discrimination)**

Acquisition mode: raw waveform vs DPP

STD FW

Acquisition Window

INPUT

Trigger

Threshold

S1
S2
S3
S4
S5
S6
S7
...
Sn

Typ. Nsample > 1K

DPP FW

Leading Edge

INPUT

TRAPEZ

HEIGHT

SAMPLES

SUM

CHARGE

MEAN

BASELINE

TIMING FILTER

Trigger

ZCROSS

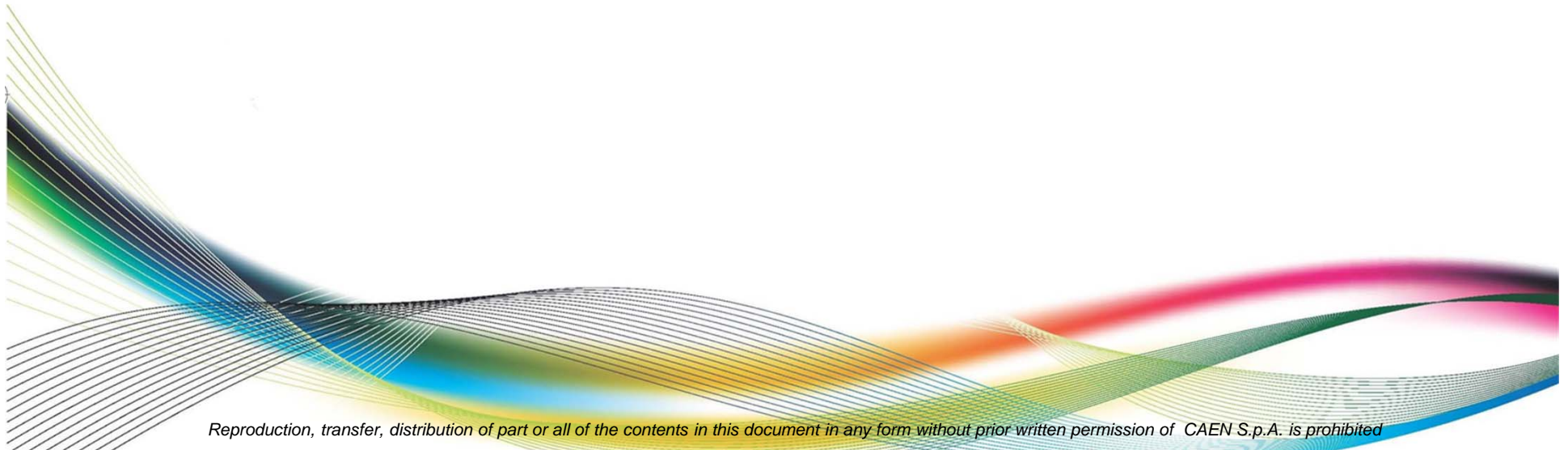
TIME STAMP

Threshold

TIME STAMP
CHARGE
BASELINE
HEIGHT
S1
S2
S3
S4

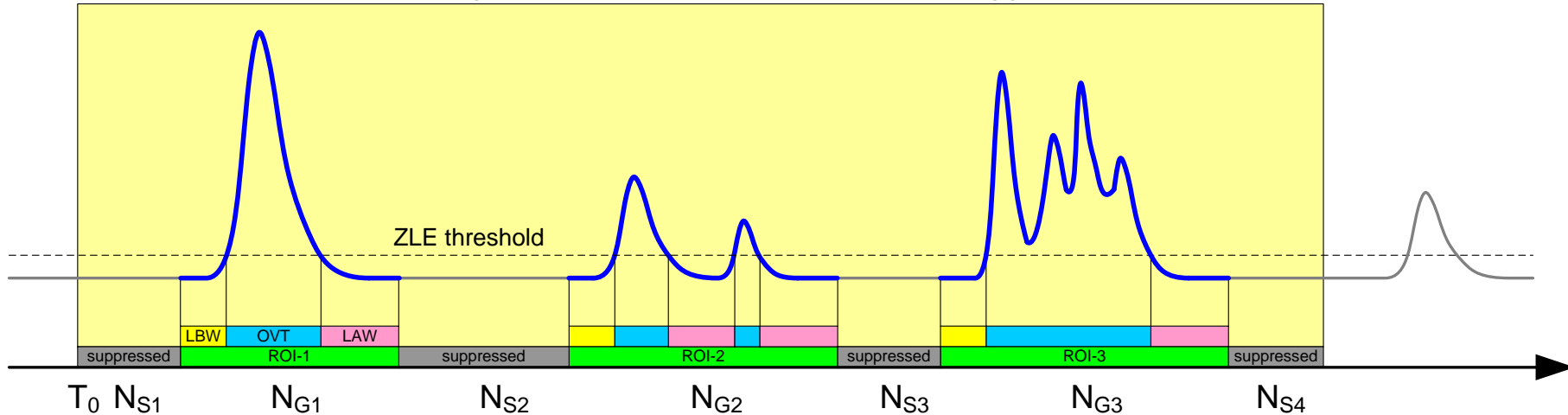
Typ. Nsample < 100

ZERO SUPPRESSION



- The zero suppression (**Zero Length Encoding**) in a waveform digitizer consists in removing from the acquisition window the parts or the waveform that don't contain useful information
- DPP only used for the **pulse identification** (Region Of Interest) and not to extract relevant quantities from the waveforms
- Typically used in beam experiments where the trigger is common to all channels, but only few of them contains events
- Available in the standard firmware of the x724, x720, x721 and x731; current version of the ZLE suffers from a readout bandwidth reduction
- A new ZLE algorithm that guarantees the best readout performances is under development for the x720 and x751

Acquisition Window (programmable size with pre and post trigger)



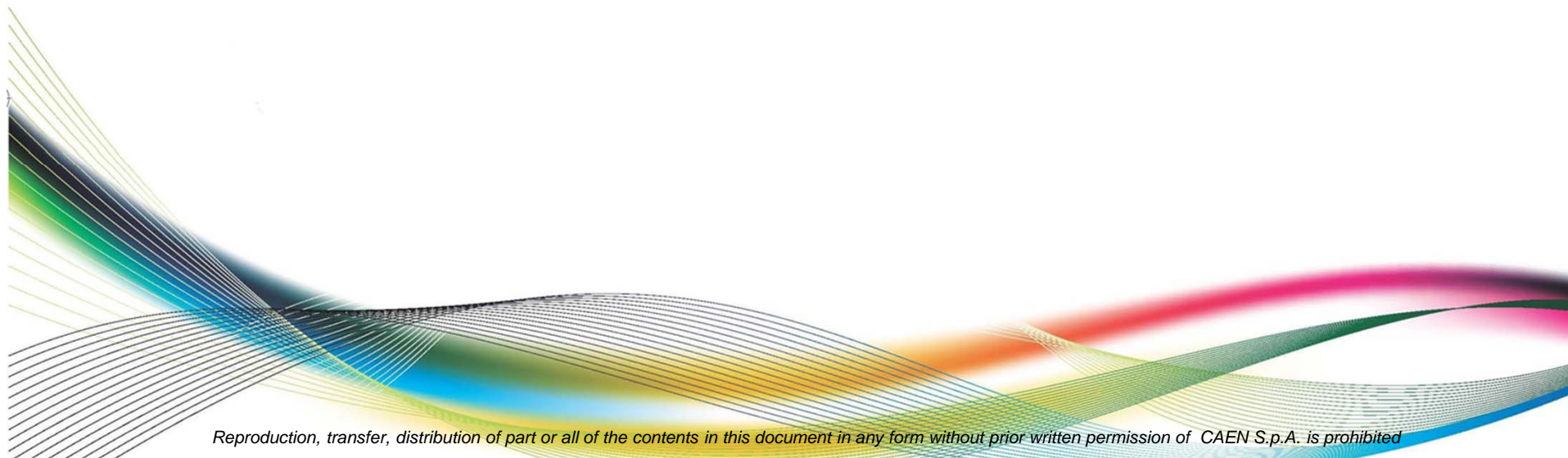
- LBW **Look Back Window:** programmable size
- OVT **OverThreshold:** lasts as long as the signal is over threshold
- LAW **Look Ahead Window:** programmable size; can be retriggered

- T_0 Time Stamp of the first sample of the Acquisition Window
- N_S Number of skipped samples belonging to the suppressed region
- N_G Number of good samples belonging to the ROI

Readout Data

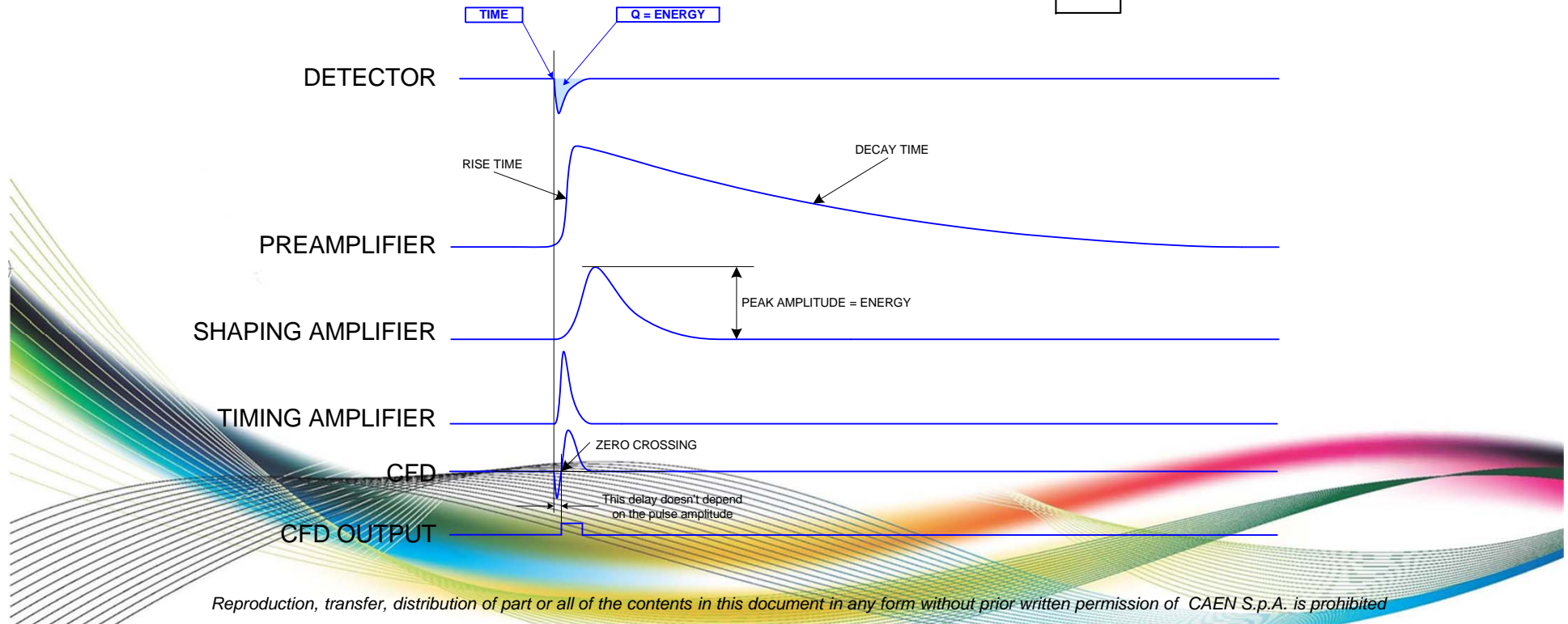
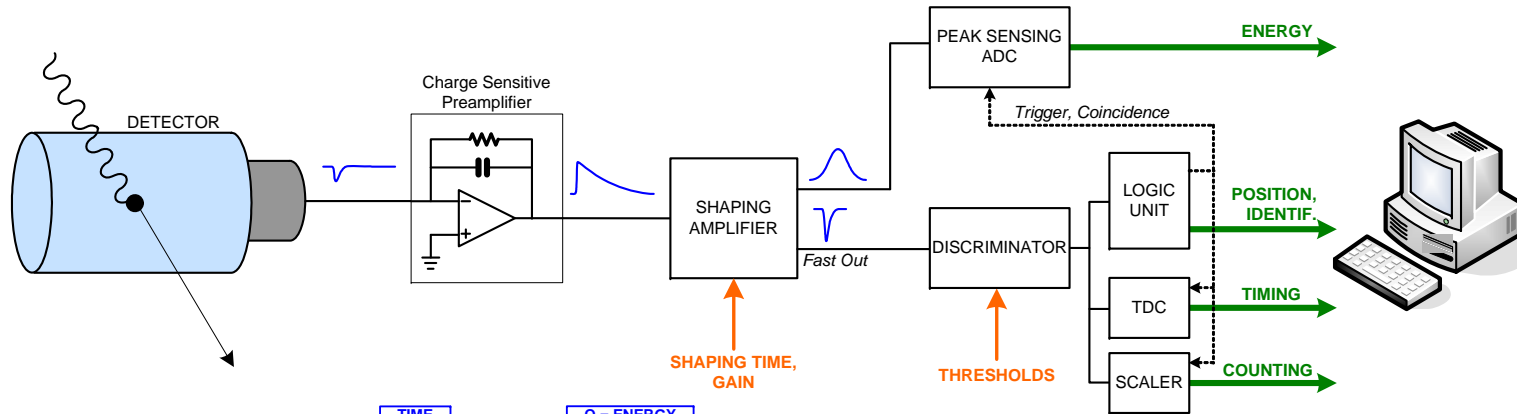
T0
NS1
NG1
samples of ROI-1
NS2
NG2
samples of ROI-2
NS3
NG3
samples of ROI-3
NS4

DPP-PHA PULSE HEIGHT ANALYSIS



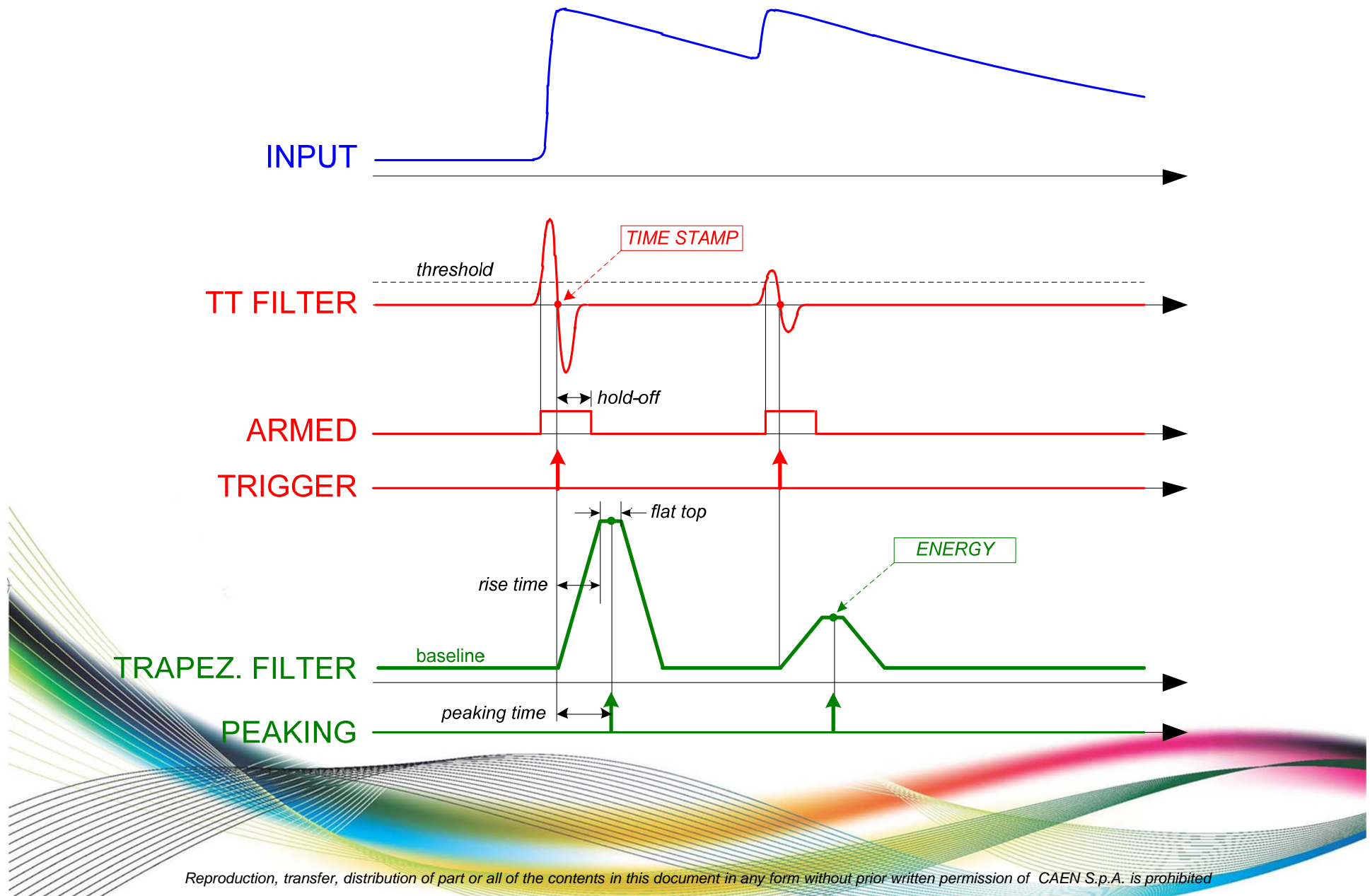
Traditional chain: example 1

charge sensitive preamplifiers



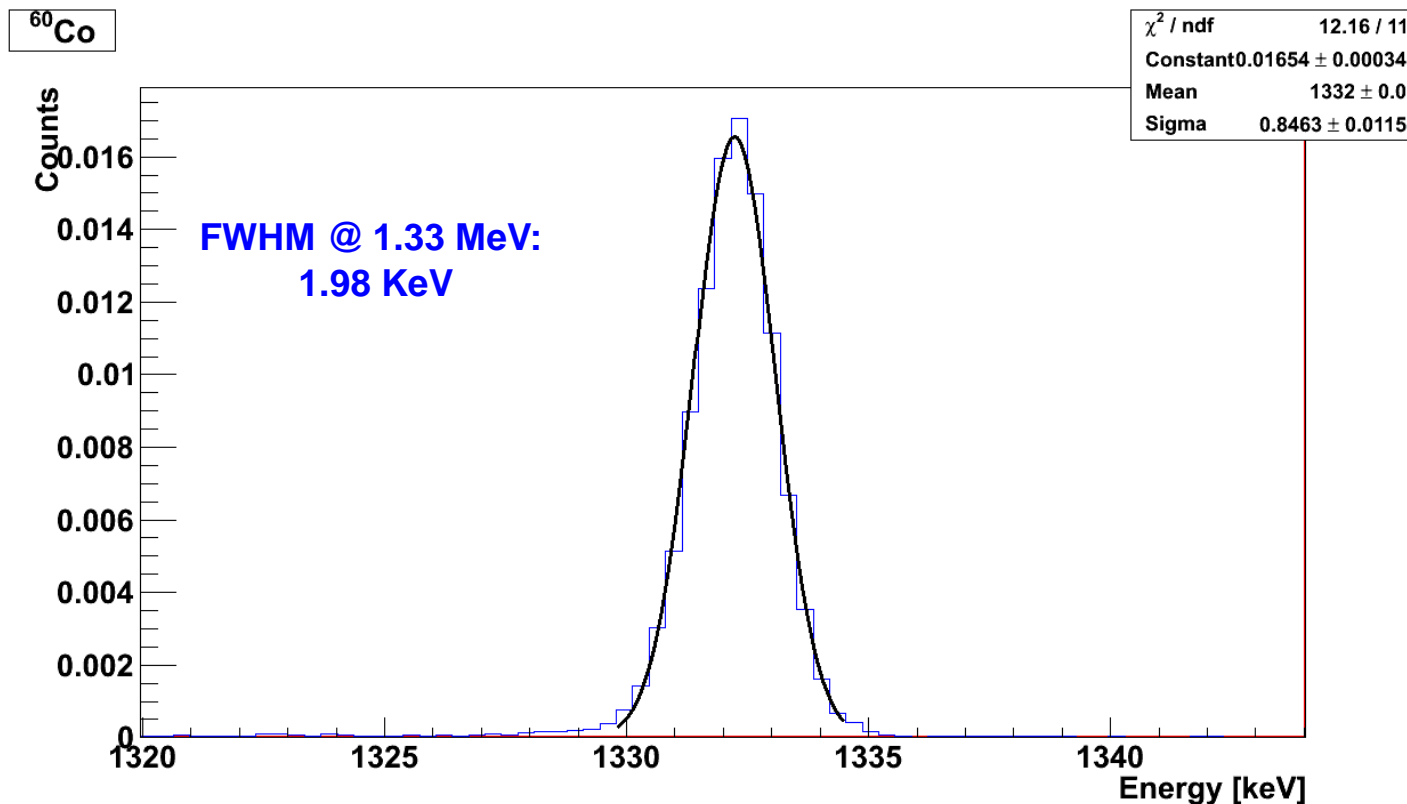
DPP for Pulse Height Analysis (DPP-PHA)

- **Digital** implementation of the **shaping amplifier + peak sensing ADC** (Multi-Channel Analyzer)
- Charge Sensitive Preamplifier directly connected to the digitizer
- Implemented in the **14 bit, 100MSps digitizers** (mod. 724)
- Provides **Pulse Height, Time Stamp** (10ns) and optionally raw data
- Pile-up rejection, Baseline restoration, ballistic deficit correction
- Low dead time => **high counting rate** (up to 1Mcps)
- Best suited for high resolution spectroscopy (HPGe and Si detectors)
- Also suitable for homeland security and biomedical applications
- Can work with segmented detectors (synchronizations, coincidences and neighbour triggering)

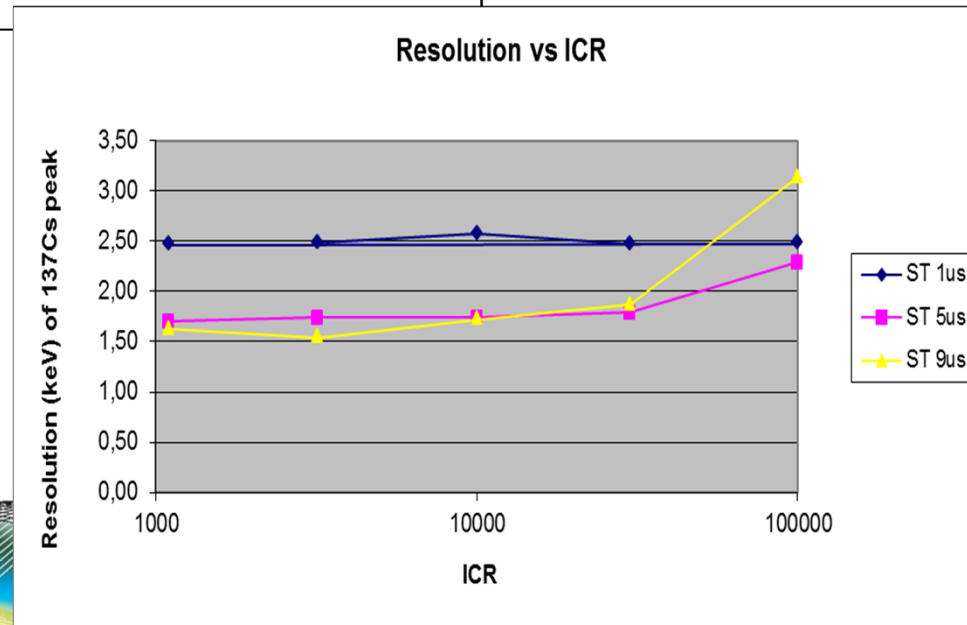
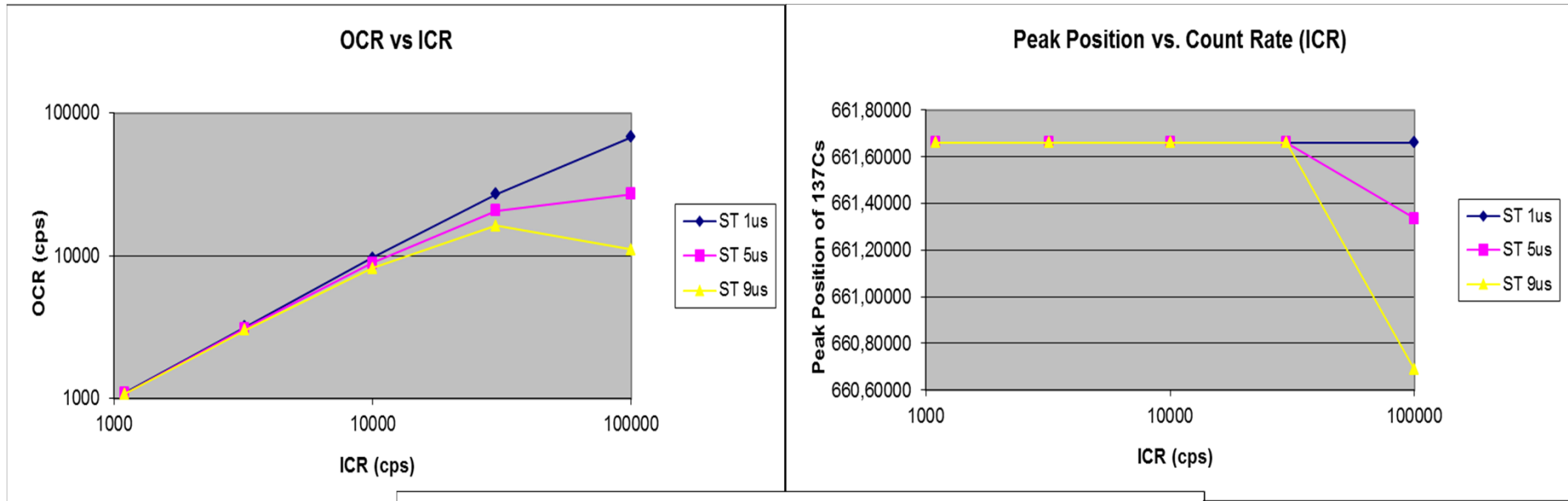


Test Results with HPGe detectors

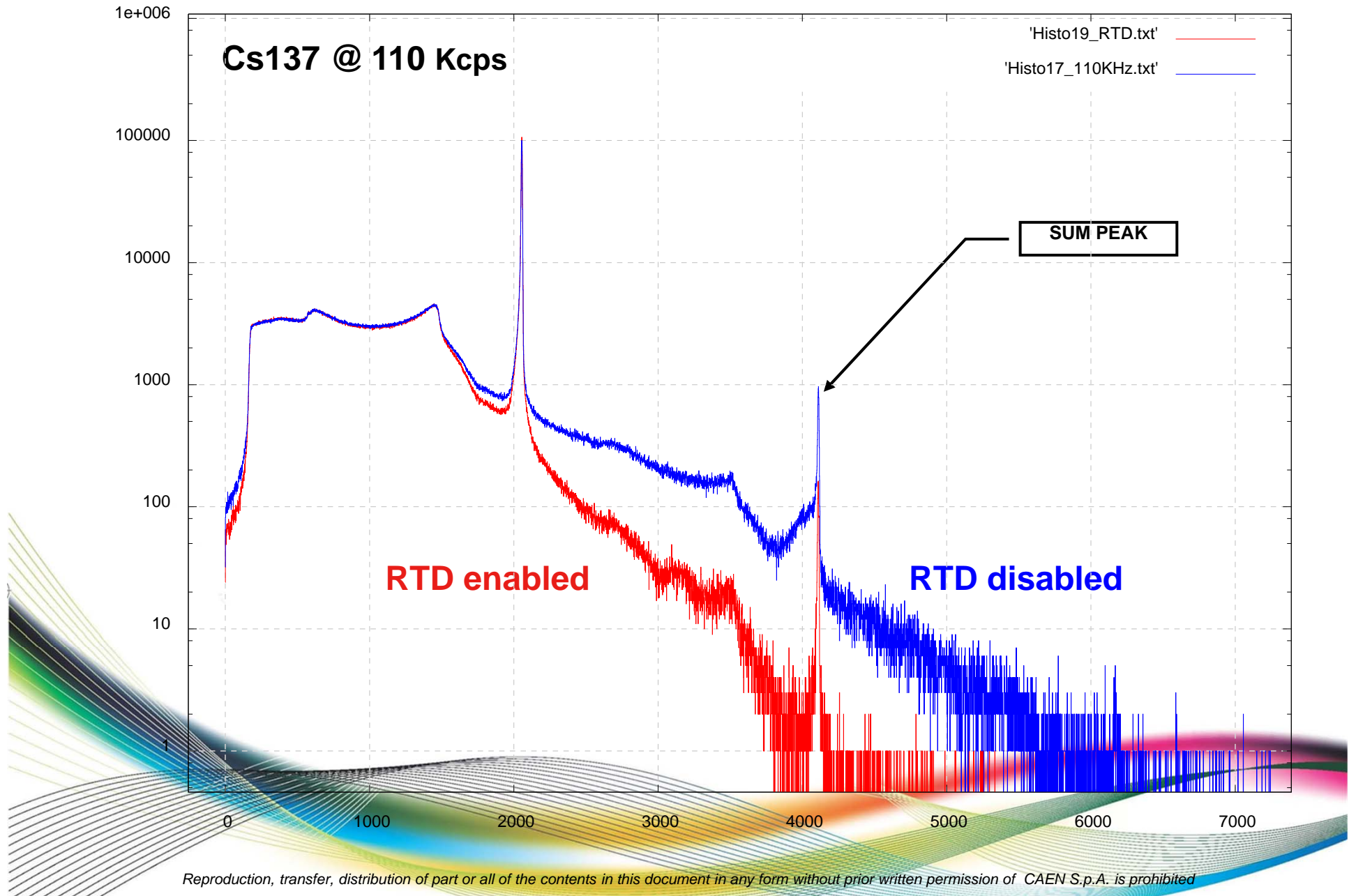
- Preliminary tests performed at LNL (Legnaro - Italy) on Nov-2008 and Feb-2009
- Duke University on Jul-2010
- University of Palermo (Dep. Of Phisycs) on Jan 2011. Detector: Ortec HP-Ge mod. GEM40P4 cooled with an X-cooler (Peltier). Preamp: A257P (time constant = 100 μ s).
- Saclay (France), lab of radiochemistry on March 2011. Different types of detectors and sources.



Test Results with HPGe (II)



Test Results with HPGe (III)

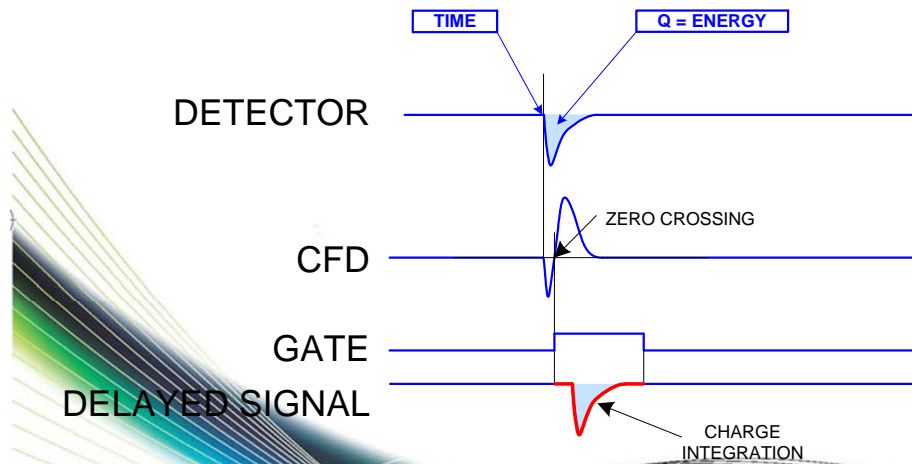
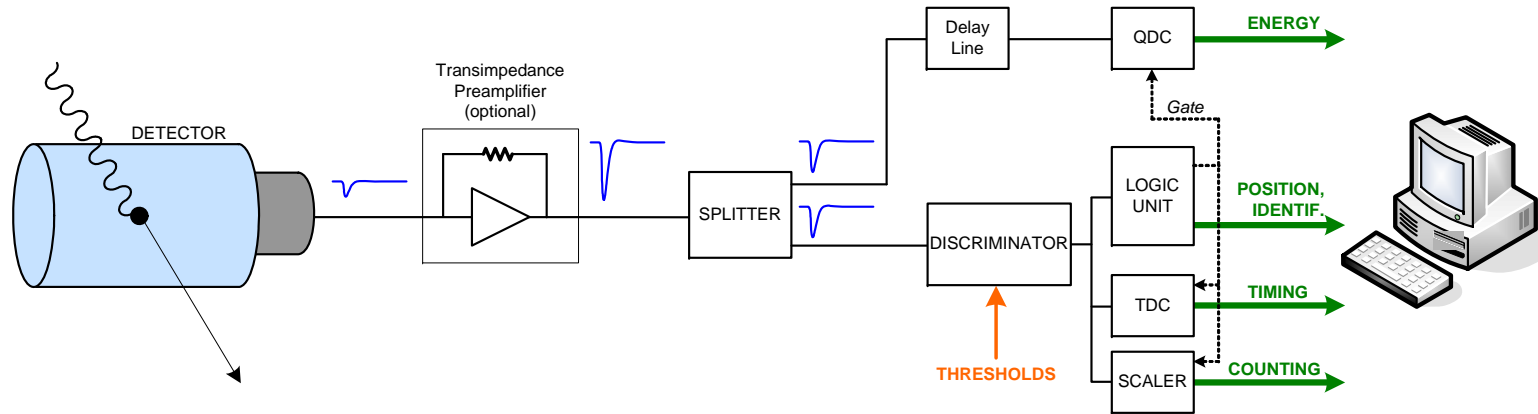


DPP-CI

DIGITAL CHARGE INTEGRATION

Traditional chain: example 2

trans-impedance (current sensitive) preamplifier

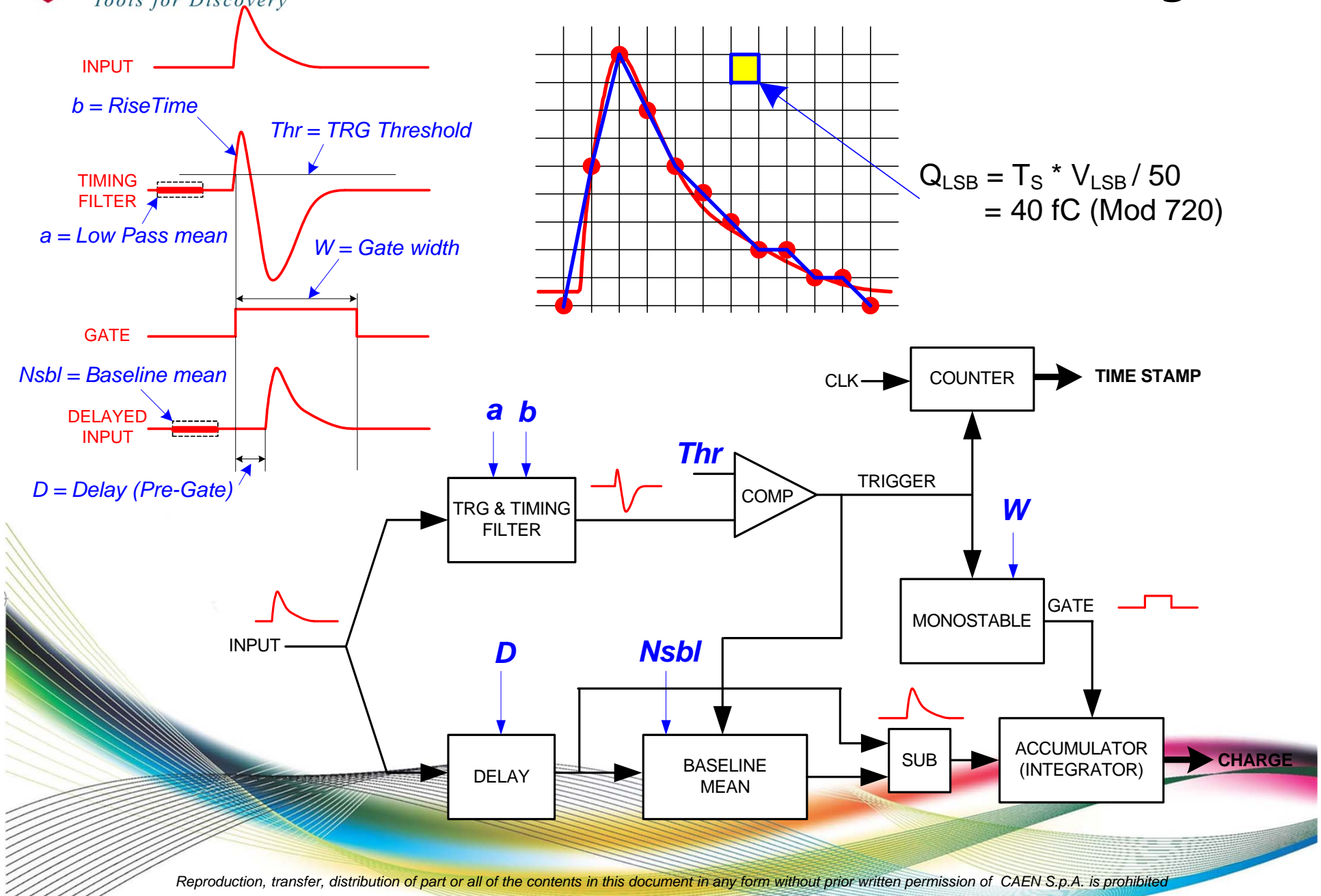


- The QDC is not self-triggering; need a gate generator
- need delay lines to compensate the delay of the gate logic

DPP for the Charge Integration (DPP-CI)

- **Digital** implementation of the **QDC + discriminator and gate generator**
- Implemented in the Mod. x720 - 12 bit, 250MS/s
- **Self-gating** integration; no delay line to fit the pulse within the gate
- Baseline restoration (pedestal cancellation)
- Extremely high dynamic range
- Dead-timeless acquisition (**no conversion time**)
- Energy and timing information can be combined
- Typically used for PMT or SiPM/MPPC readout

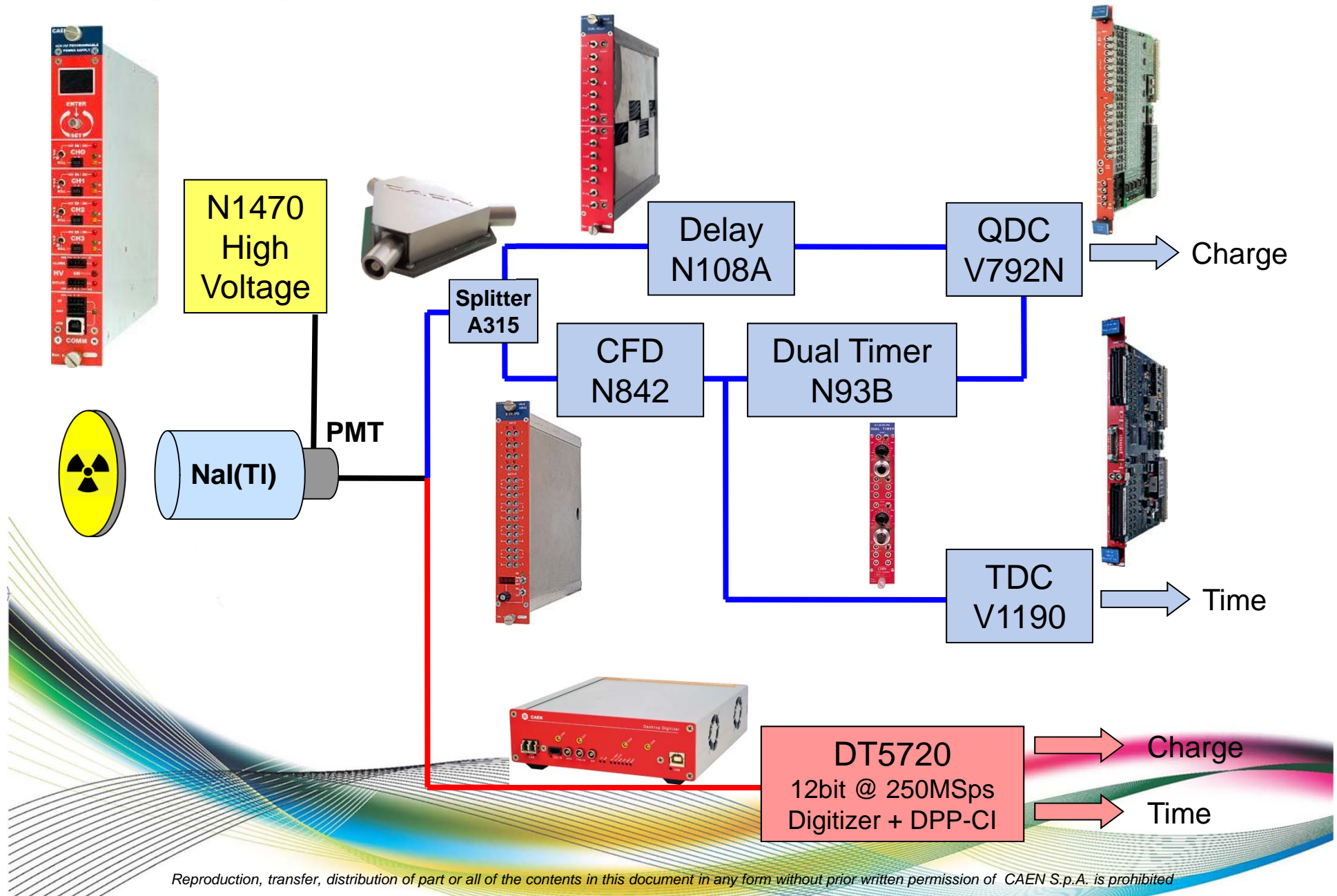
DPP-CI Block Diagram



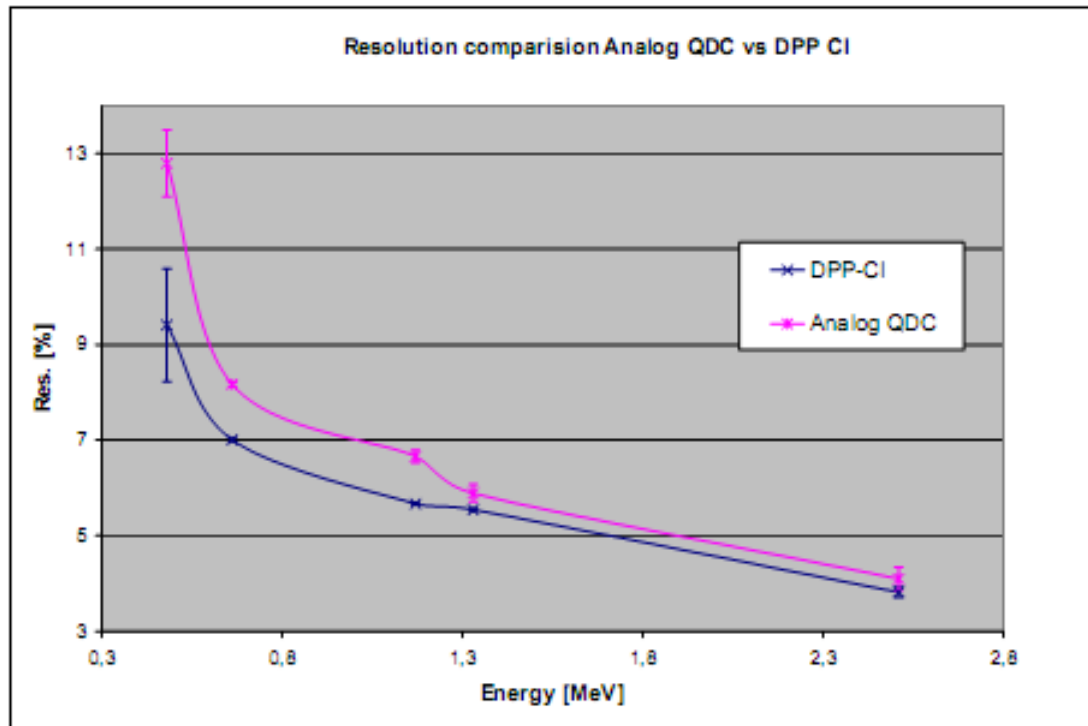
$$Q_{LSB} = T_S * V_{LSB} / 50$$

$$= 40 \text{ fC (Mod 720)}$$

DPP-CI / Analog Chain set-ups



DPP-CI: Test Results



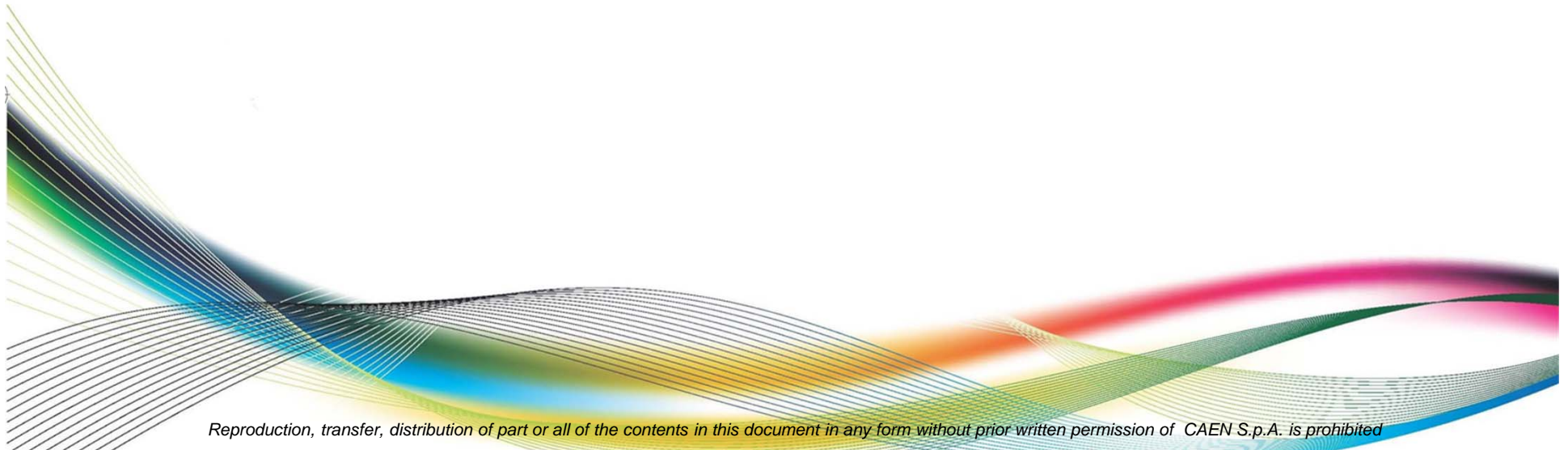
NaI detector and PMT directly connected to the QDC or digitizer

	<i>DPP-CI</i>	<i>Analog QDC</i>
Energy (MeV)	Res (%)	Res (%)
0.481 (¹³⁷ Cs Compton edge)	9.41 ± 1.18	12.80 ± 0.70
0.662 (¹³⁷ Cs Photopeak)	7.01 ± 0.04	8.17 ± 0.04
1.33 (⁶⁰ Co Photopeak)	5.67 ± 0.03	6.66 ± 0.18
1.17 (⁶⁰ Co Photopeak)	5.46 ± 0.02	5.89 ± 0.13
2.51 (⁶⁰ Co Sum peak)	3.82 ± 0.11	4.10 ± 0.24

$$\text{Resolution} = \text{FWHM} * 100 / \text{Mean}$$

DPP-PSD

PULSE SHAPE DISCRIMINATION

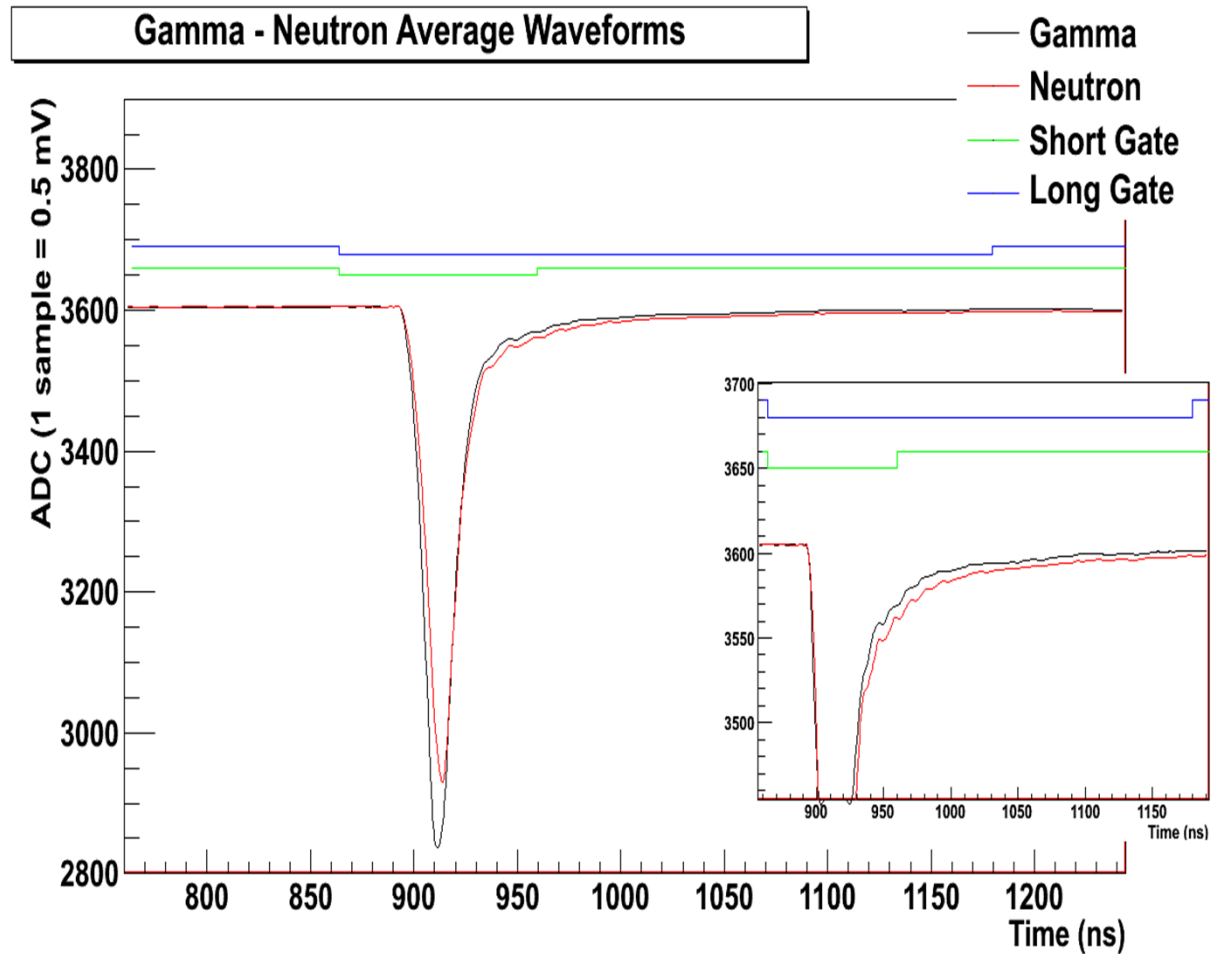


- Digital implementation of the $\Delta E/E$ analysis (**double gate charge integration**)
- Implemented in the Mod. x720 - 12 bit, 250MS/s and Mod x751 - 10 bit, 1GS/s or 2GS/s
- $PSD = (Q_{LONG} - Q_{SHORT}) / Q_{LONG}$
- Typically used with organic liquid scintillators (e.g. BC501)
- Dead-timeless acquisition (**no conversion time**)
- Alternative analysis (not implemented yet) based on the Rise Time Discrimination technique: ΔT in the Zero Crossing of two CFDs at 25% and 75%; applied to integrated output (either from C.S. preamp or digital integrator)

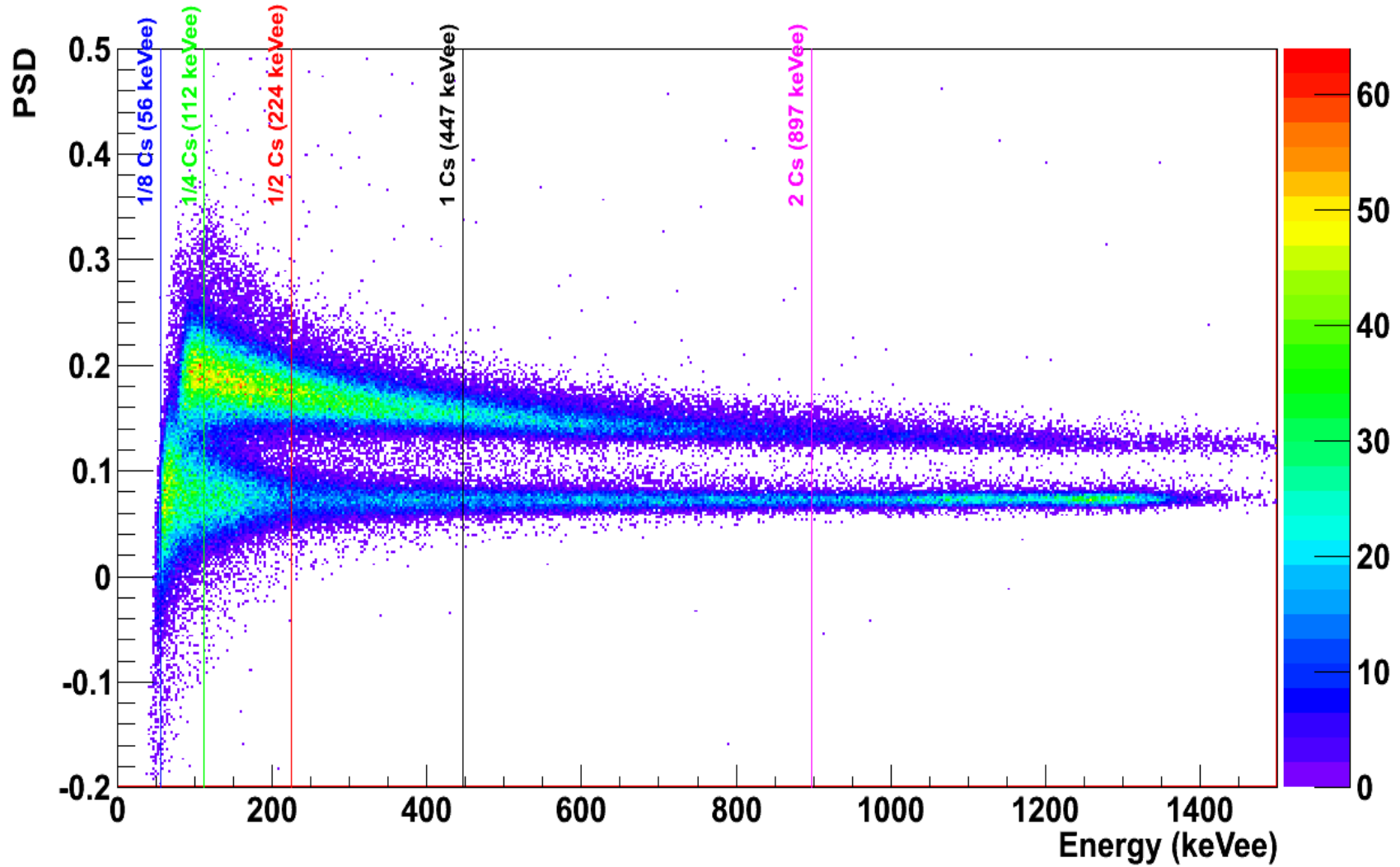
γ -n Discrimination: test results (I)

Detector: BC501A 5x2 inches,

PMT: Hamamatsu R1250

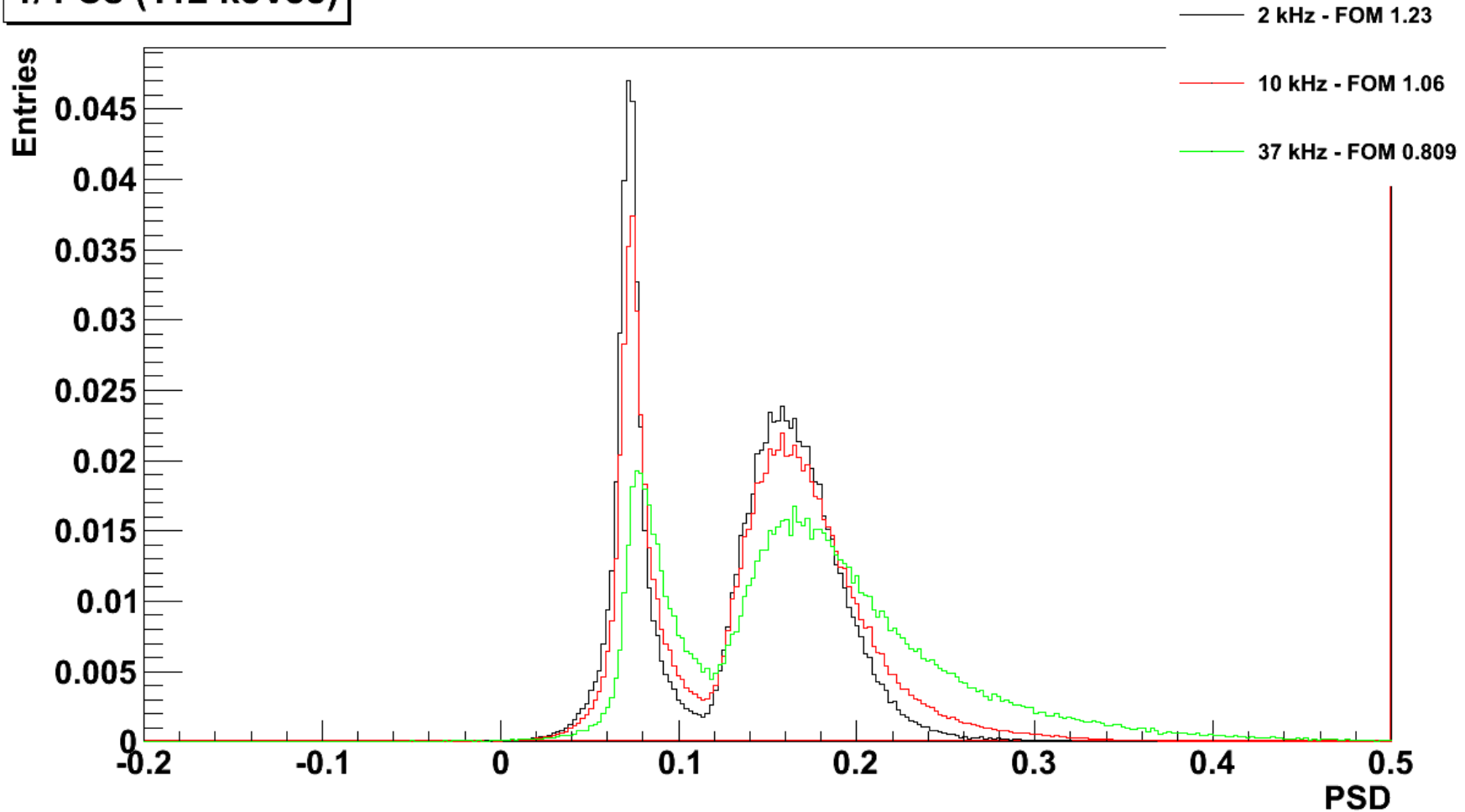


γ -n Discrimination: test results (II)

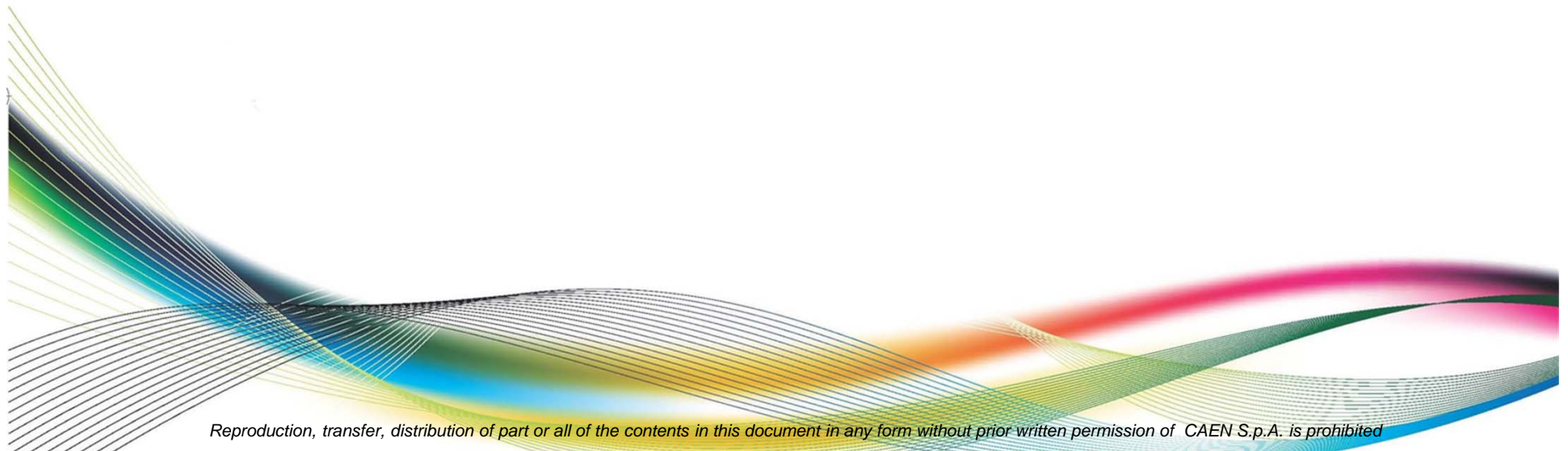


γ -n Discrimination: test results (IV)

1/4 Cs (112 keVee)



Some Real Applications



What does *synchronization* mean?

1. same sampling clock propagated to all flash ADCs:
 - ✓ External clock in/out⁽¹⁾; first board can act as a clock master and distributes the clock to many slaves in daisy chain
 - ✓ PLL for clock synthesis; lock to an external clock reference
 - ✓ Programmable Phase Adjust for cable delay compensation

2. same T zero for the time stamps:
 - ✓ Sync Input for a simultaneous start/stop of the acquisition and/or for time stamp reset
 - ✓ Sync Distribution through the boards in daisy-chain (via TrgOut)
 - ✓ Use of the first trigger to start the acquisition

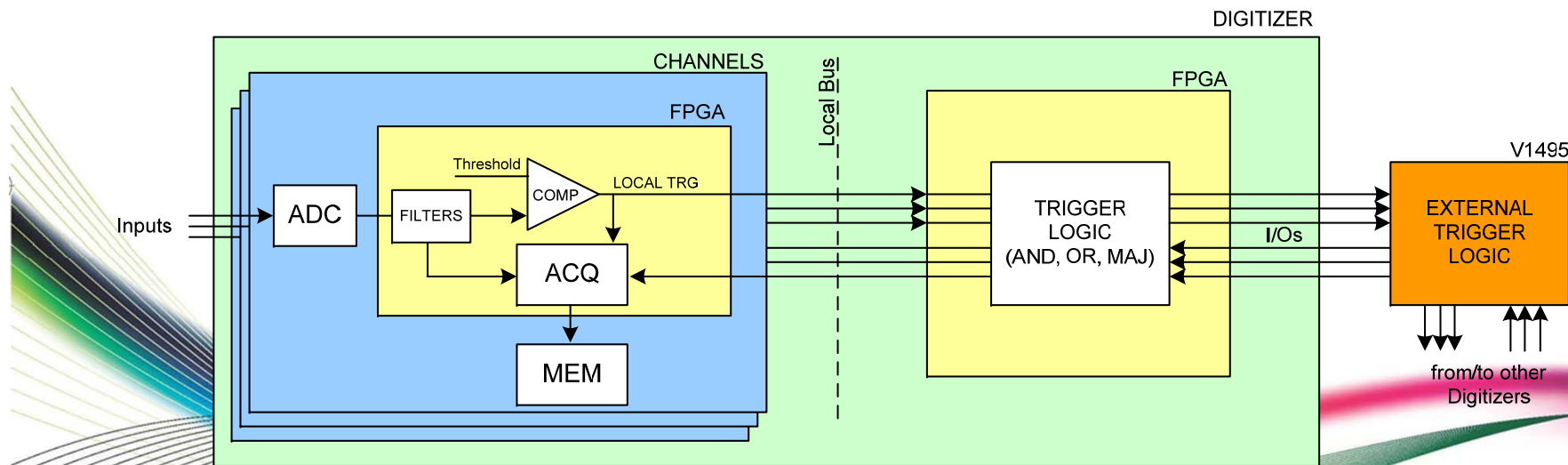
3. trigger propagation and correlation:
 - ✓ External Trigger In/Out (NIM/TLL on LEMO connectors)
 - ✓ Global or individual Trigger propagation through LVDS GPIOs⁽¹⁾
 - ✓ Neighbour triggering options for segmented and clove detectors

(1) for VME modules only

CAEN Coincidence and Event correlation (HW) *Tools for Discovery*

Hardware approach

- Propagate local triggers from each channel to the others within the board
- TR-TV mode: triggers from other channels (trigger requests) can be used as trigger validation
- Apply individual trigger masks and simple combinatorial logics on board (AND, OR, Majority)
- Use GPIOs on the front panel to propagate individual trigger inputs/outputs from/to external logic boards (e.g. V1495)

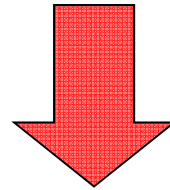


Software approach

- Read all events as long as you have enough bandwidth (i.e. make data suppression as late as you can): **preserve the information!**
- In list mode, the bandwidth requirement is very low (e.g. 8 bytes per event). Example: 8 channels at 100 KHz trigger rate gives 6.4 MB/s.
- In a modern multi-core computers, the readout process takes a small fraction of the CPU resources
- Time stamped events allow for easy and flexible software coincidence, anticoincidence, correlation, etc.

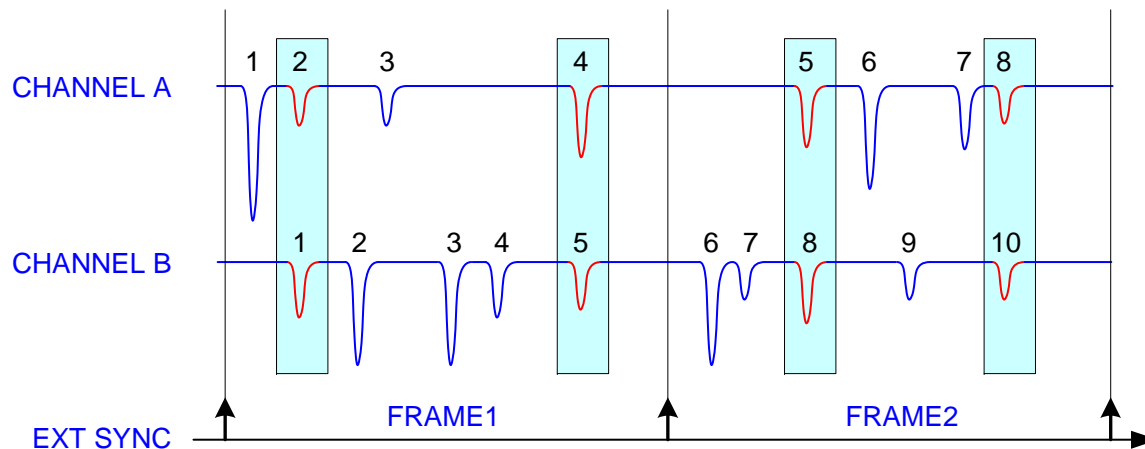
Time Frame Spectroscopic Imaging (I)

Need to get subsequent **spectroscopic images of a sample**
(1024 frames)



- For each frame multichannel spectra collection with coincidence capabilities is required
- Once a frame has been acquired, the system has to save the spectra, reset the histos and get ready to restart the measurement with **no dead time between frames**
- The frame change is **synchronous** with an external signal

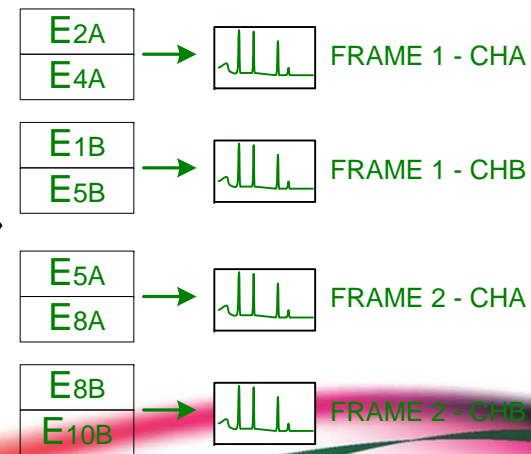
- On-board DPP-PHA processes the input pulses and produces a list of events (Energy & Timestamp)
- The DAQ software looks for coincidence using the timestamps and generates histograms
- The External Sync signal forces the boards to produce a "End of Frame" marker in the data list
- The DAQ software recognizes the marker and closes the current frame opening the next one



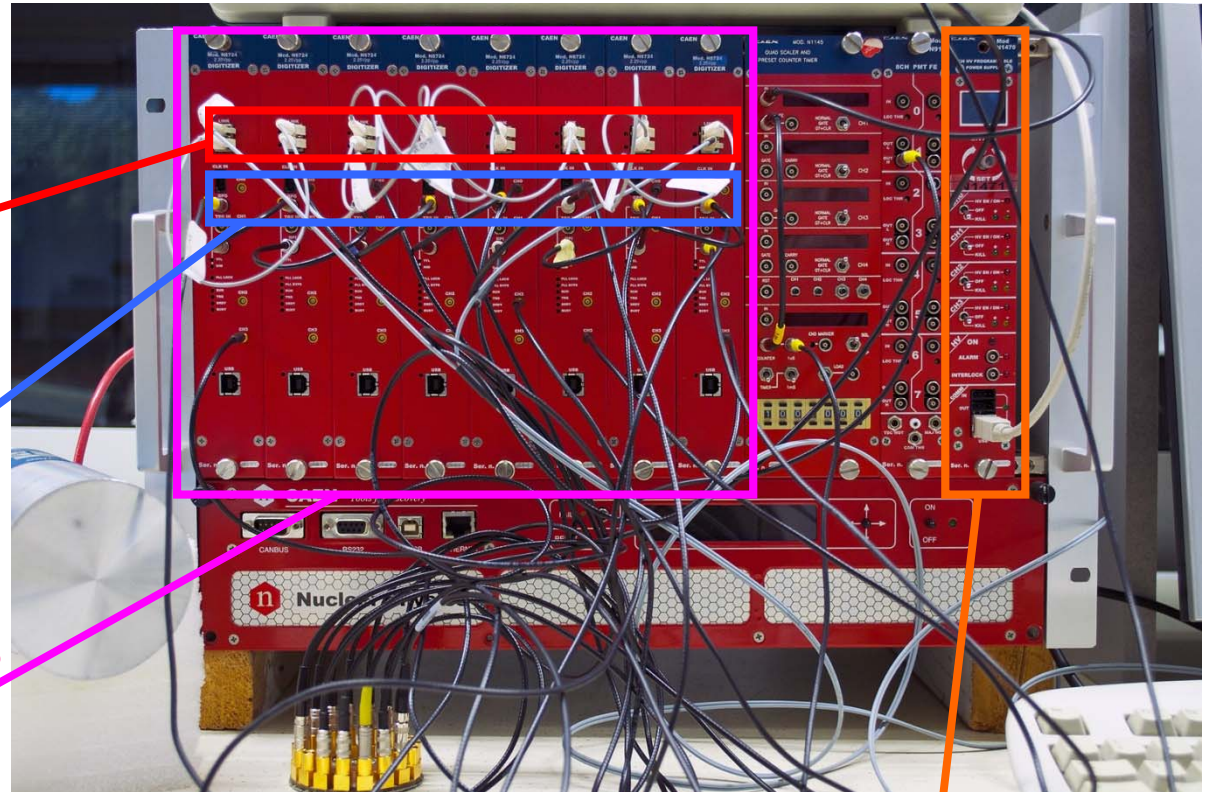
DPP-PHA

LIST - A		LIST - B	
T1A	E1A	T1B	E1B
T2A	E2A	T2B	E2B
T3A	E3A	T3B	E3B
T4A	E4A	T4B	E4B
EOF Marker		T5B	E5B
T5A	E5A	EOF Marker	
T6A	E6A	T6B	E6B
T7A	E7A	T7B	E7B
T8A	E8A	T8B	E8B
EOF Marker		T9B	E9B
		T10B	E10B
		EOF Marker	

DAQ SW



TEST SETUP

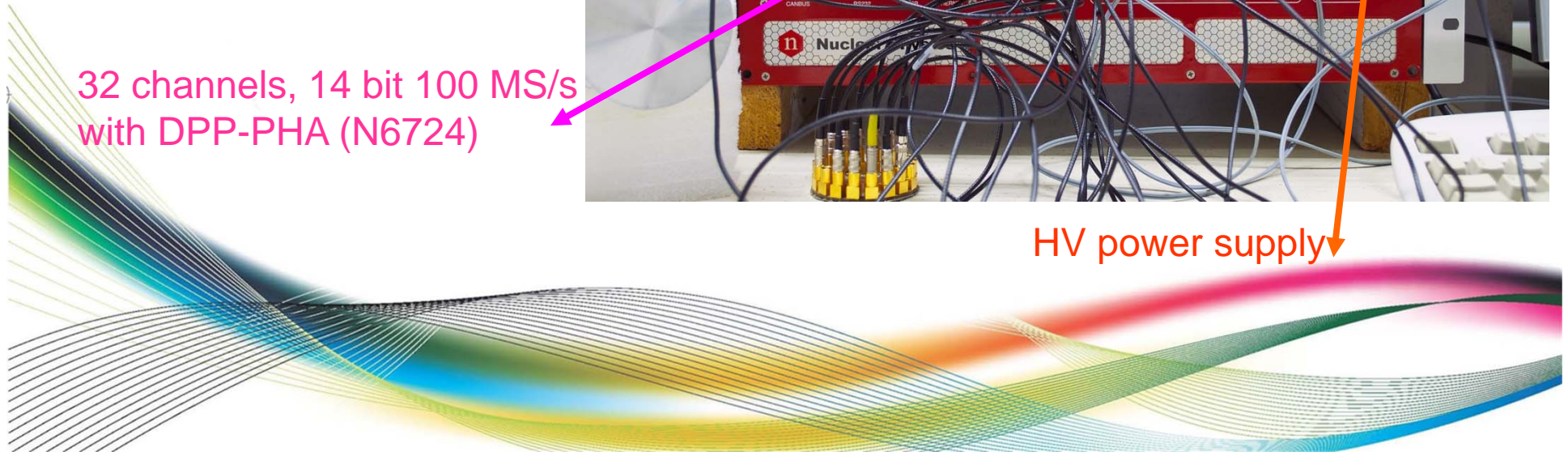


High-throughput readout via optical link (~300 kcps/ch)

Synchronous Histos collection and frame switch via daisy chain

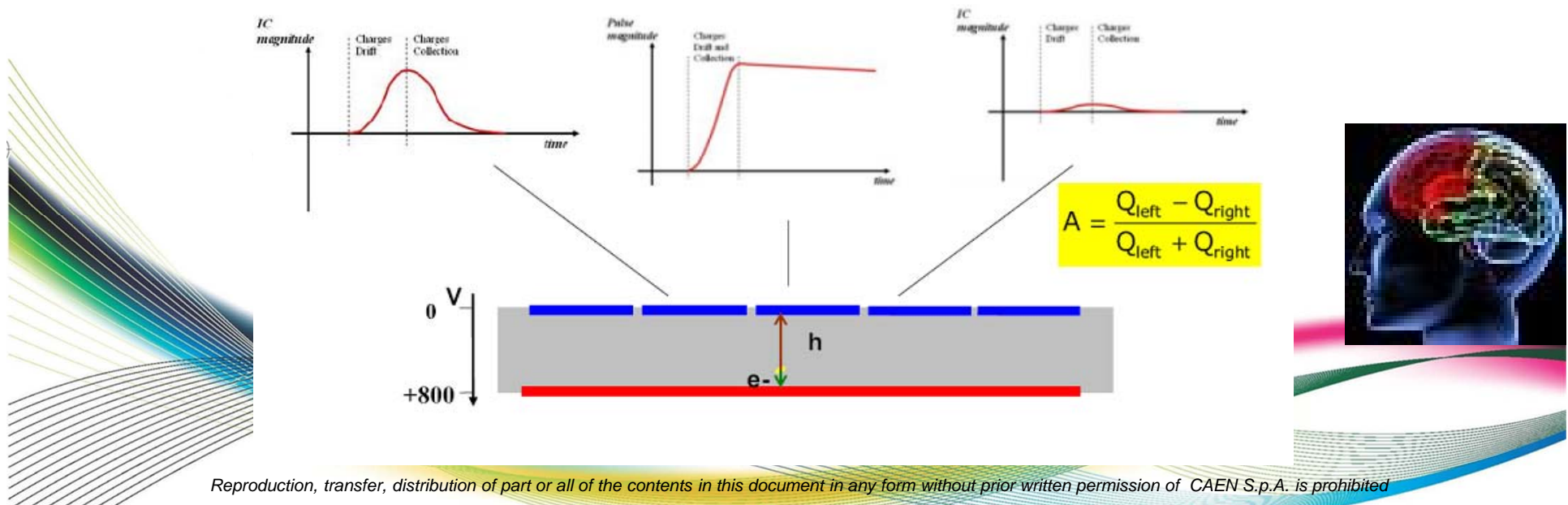
32 channels, 14 bit 100 MS/s with DPP-PHA (N6724)

HV power supply

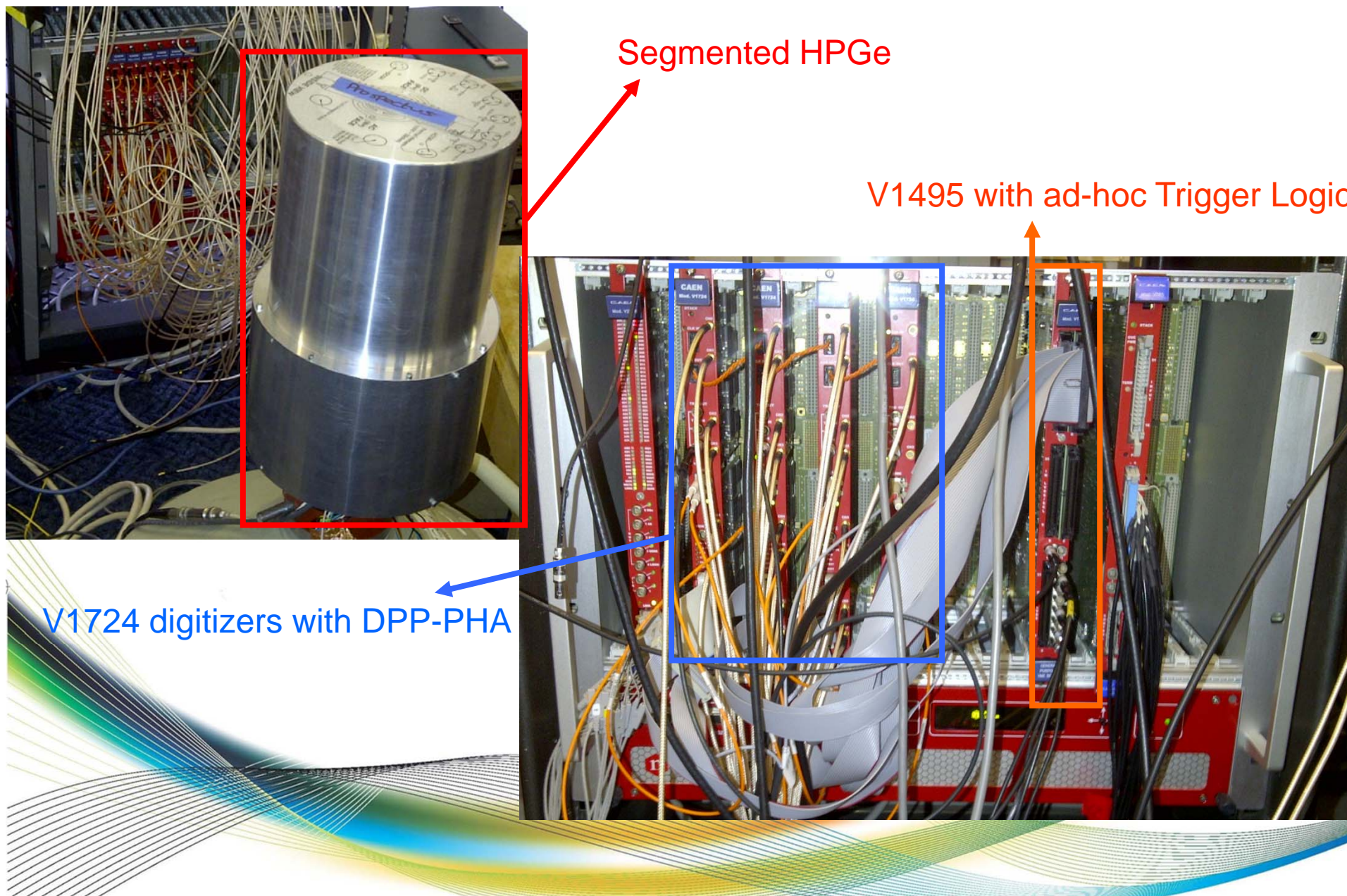


Individual inter-channel triggering (I)

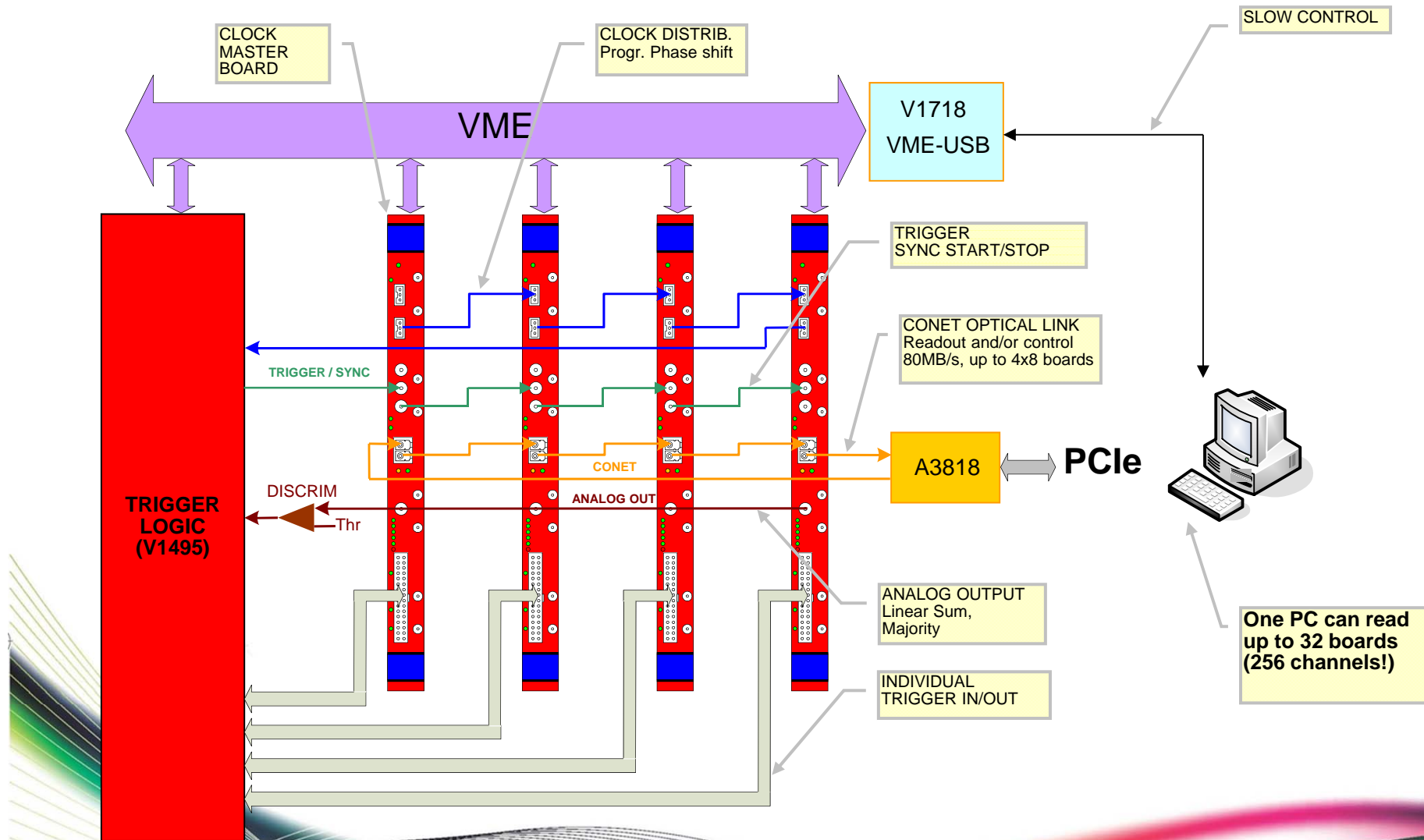
- Feature developed for the project *ProSPECTus* (Compton camera)
- Mainly needed in segmented or clove detectors
- **One channel triggers itself and also neighbour channels** (also from board to board)
- Individual TRG-IN and TRG-OUT lines from each channel to the Front Panel GPIO connector (8 inputs + 8 outputs)
- **External trigger unit** (V1495) for the coincidence matrix implementation



Individual inter-channel triggering (II)



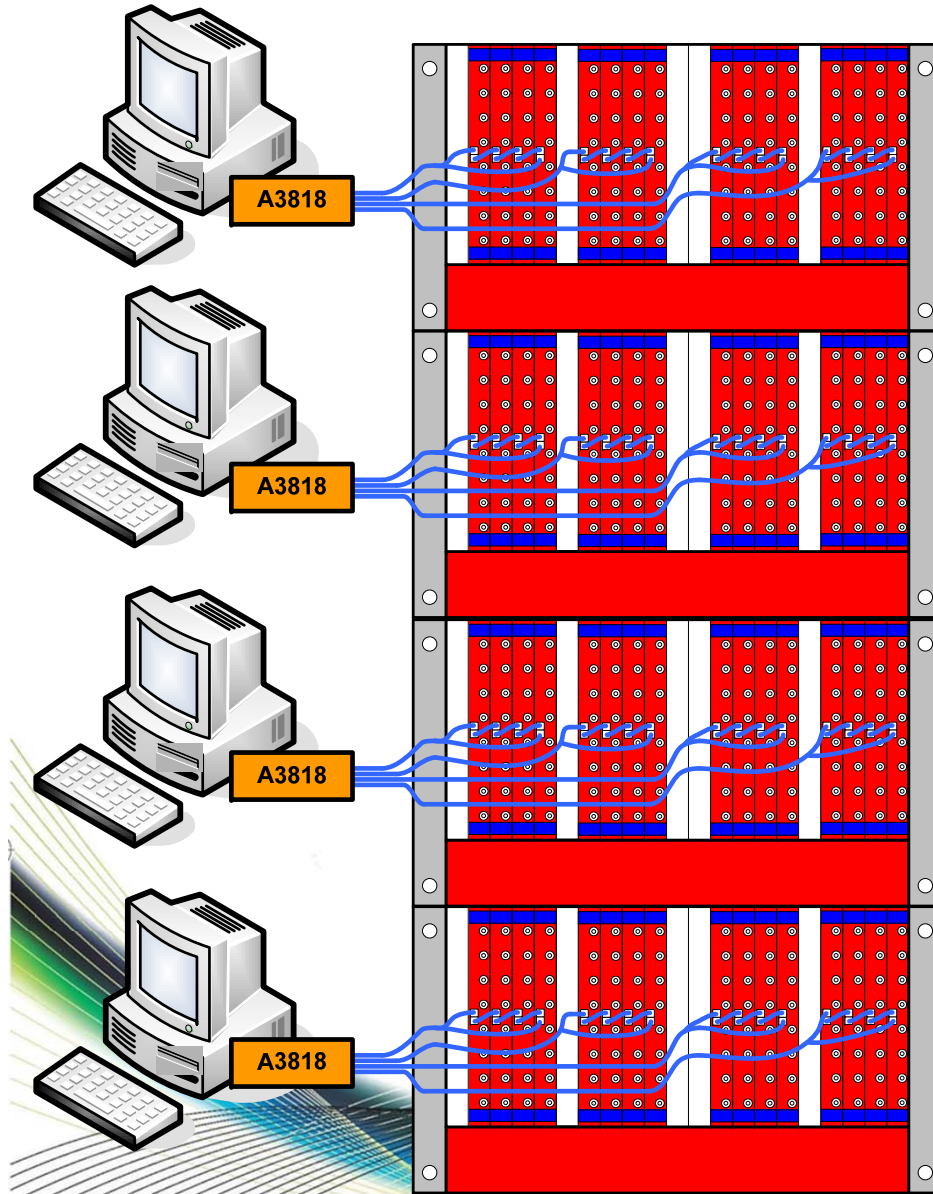
Individual inter-channel triggering(III)



Multi purpose low-background experiment with LXe.

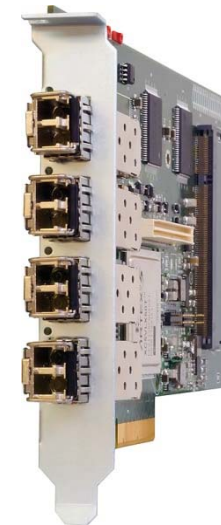
- Xenon **MASS**ive detector for Solar neutrino (pp/ ^7Be)
- Xenon neutrino **MASS** detector (double beta decay)
- Xenon detector for Weakly Interacting **MASS**ive Particles (DM)





XMASS Experiment (II)

- 80 V1751 modules in 5 VME crates
- ZLE
- 640 channels (10 bit @ 1GHz)
- 5 A3818s 4 link PCIe cards
- 20 parallel CONET links
- 4 digitizers daisy chained
- Readout Bandwidth = ~ 2 MB/s/ch
- Total aggregate throughput = ~ 1 GB/s



A3818
PCIe 8x
CONET Controller

Thank you!

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