UNIVERSITÀ DEGLI STUDI DI PADOVA

Admission to the 2nd year

Ciro Fabian Bermudez Marquez

cirofabian.bermudezmarquez@studenti.unipd.it

13 September 2024

General Information

- **Name and surname:** Ciro Fabian Bermudez Marquez
- **Cycle and A.Y:** 39th Series, 2023/2024
- **Curriculum:** Electronics
- **Tutor:** Flavio Loddo
- **Research Center:** INFN Bari
- **Topic:** Design of read-out electronics in 28 nm CMOS technology for next generation pixel detector

Agenda

- Courses and training activities
- Research topic and objectives
- Verification and HEP
- Verification Methodology
- Research activities carried out so far 1st year
- Plan for 2nd and 3rd years

Courses and training activities

Courses and training activities

Courses	Credits	Professor	Hours	Year
Front-end electronics DAQ systems for radiation detection (HE5)	1.5	Adriano Di Giovanni	20	1st
Design of readout integrated circuits for particle detectors	2.5	Flavio Loddo	20	2nd
Programmable System on Chip (SoC) for data acquisition and processing	2.5	Domizia Orestano	20	2nd
Electronic systems in high energy physics	6	Adriano Lai	48	2nd

Training activities	Dates	Place	Year
Verification with UVM for HEP Workshop	(27/02/2024 – 01/03/2024)	CERN	1st
Training Framework PixESL for simulation of pixel chip	(07/04/2024 – 12/04/2024)	CERN	1st
Cadence, System Verilog for design and verification	(07/02/2024 – 07/04/2024)	Online	1st
Synopsys, Language: System Verilog Testbench	(06/02/2024 – 06/04/2024)	Online	1st
Synopsys, Language: System Verilog Verification using UVM	(12/04/2024 – 12/06/2024)	Online	1st
Cadence, SystemC language Fundamentals	To be defined	Online	2nd
Cadence, SystemC Transaction-Level Modeling TLM2.0	To be defined	Online	2nd

Research topic and objectives

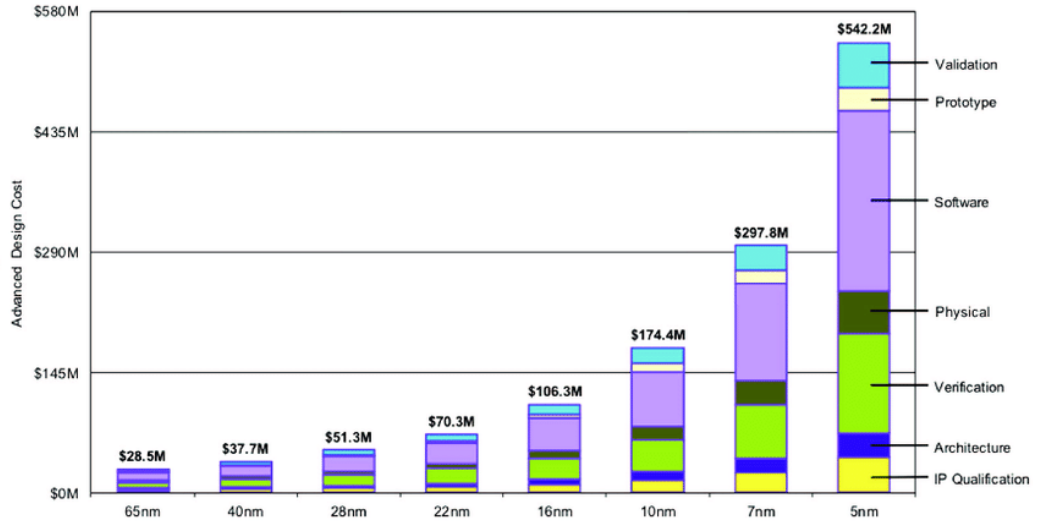
Research topic and objectives

The research focuses on the development of a UVM verification framework to prove the correctness of pixel chip design to be used in future projects in the field of High Energy Physics (HEP). Moreover, the modelling of pixel-based detectors, from front-end to back-end, at a high level of abstraction to perform architectural studies will be implemented. This will provide metrics to compare different solutions to satisfy functional and non-functional requirements, both at detector and readout chip level.

Verification and HEP

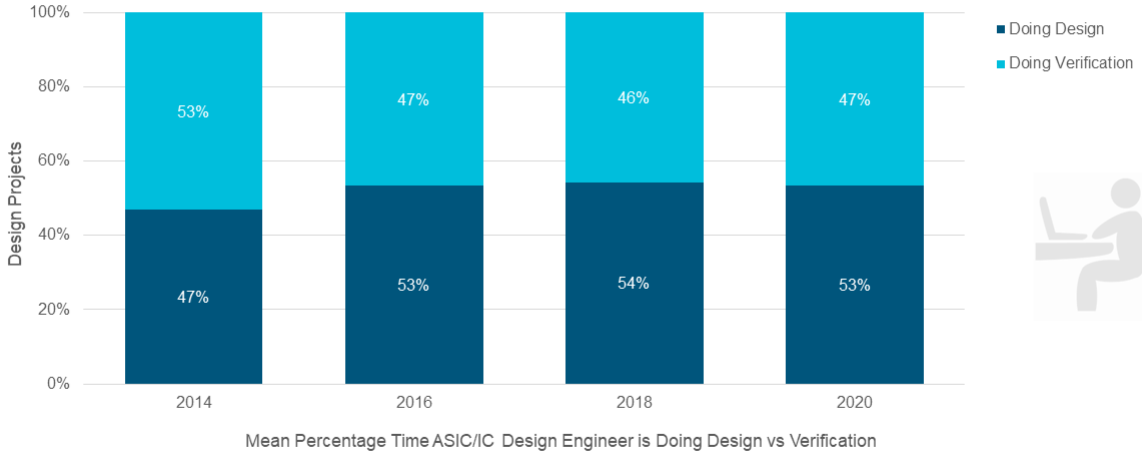
What is Verification

- **Design activity to prone correctness**
  - Verification is a resource limited quest to find as many bugs as possible before shipping.
- **Hard problem**
  - How to prove absence of bugs?
- **Bottleneck**
  - ASIC verification is more complex and time consuming than design
  - Verification is resource intensive
  - New skill in HEP community



Chip Design and Manufacturing Cost under Different Process Nodes: Data Source from IBS

Mean Time ASIC/IC Design Engineer is Doing Design vs Verification



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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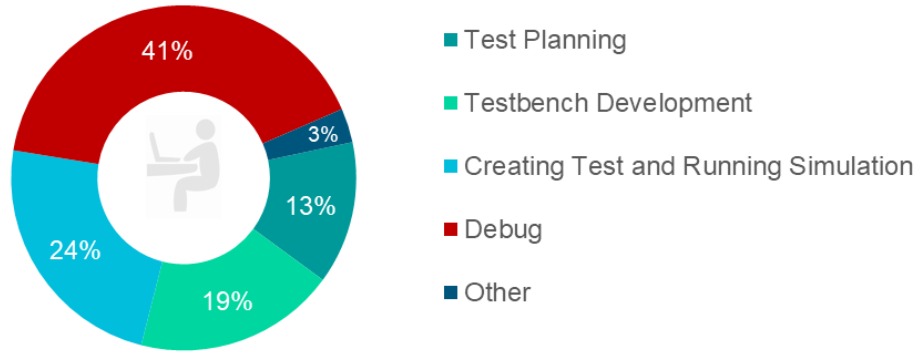
Verification for HEP ASICs

- **Extreme Radiation Tolerance**
  - Fault injection campaigns
  - Single Event Transient
  - TID (Total Ionizing Dose) aware designs
- **High data-rate**
  - High-Luminosity Large Hadron Collider (HL-LHC), hit rate of 3.5 GHz/cm2
  - Trigger-based architectures (RD53)
  - Data-driven architectures (Velopix)

Where ASIC/IC Verification Engineers Spend Their Time



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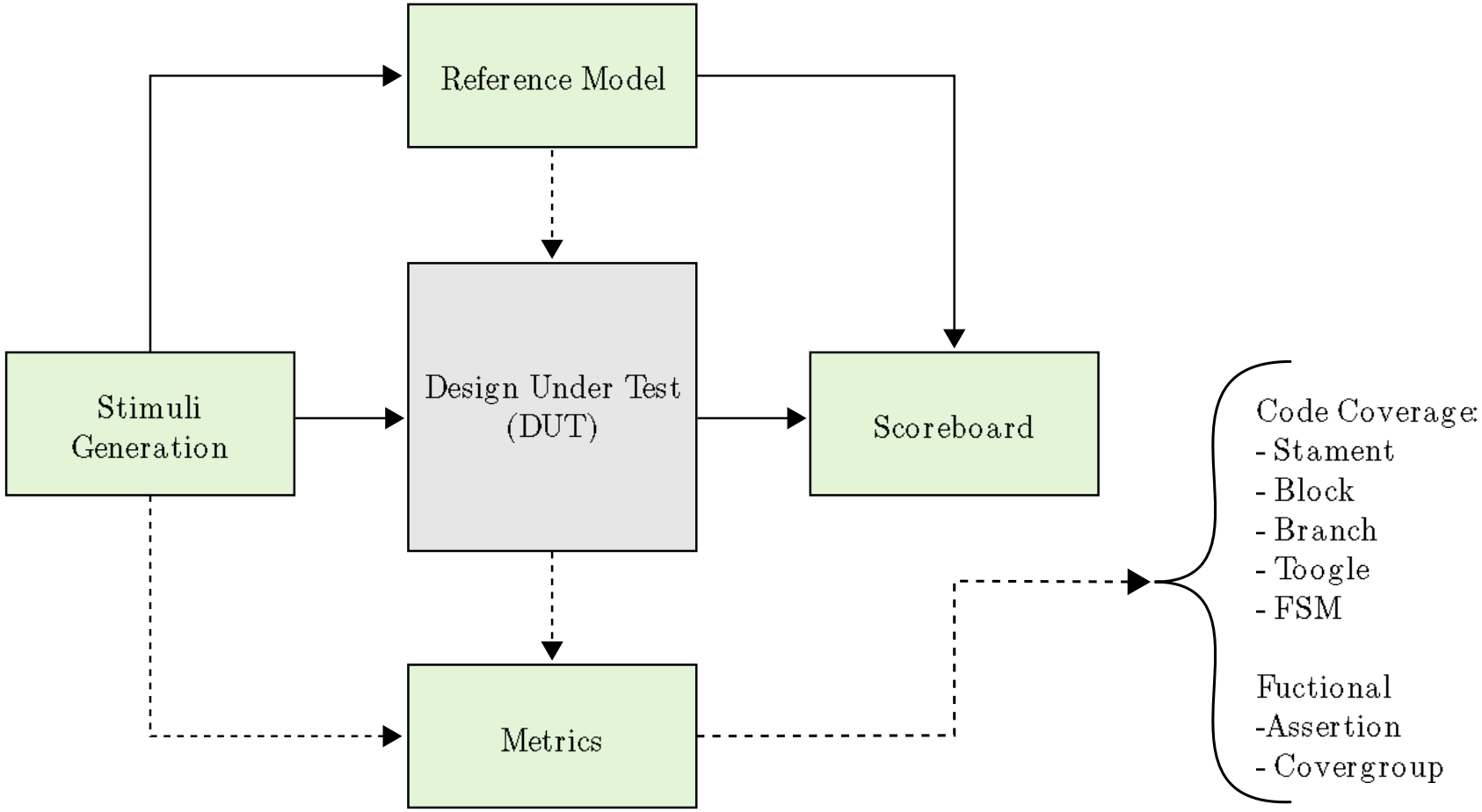
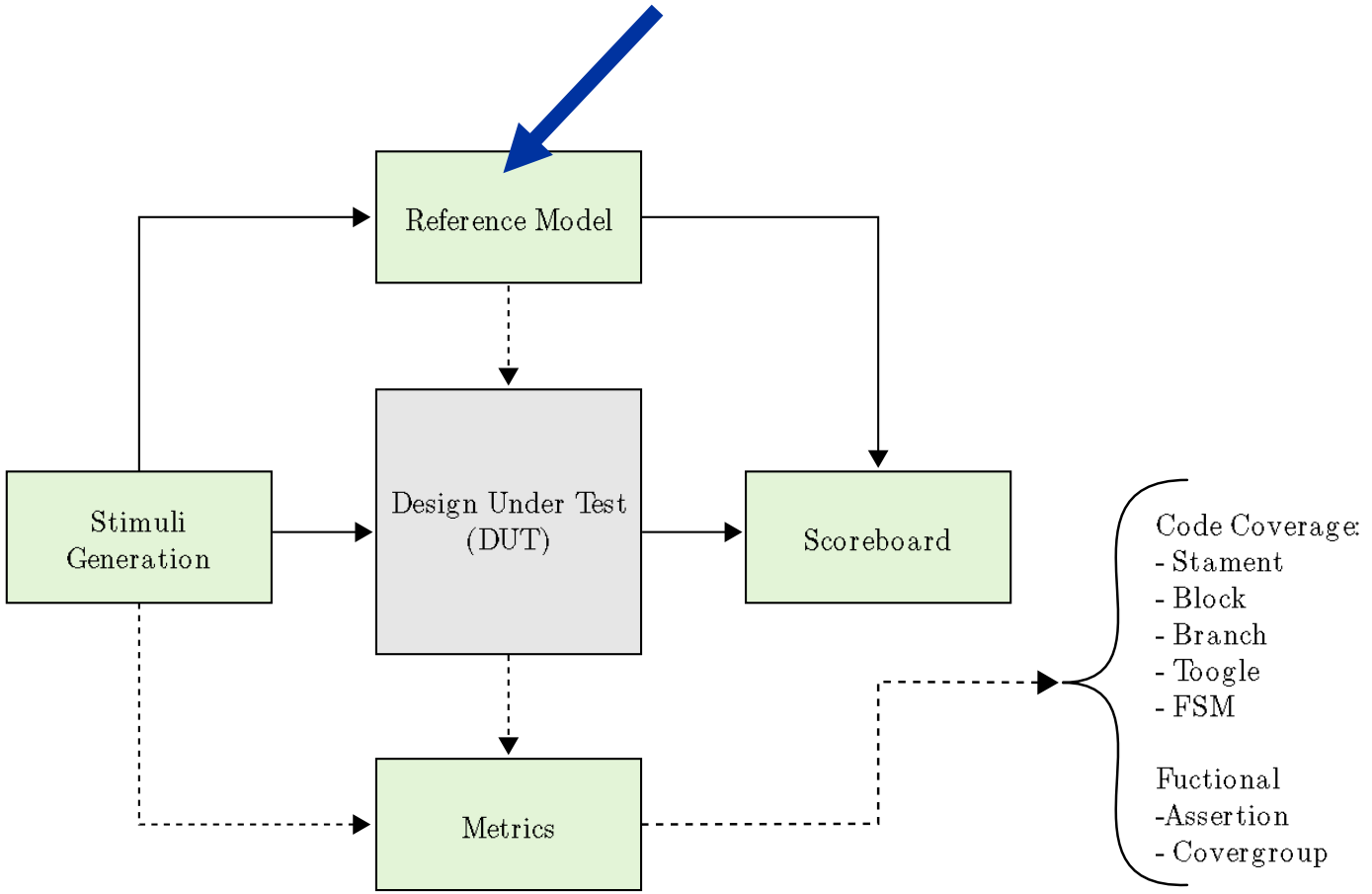
Verification Methodology

Anatomy of a Verification Environment



Reference Model

- **Receive the same stimuli as the DUT**
- **Predict DUT output**
  - Based on specifications
  - Implements the transfer function(s)
- **Tightly tied to DUT specification**
- **Using C++ / SystemC**



Research activities carried out so far 1st year

Tools

- **Improvement knowledge of the following tools:**
  - Verilog / SystemVerilog
    - UVM
  - C/C++
    - SystemC
  - Python
    - Jinja2
    - PyYAML
  - Bash
  - Synopsys

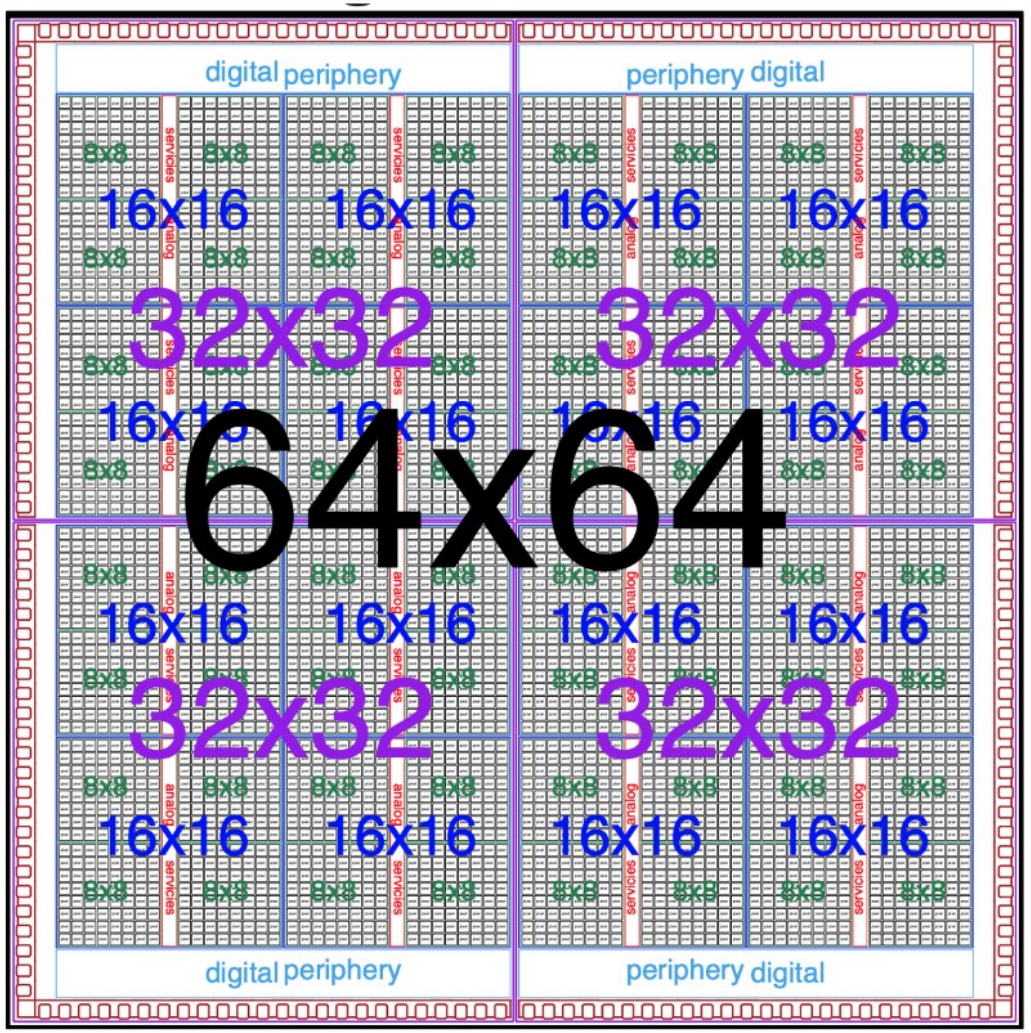
SYNOPSYS®

Activities carried out

- **Development of Verification Utility Tools and Scripts to facilitate workflow.**
  - UVC Code Generator
  - Linting and Formatting utility scripts
  - Resource Guide
  - UVM UVC Tutorial
- **Development of general purpose UVM Verification IPs (VIP) to be use in different projects**
  - GPIO UVC
  - Clock Generator UVC
  - I2C UVC

IGNITE64 ASIC

- **The IGNITE project aims at developing read-out and processing solutions for high intensity 4D-tracking**
  - Concurrent high time less than 50 ps and space resolution of 10 μm
  - Power density as low as possible around 1 W cm^{-2}
  - Operate at large fluences (> 1x 10^{16} 1 MeV neutron per cm^2)
  - High total ionizing dose (TID > 1 Grad)
  - 28 nm CMOS technology



Plan for 2nd and 3rd years

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- **2nd Year**
  - Start using UVM expertise in real ASIC - IGNITE chip
    - UVCs connection
    - Create basic coverage
    - Directed tests
  - Create new UVCs specific for the chip
  - Create SystemC model studies
    - FIFO connections
    - Datapath possibilities
    - Based on CERN PixESL framework
- **3rd Year**
  - Continue working in the development of the verification framework
  - Optimize the verification environment according to the project goals.
  - Write detail documentation for UVC IPs
  - Write the thesis
  - Prepare for thesis defense

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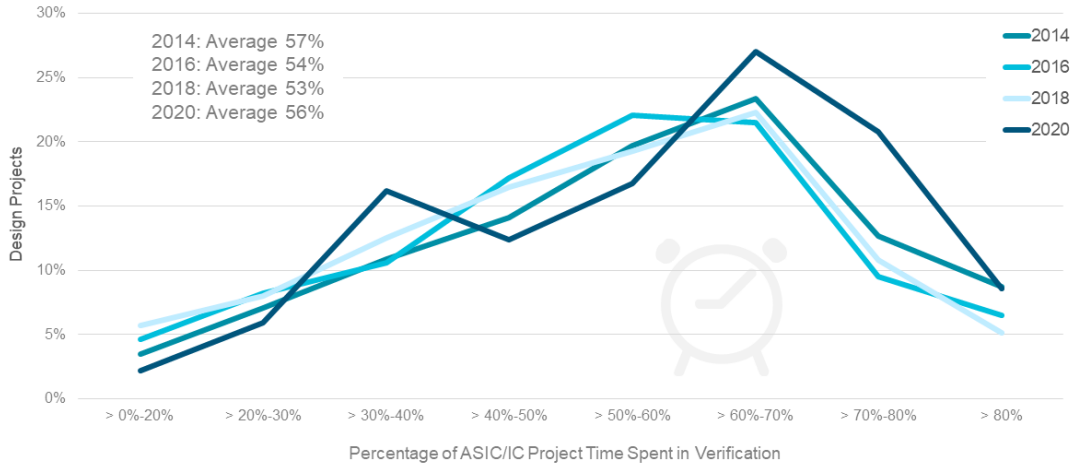
Verification: a bottleneck

- **ASIC verification is more complex and time consuming than design**
- **Verification is resource intensive**
- **New skill in HEP community**

Percentage of ASIC/IC Project Time Spent in Verification



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study

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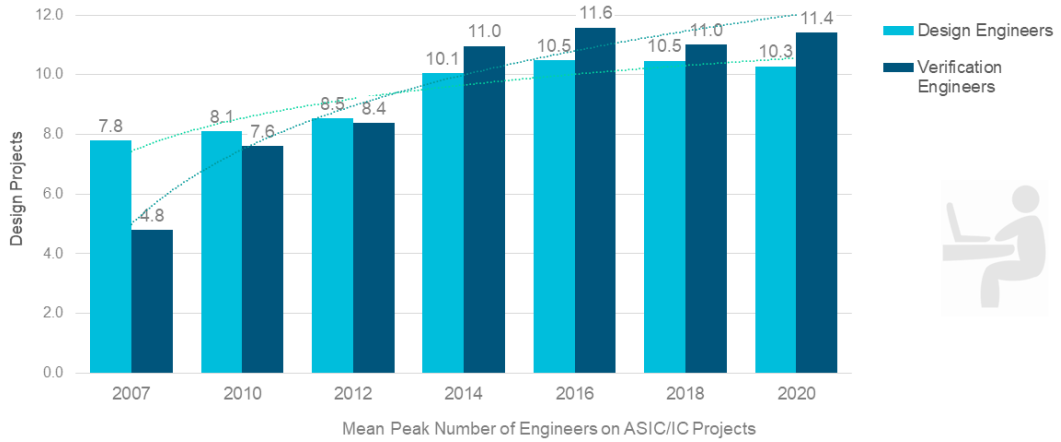
Mean Peak Number of Engineers on an ASIC/IC Project



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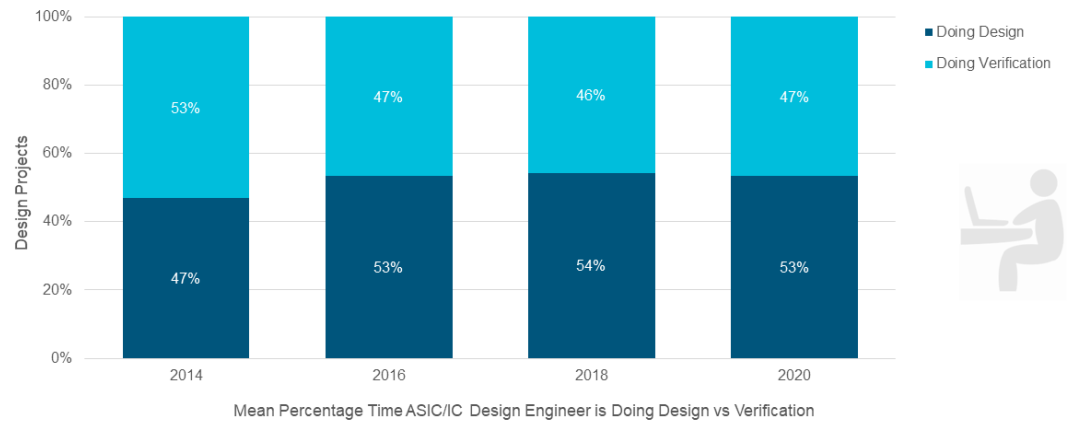
Mean Time ASIC/IC Design Engineer is Doing Design vs Verification



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Details of VIPs

- **GPIO UVC**
  - Support single pin or arrays of pins, synchronous and asynchronous change in levels
  - Use cases: driving/monitoring GPIO, reset pins
- **Clock Generator UVC**
  - Generates a set of related clock, each clock can have independent jitter and phase difference
  - Use cases: generate related clocks base on one single source as in real experiments
- **I2C UVC**
  - Control a I2C bus in a master configuration
  - Use cases: DUT configuration, registers operation