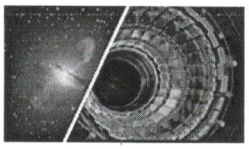

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UNIVERSITÀ DEGLI STUDI DI PADOVA

PhD course of National Interest in Technologies for Fundamental Research in Physics and Astrophysics

Annual report

Name and surname: Ciro Fabian Bermudez Marquez
Cycle and a.a.: 39th Series 2023/2024
Supervisor: Flavio Loddo

• Research activity carried out during the year

The research focuses on the development of a UVM verification framework to prove the correctness of pixel chip design to be used in future projects in the field of High Energy Physics (HEP). Moreover, the modelling of pixel-based detectors, from front-end to back-end, at a high level of abstraction to perform architectural studies will be implemented. This will provide metrics to compare different solutions to satisfy functional and non-functional requirements, both at detector and readout chip level.

The primary aim of this project is to create a comprehensive set of resources, tools, and reusable components to simplify and enhance verification in SystemVerilog, particularly focusing on Universal Verification Methodology (UVM). During the year, I focused on developing resources and automation tools to facilitate UVM adoption and improve verification efficiency. The key activities involved creating Git repositories with various verification resources and tools:

1. Resource Guide: A complete reference guide with books, papers, websites, and blogs was compiled to assist with learning UVM and SystemVerilog. This guide serves as an educational foundation.
2. Tutorial for UVM Components: I created a tutorial demonstrating how to develop UVM components from scratch. The tutorial covers essential aspects such as monitor, driver, sequence item, sequencer, sequence, agent, environment, tests, and coverage, providing a comprehensive hands-on guide.
3. Automation Scripts: To automate verification processes, I developed a script that installs Verible and Verilator. These tools enable linting and formatting of both HDL and HVL code, reducing manual errors and enforcing code quality.
4. UVC Code Generator: I developed a Python-based UVC (Universal Verification Component) code generator. This tool is based on the UVM Cookbook and Doulos' Easier UVM Coding Guidelines and helps users automatically generate reusable UVM components, saving significant development time.
5. General-Purpose IO UVC: A UVC for driving and monitoring general-purpose input/output (GPIO) pins was implemented, supporting various verification tasks.
6. Clock Generator UVC: I created a UVC to generate related clocks with independent jitter and phase differences, enabling more complex clock scenarios in simulations.
7. I2C UVC: An I2C UVC was developed to emulate an I2C master write operation, facilitating the verification of I2C-based communication protocols.

The activities above are destined to be used in the development of the verification framework of the IGNITE64 chip currently under design in the INFN community.

One of the primary challenges encountered was the complexity of UVM itself, which requires a deep understanding of Object-Oriented Programming (OOP), design patterns, and proficiency in SystemVerilog. UVM's abstraction layers are powerful but demand a solid grasp of these advanced programming concepts, making it difficult for users, especially beginners, to fully utilize UVM's capabilities.

Additionally, UVM is a constantly evolving framework, with yearly updates introducing new features and often deprecating older methodologies. This ongoing evolution makes it challenging to maintain compatibility and consistency across different UVM implementations, as some previously accepted coding practices become outdated or discouraged. To address this, I ensured that my guides and automation scripts were kept up to date with UVM 1.2, and I emphasized the use of best practices to mitigate the impact of deprecated methods.

- **List of attended courses and passed exams**
  1. Front-end electronics and DAQ systems for radiation detection (HE5)
- **List of attended conferences, workshops and schools, with mention of the presented talks**
  1. CERN – Verification with UVM for HEP Workshop (27/02/2024 – 01/03/2024)
  2. CERN – Training Framework PixESL for simulation of pixel chips (07/04/2024 – 12/04/2024)
  3. INFN Bari – Synopsys, Language: System Verilog Testbench
  4. INFN Bari – Synopsys, Language: System Verilog Verification using UVM
  5. INFN Bari – Cadence, System Verilog for design and verification
- **List of published papers/proceedings**
- **Thesis title (even temporary)**

Design and verification of read-out ASICs in 28 nm CMOS technology for next generation pixel detectors

Date, 09/09/2024 **Signature:**

Seen, the supervisor