



PhD course of National Interest in Technologies for Fundamental Research in Physics and Astrophysics

Annual report

Name and surname: Fatima Bzeih Cycle and a.a.: 39th Cycle Supervisor: Prof. Paolo Musico

• Research activity carried out during the year

Overview of the System

The data acquisition (DAQ) system developed for high-energy physics (HEP) experiments is designed to detect, amplify, digitize, and transmit data from particle detectors. These experiments generate enormous amounts of data that must be captured and processed in real-time to ensure accurate and efficient analysis. Traditionally, VME-based systems have been used, but their high cost and limited scalability have prompted the shift toward more modern solutions, such as Ethernet-based DAQ systems. Ethernet offers significant speed, flexibility, and cost advantages, making it an ideal choice for transmitting data in HEP experiments. This system's core is the FPGA Kintex-7, which handles high-speed data processing and transmission, ensuring that the DAQ board can meet the performance demands of such experiments.

Project Aim

The primary aim of the project is to design and characterize a data acquisition board for HEP experiments using 1G/10G Ethernet connections as an alternative to the traditional VME system. **Initial Research and Preparation**

At the start of this project, an extensive review of the literature on data acquisition systems in highenergy physics was conducted to understand current technologies and their limitations. This provided a solid foundation for identifying key requirements for the new system. In parallel, essential technical skills such as C programming were developed to support the implementation of complex algorithms on hardware. This groundwork was critical for understanding the broader scope of the project before moving on to FPGA programming. After gaining these foundational skills, The Kintex-7 FPGA was selected due to its ability to handle high-speed data, efficiency, and cost.

Research Activity Conducted

Throughout the first year, research efforts have focused primarily on FPGA programming, specifically in developing and testing the software needed to manage ADC deserialization and Ethernet connectivity. Significant milestones include the successful implementation of the 1G Ethernet connection using hardware-only blocks. Additionally, the ADC deserializer was developed to ensure efficient digitization of analog signals from particle detectors.

Challenges and Solutions

Several challenges arose during the development process, particularly in programming the FPGA and generating bitstream files. There were frequent implementation failures that required significant troubleshooting.

To resolve these issues, collaboration with the project supervisor prof. Paolo Musico provided critical insights into effective troubleshooting strategies. Additionally, thorough research into technical documentation and best practices for FPGA programming and Ethernet connectivity helped address these challenges. As a result, the 1G Ethernet connection and ADC deserialization were successfully implemented, creating a strong foundation for the project's future development.





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Utilizing Ethernet Instead of VME for MPD Moving forward, the focus will be on fully transitioning the MPD system from VME to Ethernet and setting up the simulation testbench for it. Once the board is available for testing, the Ethernet interface will be thoroughly evaluated and optimized to ensure it can reliably replace the traditional VME system.

• List of attended courses and passed exams

Course Title	Credit	Status
Electronics and Data Acquisition	2.5	Preparing for the final exam
Machine Learning programming in physics	2.5	Preparing for the final exam
Gaseous detector for experimental particle physics	2.5	Started from 10 th September
Design of readout integrated circuits for particle detector	2.5	Start from 4 th November
Italian Language Course	-	Start next week

• List of attended conferences, workshops and schools, with mention of the presented talks

- **Conference 1:** 16th Pisa Meeting on Advanced Detectors.
- **Type:** Participate.
- Conference 2: SIE Meeting
- **Type:** Poster Presentation.
- Paper Title: Low Power Design of Approximate Adders based on Inexact Full Adder
- **Objective:** Present a poster summarizing part of the master thesis work.
- > Searching to attend summer school next months.

• List of published papers/proceedings

 Soon will start to write a paper about the work done which is "Development of a high performance network based data acquisition board dedicated to high energy physics experiment".





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- Second paper will be about the Performances of a newly developed network based data acquisition board....
- Thesis title (even temporary)

"Design and Characterization of a Data Acquisition Board for High Energy Physics Experiment with a 1G/10G Copper/Optical Ethernet connection"

Date: 9/9/2024

Signature: F.B

Seen, the supervisor

Paolo Musico