

Quantum Computing @ CINECA

Integrating a Quantum Accelerator into an HPC Environment

Daniele Ottaviani

Cineca Quantum Computing Lab

Teaching, Outreaching
and Dissemination



European and National
projects



Fondazione
ICSC
Centro Nazionale di Ricerca in HPC,
Big Data and Quantum Computing

EURO



QUANTUM
COMPUTING
AND
SIMULATION
CENTER

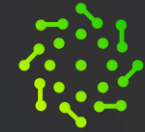


QUANTUM COMPUTING LAB

Quantum Computing
Resources

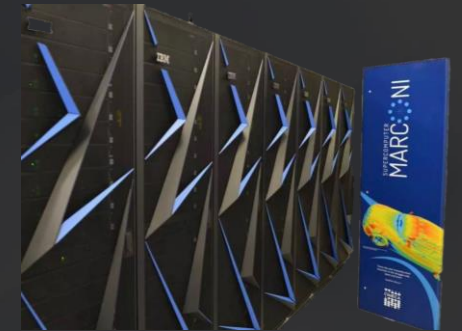
Cloud QC

D:WAVE
The Quantum Computing Company™



PASQAL

HPC QC
Emulation



CINECA

QUANTUM
COMPUTING LAB

Cineca Quantum Computing Lab

Teaching, Outreaching
and Dissemination



European and National
projects



Fondazione
ICSC

Centro Nazionale di Ricerca in HPC,
Big Data and Quantum Computing

EURO



QUANTUM
COMPUTING
AND
SIMULATION
CENTER

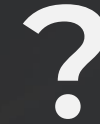
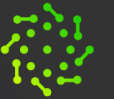


QUANTUM COMPUTING LAB

Quantum Computing
Resources

Cloud QC

D:WAVE
The Quantum Computing Company™



PASQAL

Hybrid HPC-QC System



CINECA



Available emulators on Leonardo

Already available

- Cirq (Google) – GPU, cuQuantum
- Ocean (D-wave)
- Qiskit (IBM) – MPI, GPU, cuQuantum
- Pulser (Pasqal)
- Qibo – GPU, cuQuantum
- PennyLane – MPI, GPU, cuQuantum
- Quantum Matcha Tea – MPI, GPU

Work in progress:







- QuEST – MPI, GPU
- Cuda Quantum – MPI, GPU, cuQuantum





EuroHPC
Joint Undertaking

The EuroHPC JU has selected six sites across the European Union to host and operate the first EuroHPC quantum computers in:

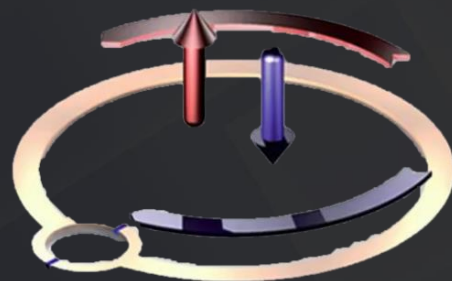
-  Czechia
-  France
-  Germany
-  Italy
-  Poland
-  Spain



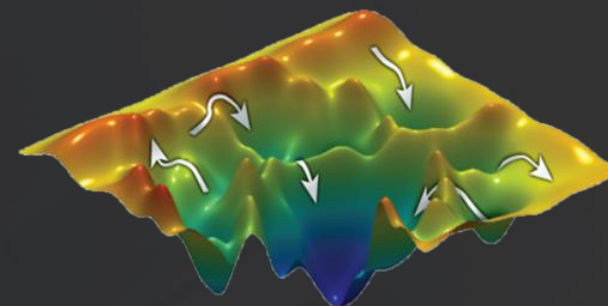
EuroQHPC-I



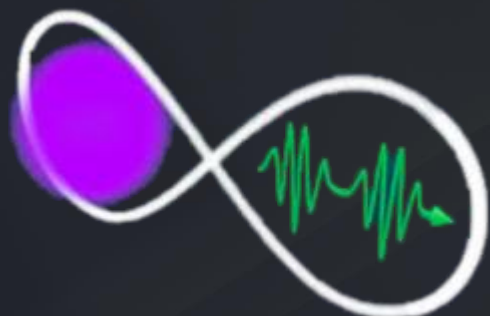
**EuroQCS
Italy**



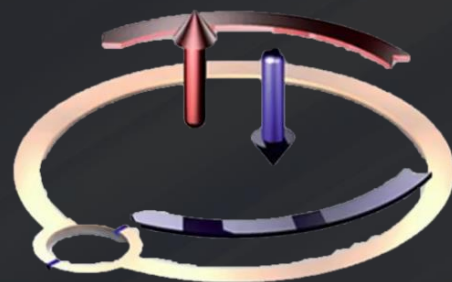
LUMI-Q



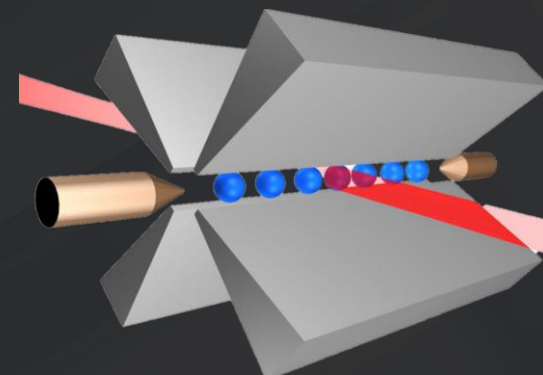
**EuroQCS
Spain**



**EuroQCS
France**



**Euro-Q-
Exa**

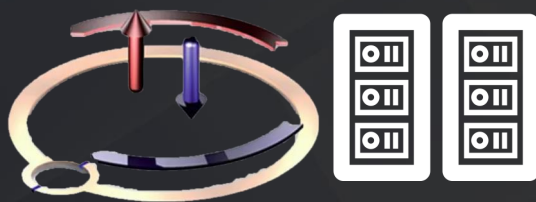


**EuroQCS
Poland**

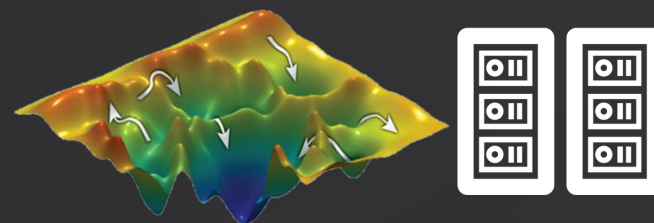
EuroQHPC-I



EuroQCS
Italy



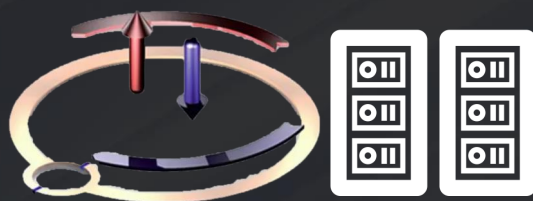
LUMI-Q



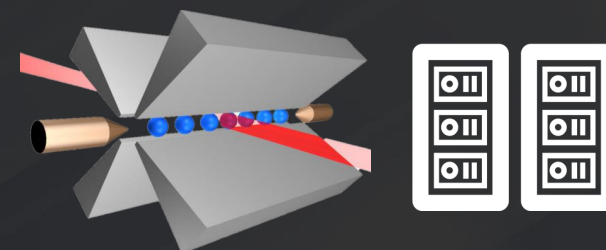
EuroQCS
Spain



EuroQCS
France

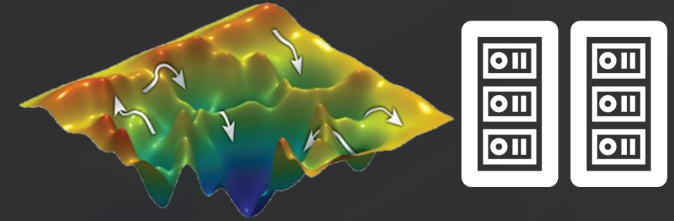
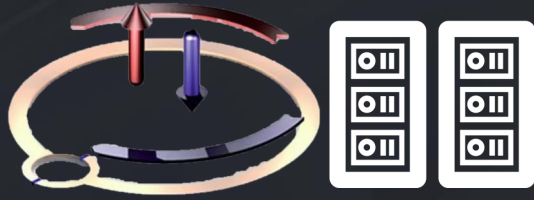
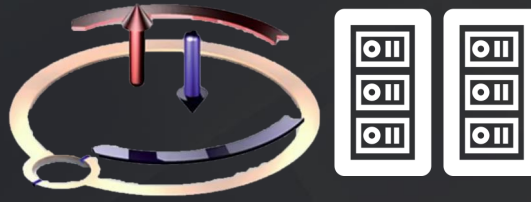


Euro-Q-
Exa

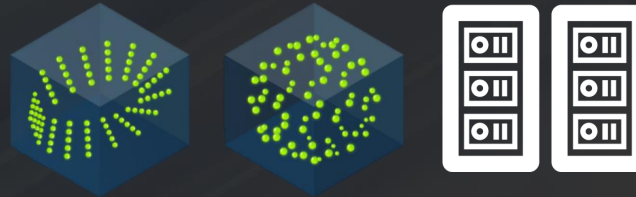
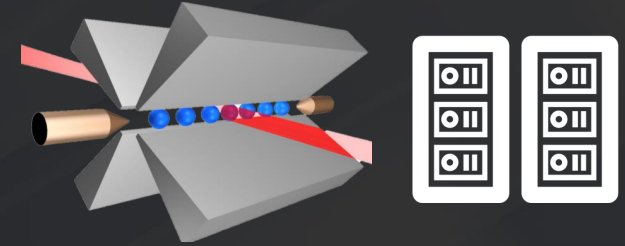


EuroQCS
Poland

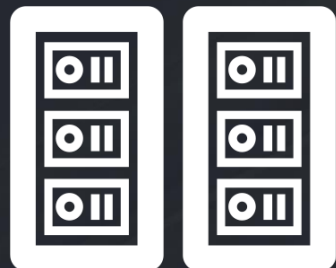
EuroQHPC-I



EuroHPC
Joint Undertaking



EuroQCS-Italy



Leonardo - BullSequana XH2000, Xeon Platinum 8358 32C 2.6GHz, NVIDIA A100 SXM4 64 GB, Quad-rail NVIDIA HDR100 Infiniband

Rpeak 306.31 PFlop/s, Top500 Rank: 7



Neutral Atoms Analog Quantum Simulator

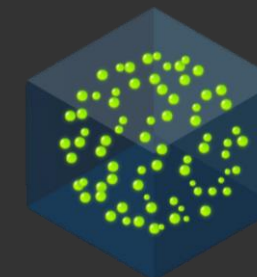
140 qubits – Q2 2025

Upgrade path: enabling partial addressability (Q3 2026)



Superconducting Digital Quantum Computer

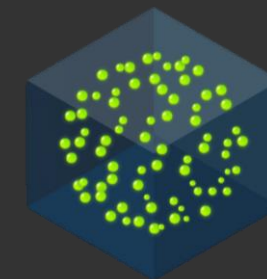
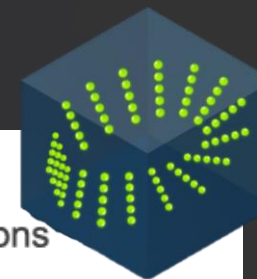
54 qubits – Q1 2025



EuroHPC
Joint Undertaking

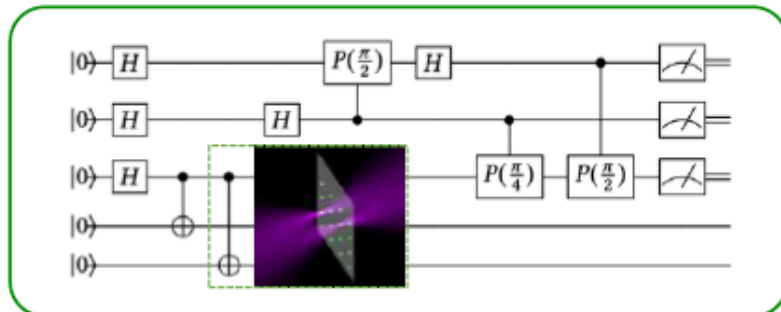


Neutral Atoms Quantum Simulators



Digital mode

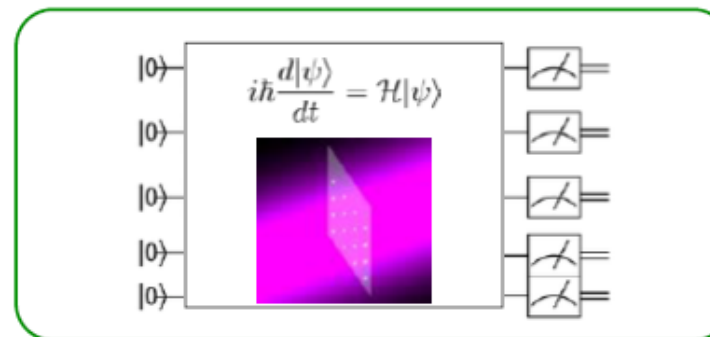
Programming a logic circuit = **quantum gates**



Elementary operations on individual qubits, or on several qubits at the same time → **universal** but very **sensitive to noise**

Analog mode

Programming a **sequence of Hamiltonian** evolutions



The Hamiltonian faithfully describes the dynamics of the physical system → **not universal** but offers **better performances with NISQ processors**.

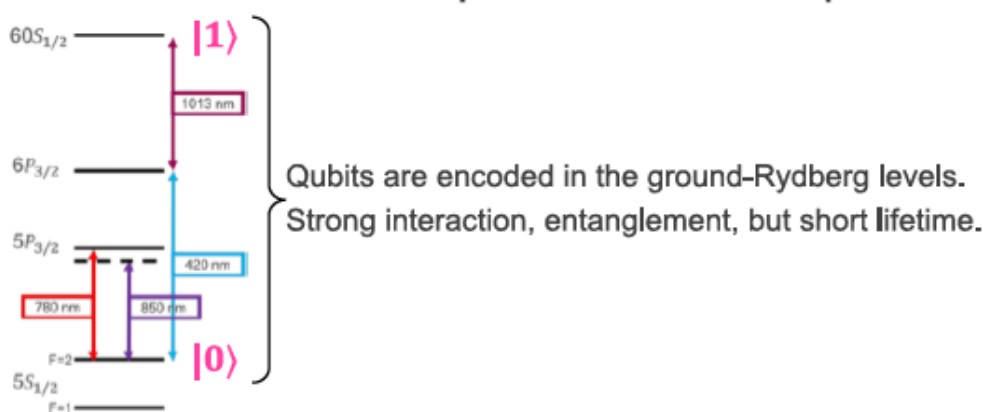
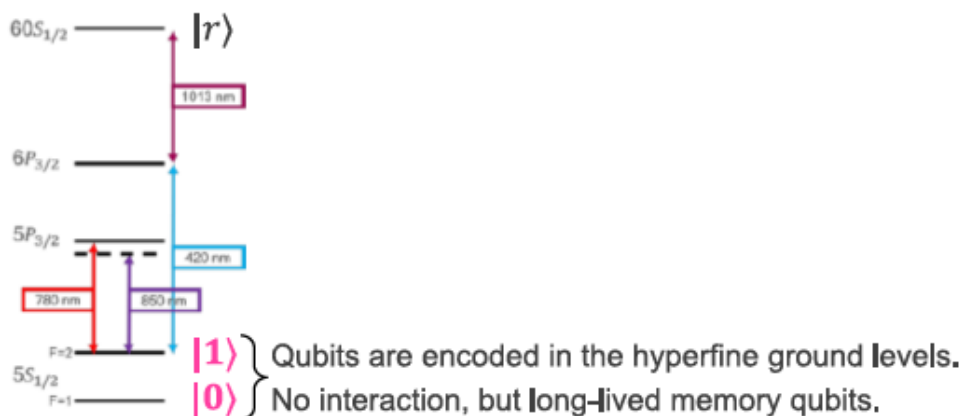
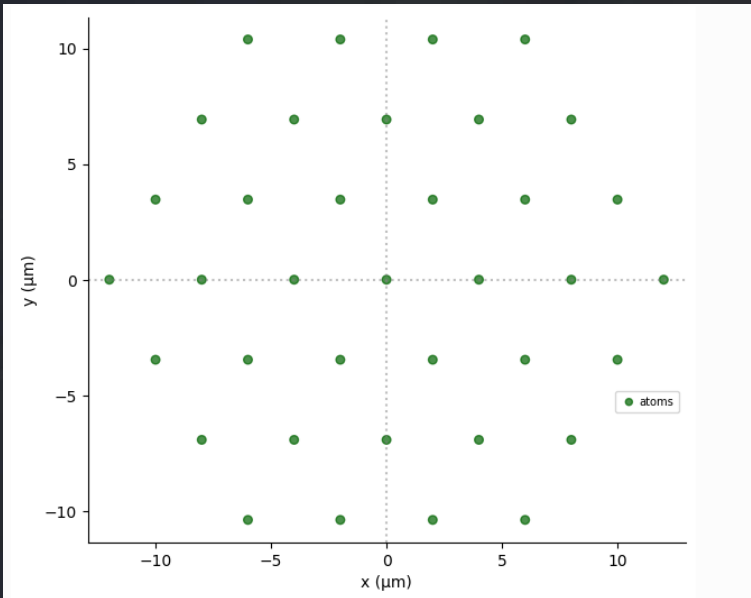
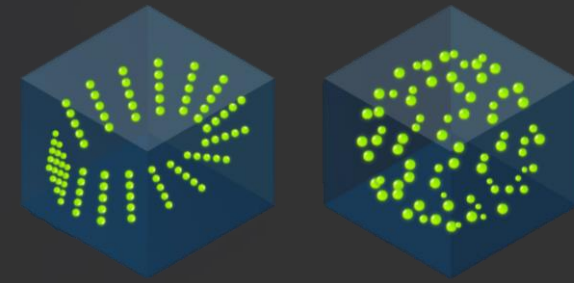


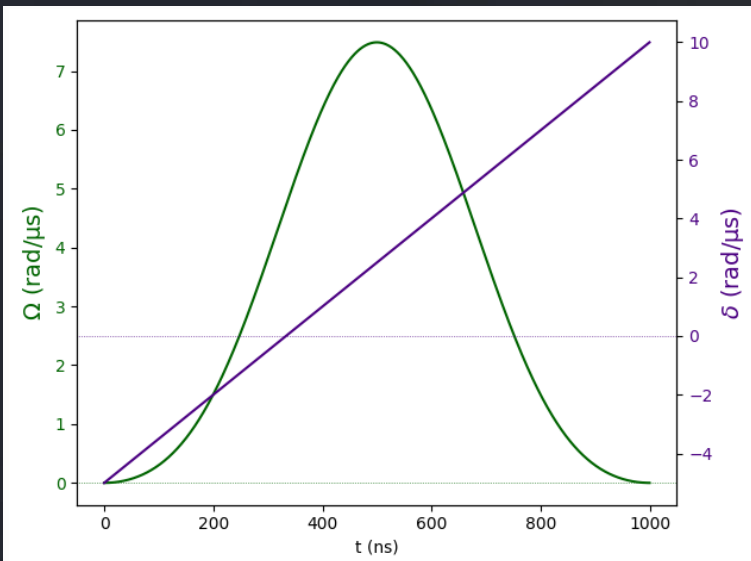
Figure 454: a clear explanation of the difference between a digital gate-based mode and an analog, quantum simulation mode.

Source: Pasqal. 2023.

Neutral Atoms Quantum Simulators

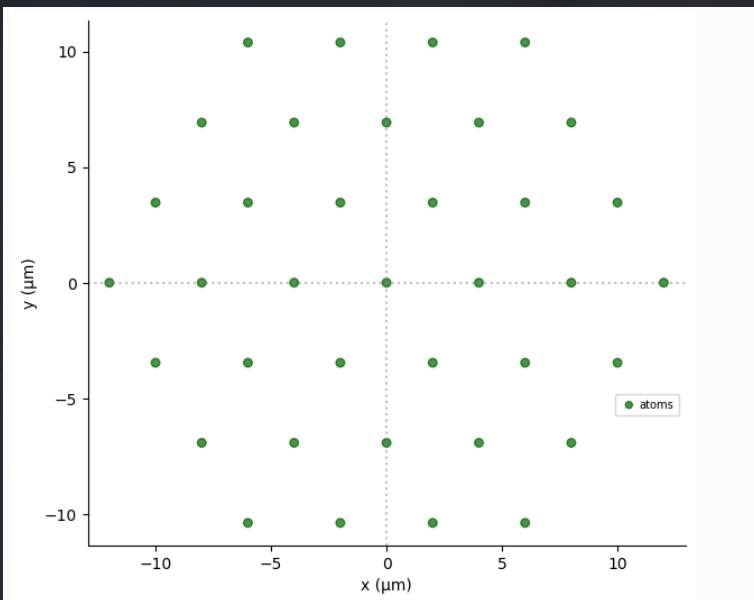
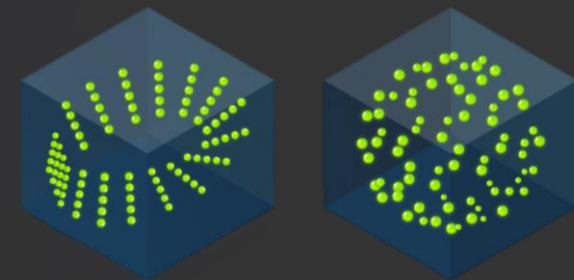


$$\frac{\hbar}{2} \sum_i \Omega(t) \sigma_i^x - \frac{\hbar}{2} \sum_i \delta(t) \sigma_i^z + \sum_{i < j} U_{ij} n_i n_j$$
$$\mathbf{n} = (1 + \sigma^z) / 2, \quad U_{ij} \propto R_{ij}^{-6}$$

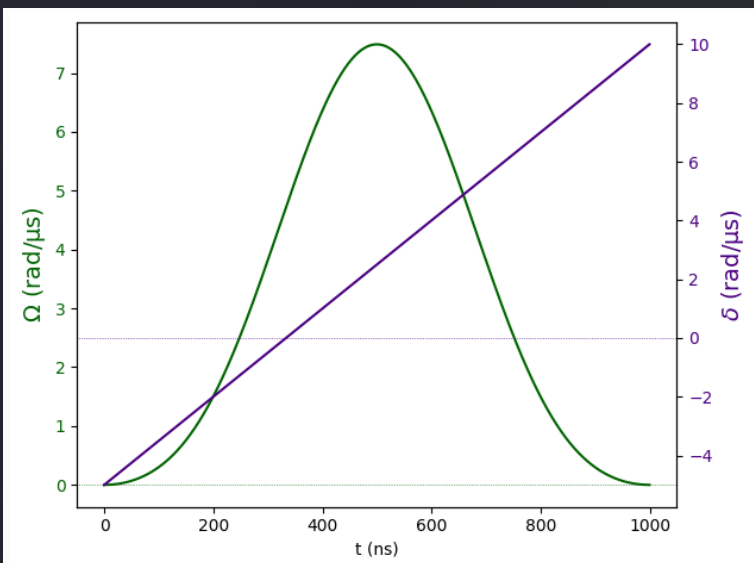


<https://pulser.readthedocs.io/en/stable/review.html>

Neutral Atoms Quantum Simulators



$$\frac{\hbar}{2} \sum_i \Omega_i(t) \sigma_i^x - \frac{\hbar}{2} \sum_i \delta(t) \sigma_i^z + \sum_{i < j} U_{ij} n_i n_j$$
$$n = (1 + \sigma^z) / 2, \quad U_{ij} \propto R_{ij}^{-6}$$



Partial Addressability

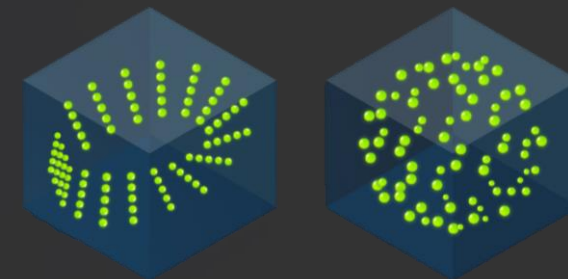
Understanding Quantum Technologies

Understanding Quantum Technologies

Seventh edition – 2024

Olivier Ezratty

Neutral Atoms Quantum Simulators



neutral atoms qubits key takeaways

highlights

- operational systems with 100-300 atoms in simulation mode and not far from a provable quantum advantage.
- long qubit coherence time and fast gates.
- identical atoms, that are controlled with the same laser and microwave frequencies.
- first logical qubits thanks to movable atoms.
- works in both simulation and gate-based paradigms.
- no need for specific integrated circuits.
- uses standard apparatus: lasers, optics, controls, cryogenics.
- low energy consumption.

challenges

- crosstalk between qubits: can be mitigated with two-elements atom architectures.
- slow operations: 1 Hz simulation cycle.
- harder to implement with gate-based model: need a stable universal gate set with support for error correction.
- need to move atoms around: to enable many-to-many two-qubit gates and reducing QEC overhead, enabling qLDPC, but with risk of losing the atoms on the way.
- implement full QND measurement: needed for error correction.
- losing atoms during computing while disconnecting the tweezers.

variations

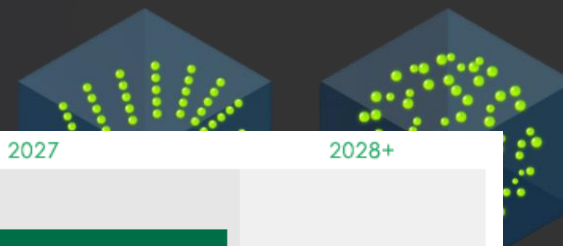
- dual species qubits: to improve QND measurement.
- nucleus spin qubits: with longer coherence times, in seconds.
- circular Rydberg atoms: more stable.
- fermionic computing: better for chemical simulations.
- bosonic codes (cat-codes, GKP) with atom qubits: better QEC.
- hybrid gate-based and analog: for specific case studies.
- atoms trapped on nanophotonic circuits: enabling interactions.
- hybrid neutral atoms and ions: getting the best of both worlds.
- atom ensembles: studied particularly in China.

path to scalability

- powerful lasers: needed to control >300 atoms, with stabilized power, fiber lasers.
- atoms positioning: large scale SLM+AOD to trap up to 10K atoms.
- QND measurement: using dual species and/or atoms shuttling.
- faster operations and duty cycle: better and more powerful lasers, fast classical controls (FPGA, ASIC).
- implement full universal gate set: T gate & magic state distillation.
- QPU interconnect: photon based, including for memories, can also use nanophotonic circuit traps.

Figure 441: pros and cons of cold atoms quantum computers and simulators. (cc) Olivier Ezratty, 2022-2024.

Neutral Atoms Quantum Simulators



2022 - 2023

2024 - 2025

2026 - 2027

2028+

Technology
PASQAL & affiliated ecosystem

HARDWARE PLATFORM

Max qubits

200

Addressability

Z add

1,000

Z+X add

Addressable 1Q and 2Q gates

10,000

Base repetition rate

1 Hz

3 Hz

10 Hz

100 Hz

FTQC Program

Atom shuttling

Ultra High-Fidelity Gates

Scalable logical qubits architecture

HARDWARE ACCELERATED LIBRARIES

Quantum Matter & Quantum AI

Algorithm Blueprint

Algorithm Development

Production

Products

QUANTUM PROCESSORS

Generation

Orion Alpha
~3M gates

Orion Beta
~5M gates
On premise delivery

Orion Gamma
~10M gates
On premise delivery

Vela
~40M gates

Pegasus
~200M gates

Centaurus FTQC QPU
128+ Logical qubits
200M+ gates

Total hours of QPU for users

500

5-10,000

20-30,000

60-70,000

200-250,000

500-550,000

Factories

France

Canada

Factory 3

COMMUNITY

Platform

Learn

Interact

Collaborate

Open-source Software Stack

Pulser

Qadence

Solvers & Emulators

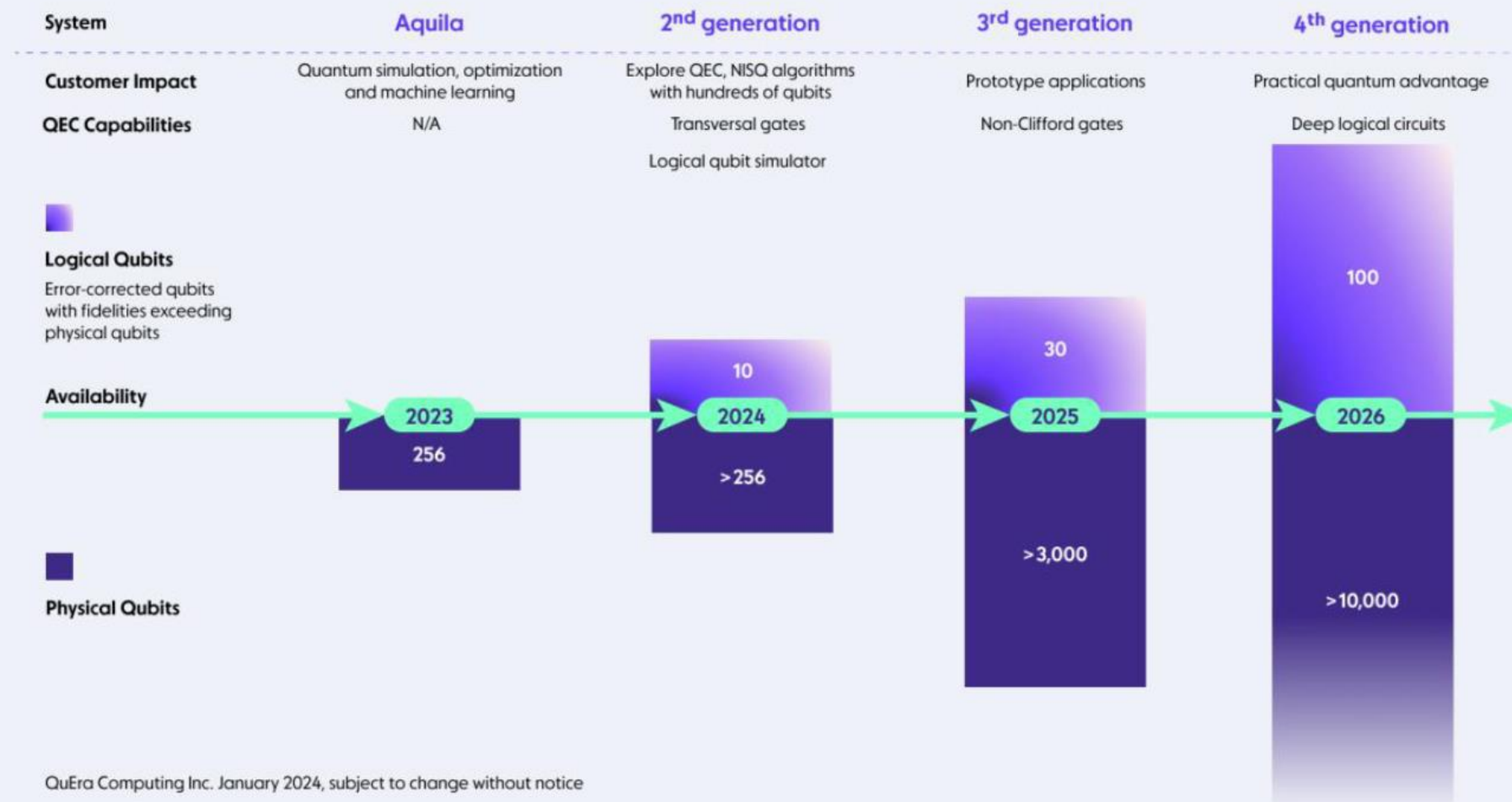


Pasqal

Neutral Atoms Quantum Simulators

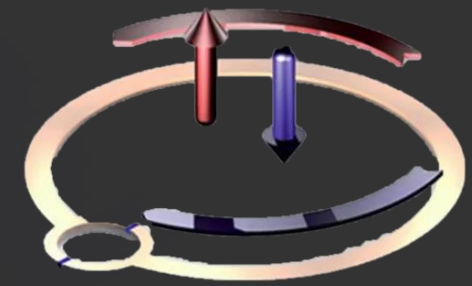


Error-Corrected Quantum Computing Roadmap



QuEra Computing Inc. January 2024, subject to change without notice

Superconducting Qubits



superconducting qubits key takeaways

highlights

- **key technology** in the academic world and with the largest and well funded commercial vendors community including large players like IBM, Google, IQM and Rigetti.
- **record of 156 programmable qubits** with 99.7% two qubit gates fidelities (IBM Heron r2, 2024).
- **noise reduction** constant progress in regular transmons with tunable couplers and with bosonic qubits which could enable a record low ratio of physical/logical qubits.
- **first break-even logical qubits:** Google in August 2023.
- **enabling technologies** are abundant with cryostats, cabling, analog electronics, amplifiers, and sensors.
- **quantum error mitigation** and **quantum error correction** known techniques to enable NISQ applications and future FTQC designs.

challenges

- **qubits variability:** requires calibration and complex micro-wave frequency maps and need to contain crosstalk.
- **qubit connectivity:** limited to neighbor qubits in 2D structures.
- **qubit coherence time:** usually $< 300 \mu\text{s}$ with some lab records $> 1\text{ms}$.
- **cryogeny:** constrained technology at $< 15 \text{ mK}$, but not a scientific obstacle per se, more an engineering one. Yield can be improved.
- **logical qubits:** are not yet under break even. They are currently worse than physical qubits in most experiments.
- **cabling clutter:** complexity and many passive and active electronic components to control qubits with micro-waves and other signals.
- **qubits size:** uneasy miniaturization limits qubit # per chips and requires QPU interconnect solutions.
- **qubit fidelities:** have a hard time reaching 99.9%, needed for QEC.

variations

- **bosonic qubits:** cat-qubits, GKP, dual rail with self-correction and lower QEC overhead. They are less mature but promising.
- **fluxonium qubits:** with better fidelities but a more complicated designs and few involved vendors.
- **qutrits:** with larger Hilbert space, which are exotic in the commercial world.
- **Andreev spin qubits:** localized excitation of the BCS condensate that natively has only two levels, using a nanowire.
- **hybrid quantum analog-digital architectures:** to solve specific problems, not generic.

path to scalability

- **materials:** improve elements purity, identify other promising ones.
- **EDA:** full stack electronic design automation tools.
- **manufacturing:** industrialization, 300 mm wafers epitaxial deposition.
- **qubit mid-range coupling:** to enable lower overhead qLDPC QEC.
- **interconnect:** using transduction and photonic gate teleportation.
- **signals multiplexing or SFQ control electronics:** to reduce cabling overhead and cryogenic requirements.
- **QEC syndrome detection** speed improvements using ASICs.
- **cryostats:** larger and more efficient.

Figure 301: superconducting qubits highlights, challenges, variations and path to scalability. (cc) Olivier Ezratty, 2021-2024.

Superconducting Qubits



IBM Q
may 2016
5 qubits



IBM Q may 2017
17 qubits

IBM Q
oct 2017
50 qubits
(labo)



IBM Q System One jan 2019
20 qubits

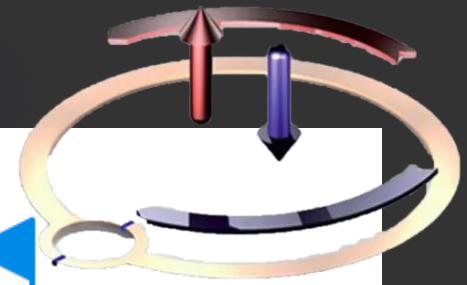
Rochester sept 2019
53 qubits

Nature paper on quantum utility with QEM june 2023

Eagle nov 2021
127 qubits

System Two 2023

Osprey may 2023
433 qubits
(retired in 2023)



2017

2018

2019

2020

2021

2022

2023

2024

IBM oct 2017
HPC 56 qubits simulator

Hummingbird 2020
65 qubits

Condor 2023
1,121 qubits (retired)

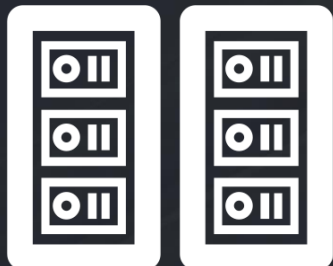
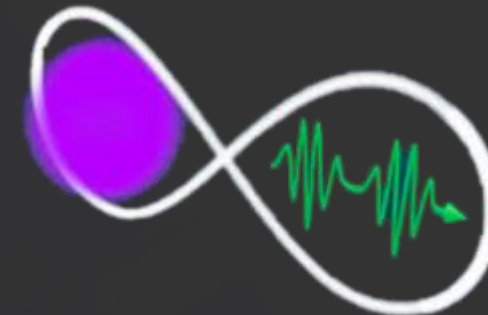
Heron r1 2023
133 qubits

IBM Q System One jan 2020
28 qubits

Heron r2 2024
156 qubits



EuroQCS-France



JOLIOT-CURIE ROME - Bull Sequana XH2000 , AMD Rome 7H12 64C 2.6GHz, Mellanox HDR100

Rpeak 12.04 PFlop/s, Top500 Rank: 132



Neutral Atoms Analog Quantum Simulator
100 qubits – Q1 2025

<HPC|Q.S>



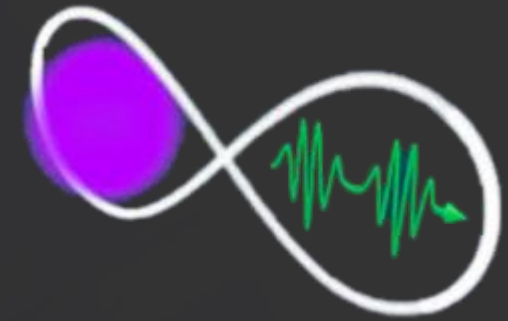
EuroHPC
Joint Undertaking



Photonic Quantum Computer
12 qubits – Q3 2025
Upgrade path: 24+ qubits Q3 2026

QUANDELA

Photonic Quantum Computers



photon qubits key takeaways

highlights

- **stable qubits** with absence of decoherence.
- **ambient temperature for processing.**
- **emerging nano-photonic manufacturing techniques** enabling scalability.
- **easier to scale-out** with inter-qubits communications and quantum telecommunications.
- **MBQC/FBQC** circumventing the fixed gates depth computing capacity and difficulty to create multiple qubit gates.
- **boson sampling-based quantum advantage:** starts to being programmable but a practical quantum advantage remains to be proven.

challenges

- **need to cool photon sources and detectors:** but at relatively reasonable temperatures between 2K and 10K, requiring lightweight cryogenic systems (unless also cooling the whole photonic circuit).
- **not yet scalable in number of operations:** due to probabilistic character of quantum gates and the efficiency of photon sources in most paradigms.
- **non-deterministic cluster states** and two-photon interactions.
- needs **delay lines** and **optical switches.**
- **heat generated by phasers:** increasing cooling budget.
- **photon detectors efficiency** is too low, at 89% with PsiQuantum.
- **photon losses** must be contained in nanophotonic circuits.

variations

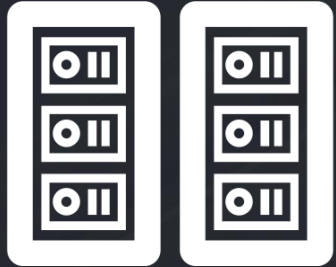
- **encoding:** direct variables qubits (DV), continuous variables (CV) qubits, multimode photon encoding.
- **MBQC** (measurement based quantum computing) and **FBQC** (fusion-based quantum computing).
- **BS/GBS:** programmable Boson sampling and Gaussian boson sampling.
- **hybrid approaches:** spin-optical quantum computing (SPOQC) with quantum dots spin qubits (Quandela), hybrid atom-photon qubits.
- **classical photonic models:** coherent Ising models, photonic waveguide arrays and interferometric systems.

path to scalability

- **efficiency:** improve photon sources efficiency, determinism and indistinguishability, improve photon detectors efficiency (SNSPD and PNRD).
- **cluster states:** generate large cluster states, with or without heralding.
- **interactions:** improve fusion efficiency in FBQC.
- **losses:** large-scale and low-losses optical switches and wave guides, reduce photon losses in nanophotonic circuits thanks to higher precision manufacturing and new materials.
- **energy:** create low-heating phasers to minimize power consumption.
- **nanophotonics:** heterogeneous nanophotonic circuits (III-V + silicon).
- **classical control speed:** particularly with FBQC models.

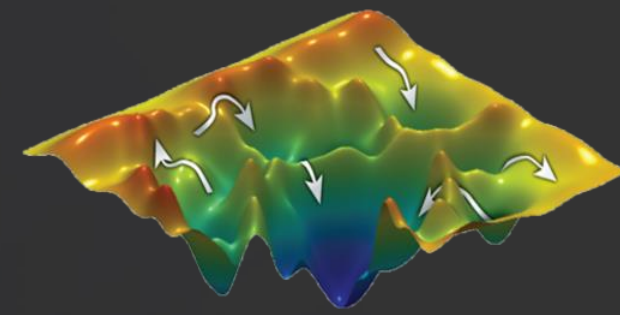
Figure 465: highlights, challenges, variations and path to scalability of photon qubits. (cc) Olivier Ezratty, 2022-2024.

EuroQCS-Spain



MareNostrum 5 ACC - BullSequana XH3000, Xeon Platinum 8460Y+ 32C 2.3GHz, NVIDIA H100 64GB, Infiniband NDR

Rpeak 249.44 PFlop/s, Top500 Rank: 8



Superconducting qubits Coherent Quantum Annealer

10 qubits – Q3 2025

Upgrade path: two different upgrades

First one Q3 2026

Second one Q3 2027



EuroHPC
Joint Undertaking

Quantum Annealing

2-local Ising Hamiltonian initialization

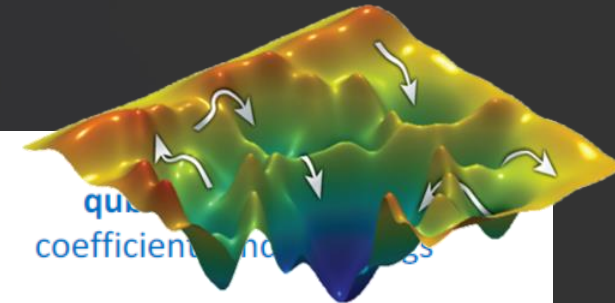
defines h_i and J_{ij} and set all σ_i^z at +1

$$\mathcal{H}_P = \underbrace{\sum_{i=0}^N h_i \sigma_i^z}_{\text{net qubits energy longitudinal interactions}} + \underbrace{\sum_{i<j}^N J_{ij} \sigma_i^z \sigma_j^z}_{\text{qubits connections energy longitudinal field}}$$

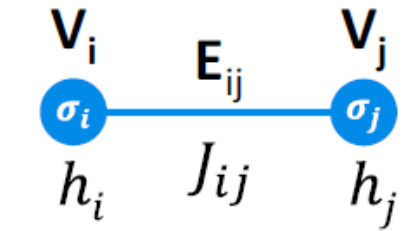
quantum annealing process
increases $B(s)$ and decreases $A(s)$ gradually

$$\mathcal{H}_S(t) = \underbrace{\mathcal{H}_P \frac{B(s)}{2}}_{\text{final Hamiltonian}} + \underbrace{\mathcal{H}_n(t)}_{\text{unknown effect of noise}} - \underbrace{\frac{A(s)}{2} \sum_{i=0}^N \sigma_i^x}_{\text{initial Hamiltonian}}$$

Ising model Hamiltonian → \mathcal{H}_P
effect from the variation of a transverse field → $A(s)$
trivial initial state all qubits at +1 in x direction → σ_i^x



quantum annealing process
coefficients and noise



problem variables

- h_i linear coefficient (bias) on qubit usually discretized
- J_{ij} coupling between vertices V_i and V_j discretized and implemented with couplers non zero values limited by coupling topology

problem unknowns

- σ_i^z qubits values : +1 or -1 (« spin orientation »)
- σ_i^z and σ_i^x are Pauli operators

annealing time operators

- t time
- t_f total annealing time, about $5\mu s$
- s fraction of annealing time= t/t_f
- $A(s)$ tunneling energy at anneal fraction s reduced over time as a $\Gamma(t)$ transverse magnetic field applied to all qubits is reduced
- $B(s)$ problem Hamiltonian energy at anneal fraction s increases over time during annealing

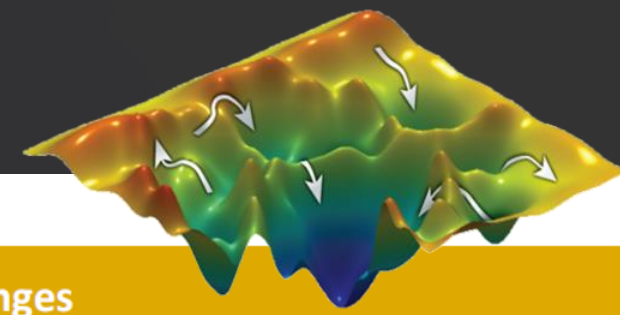
qubits topology

- V_i vertices containing qubit i
- E_{ij} edge connecting qubits i and j

system energy

- \mathcal{H}_P initial system Hamiltonian
- $\mathcal{H}_n(t)$ system noise Hamiltonian
- $\mathcal{H}_S(t)$ total Hamiltonian

Quantum Annealing



quantum annealing key takeaways

highlights

- **mature development tools offering:** D-Wave hybrid solver.
- **large number of software startups:** particularly in Japan and Canada.
- **cloud availability:** quantum annealers are available in the cloud by D-Wave and Amazon Web Services.
- **case studies:** greatest number of well documented case studies in many industries although still at the proof-of-concept stage.
- **near quantum advantage:** in some situations.
- **highly integrated DC qubit control** integrated in the chip (SFQ).

challenges

- **only one operational commercial vendor, D-Wave.**
- **computing high error rate.**
- **most commercial applications are still at the pilot stage and not production-grade scale, but they are closer than gate-based use cases.**
- **no generic operational proof of quantum advantage.**
- **need to improve qubit connectivity to improve embeddings.**

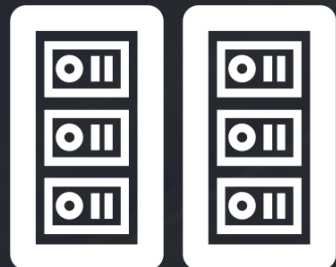
variations

- **hybrid quantum analog-digital architectures:** to solve specific problems, not generic.
- **digital annealing** ala Fujitsu.
- **photonic coherent Ising machines.**

path to scalability

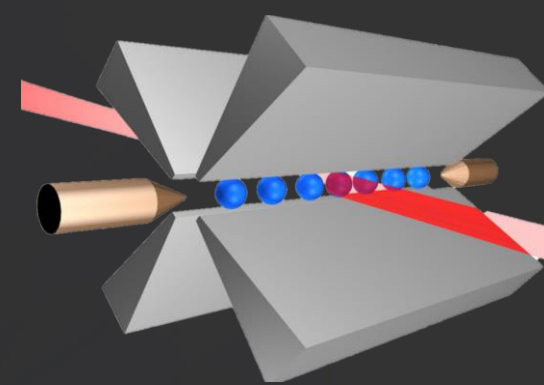
- **better qubit connectivity.**
- **noise reduction.**
- **error mitigation.**

EuroQCS-Poland



Altair - CH121L V5 Liquid-Cooled, Xeon Platinum 8268
24C 2.9GHz, Infiniband EDR

Rpeak 5.88 PFlop/s, Top500 Rank: 250



Trapped Ions digital quantum computer
20 qubits Q3 2025



EuroHPC
Joint Undertaking

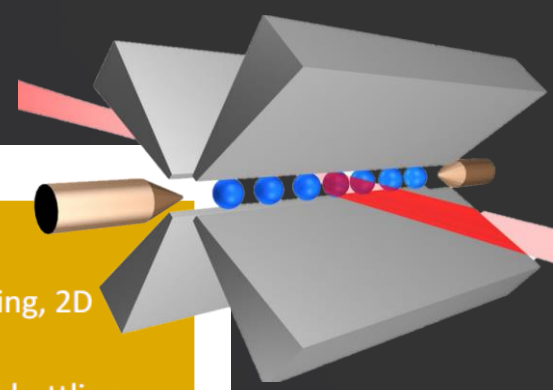


CINECA

 **QUANTUM
COMPUTING LAB**

Trapped Ions Quantum Computers

trapped ions qubits key takeaways



highlights

- **first two-qubit gate fidelities reaching 99.9%** (Quantinuum, Oxford Ionics).
- **first logical qubits** above break-even.
- **high ratio between coherence time and gate time:** supports deep algorithms in number of gate cycles.
- **low qubits variability** given the ions are all the same.
- **entanglement** possible between all qubits on 1D architecture which speeds up computing, avoiding SWAP gates.
- requires some cryogeny at **4K to 10K**.
- **QPU interconnect** can directly use photon entangled resources.

challenges

- **unproven scalability options beyond 60 qubits** (ions shuttling, 2D architectures, photon interconnect, micro-Penning traps).
- **slow computing:** due to long quantum gate times and ions shuttling which may be problematic for deep algorithms in a FTQC regime despite better qubit many-to-many connectivity at small scale.
- **two-qubit gate times** increase with ion distance in some laser-driven 1D and 2D settings.
- **many-to-many connectivity** works only at small scale.
- **control signals variability:** microwave, lasers, etc.
- **ions heating phenomenon:** it is not yet explained yet and really contained.

variations

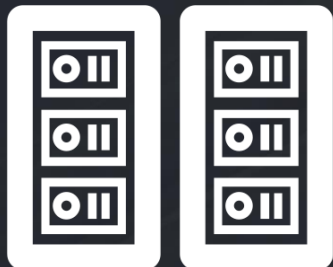
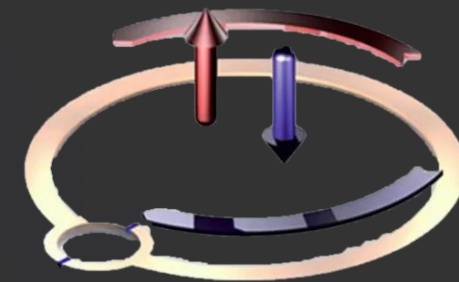
- **microwave/DC drive** instead of laser drive.
- **connectivity:** many-to-many within zones and ions shuttling between zones.
- **dual species** like ytterbium + barium for computing and cooling.
- **Rydberg ion qubits** for avoiding phonon and heating effect.
- **hybrid neutral atoms-ions** platforms.

path to scalability

- **2D QCCD** and ions shuttling.
- **QCCD tiling** (Universal Quantum).
- **multi modules** ion traps with intermodules ions shuttling.
- **multi-layer ion traps** to enable long-range microwave based entanglement.
- **photonic interconnect** to entangle qubits from different QPUs.

Figure 408: highlights, challenges, variations, and path to scalability of trapped ions qubits. (cc) Olivier Ezratty, 2022-2024.

Euro-Q-EXA



SuperMUC-NG - ThinkSystem SD650, Xeon Platinum
8174 24C 3.1GHz, Intel Omni-Path

Rpeak 26.87 PFlop/s, Top500 Rank: 50



Superconducting Digital Quantum Computer
54 qubits – Q3 2025
Upgrade path: 150 qubits Q4 2026

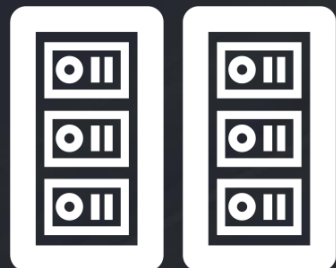


EuroHPC
Joint Undertaking

Selected IQM Radiance Machine
<https://www.meetiqm.com/products/iqm-radiance>

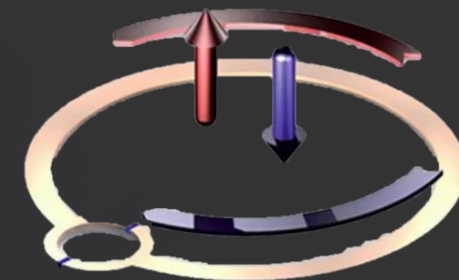
IQM

LUMI-Q



Karolina, GPU partition - Apollo 6500, AMD EPYC 7763 64C 2.45GHz, NVIDIA A100 SXM4 40 GB, Infiniband HDR200

Rpeak 9.08 PFlop/s, Top500 Rank: 135



Superconducting Digital Quantum Computer with unique star topology
24 qubits – Q3 2025

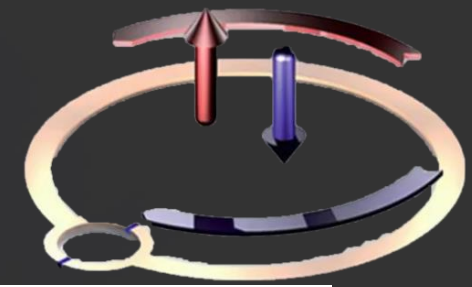
Selected IQM Custom («Radiance Star») Machine



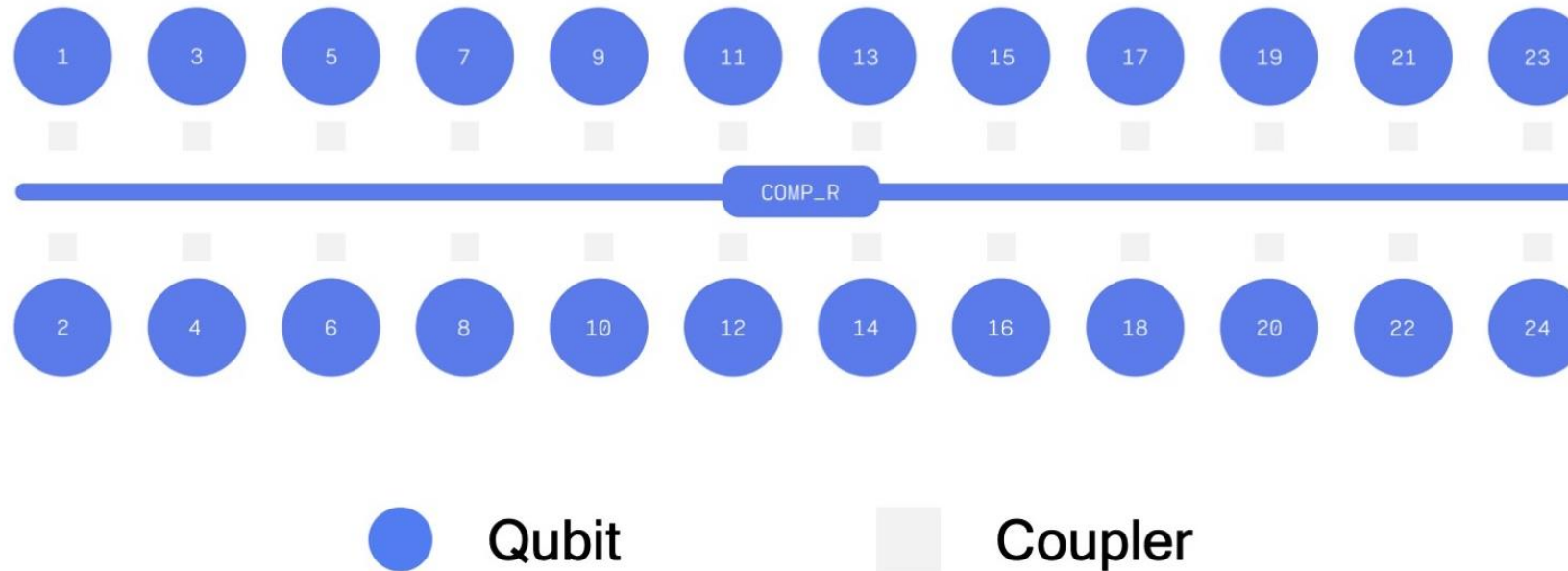
EuroHPC
Joint Undertaking

IQM

Radiance Star Topology



IQM Star 24



Integrating HPC and QC

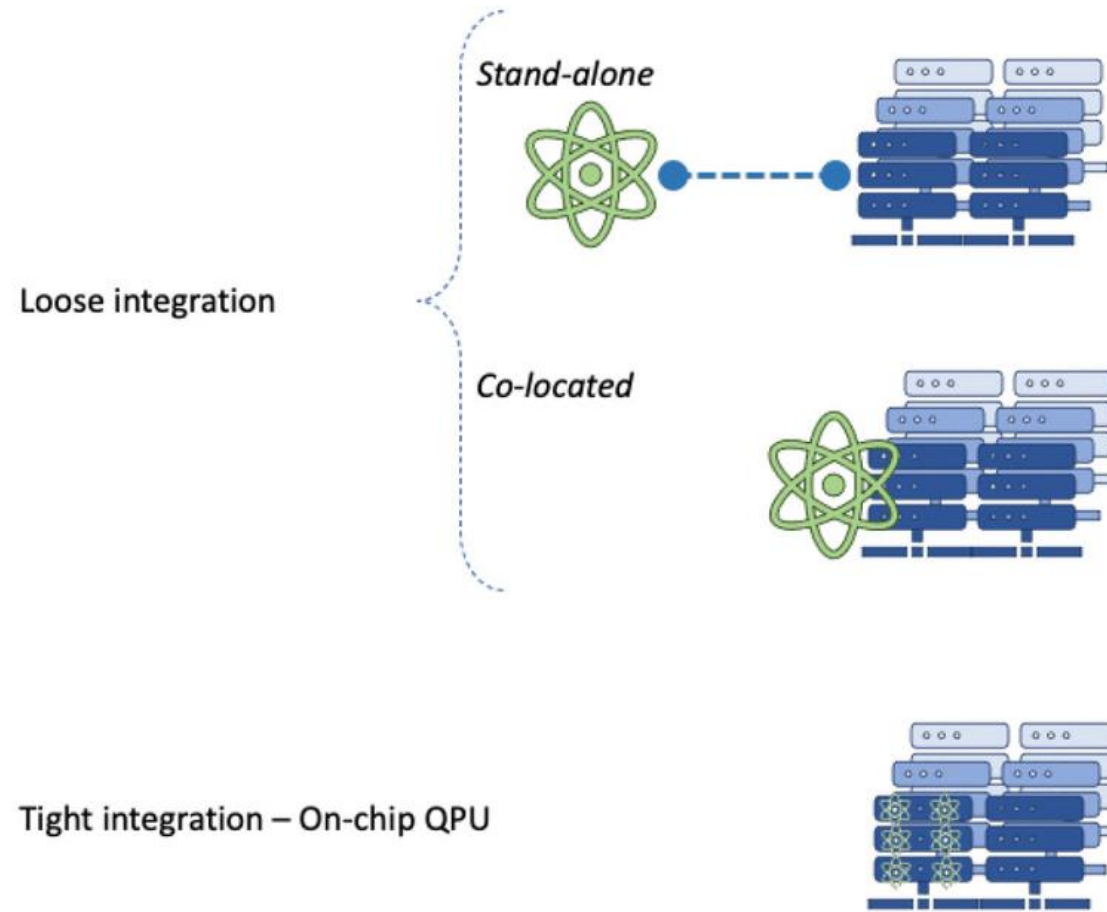


Figure 2. Representation of different levels of integration of QC systems with classical systems (tight or loosely coupled)

ETP4HPC White Paper: < QC | HPC > Quantum for HPC → <https://www.etp4hpc.eu/white-papers.html#quantum>

Integrating HPC and QC

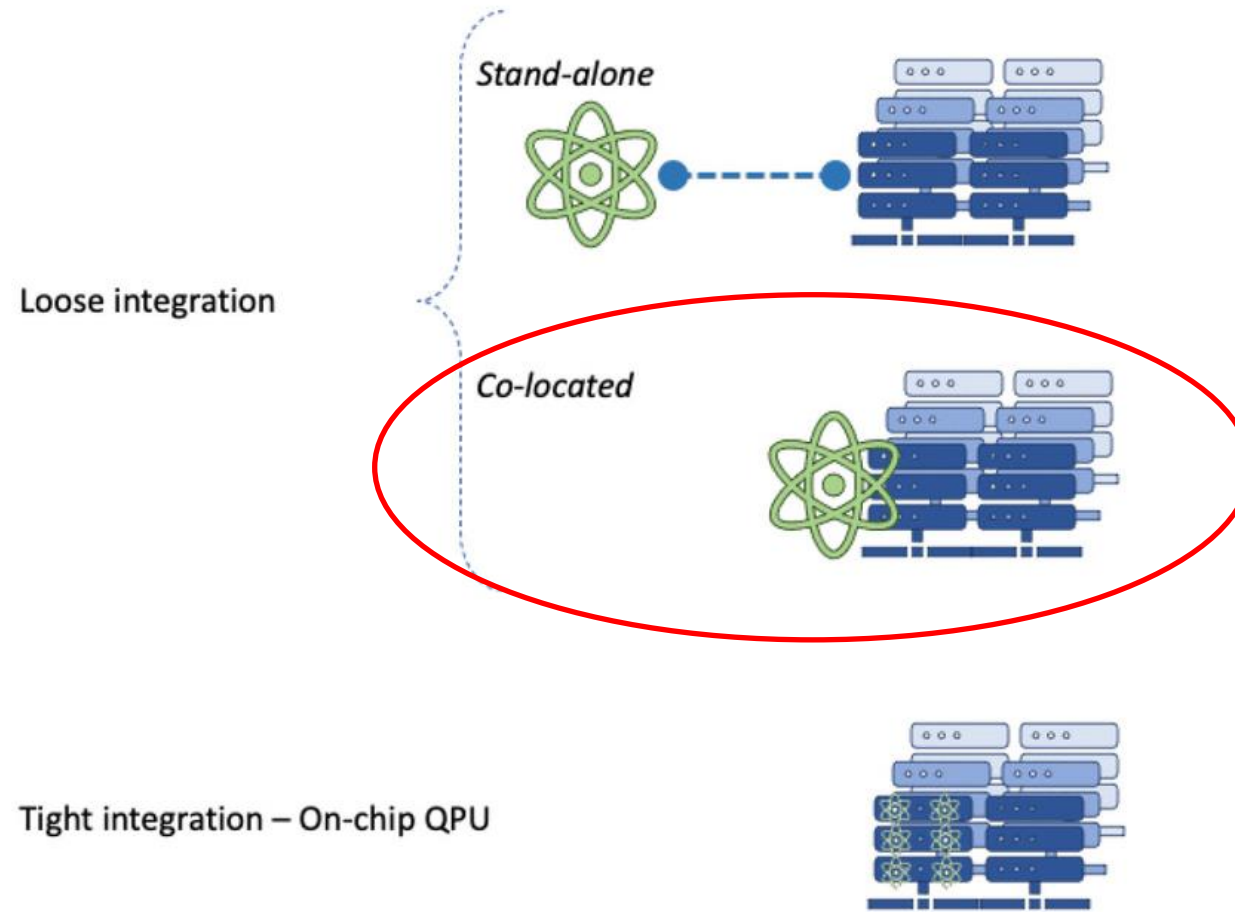


Figure 2. Representation of different levels of integration of QC systems with classical systems (tight or loosely coupled)

ETP4HPC White Paper: < QC | HPC > Quantum for HPC → <https://www.etp4hpc.eu/white-papers.html#quantum>

Integrating HPC and QC

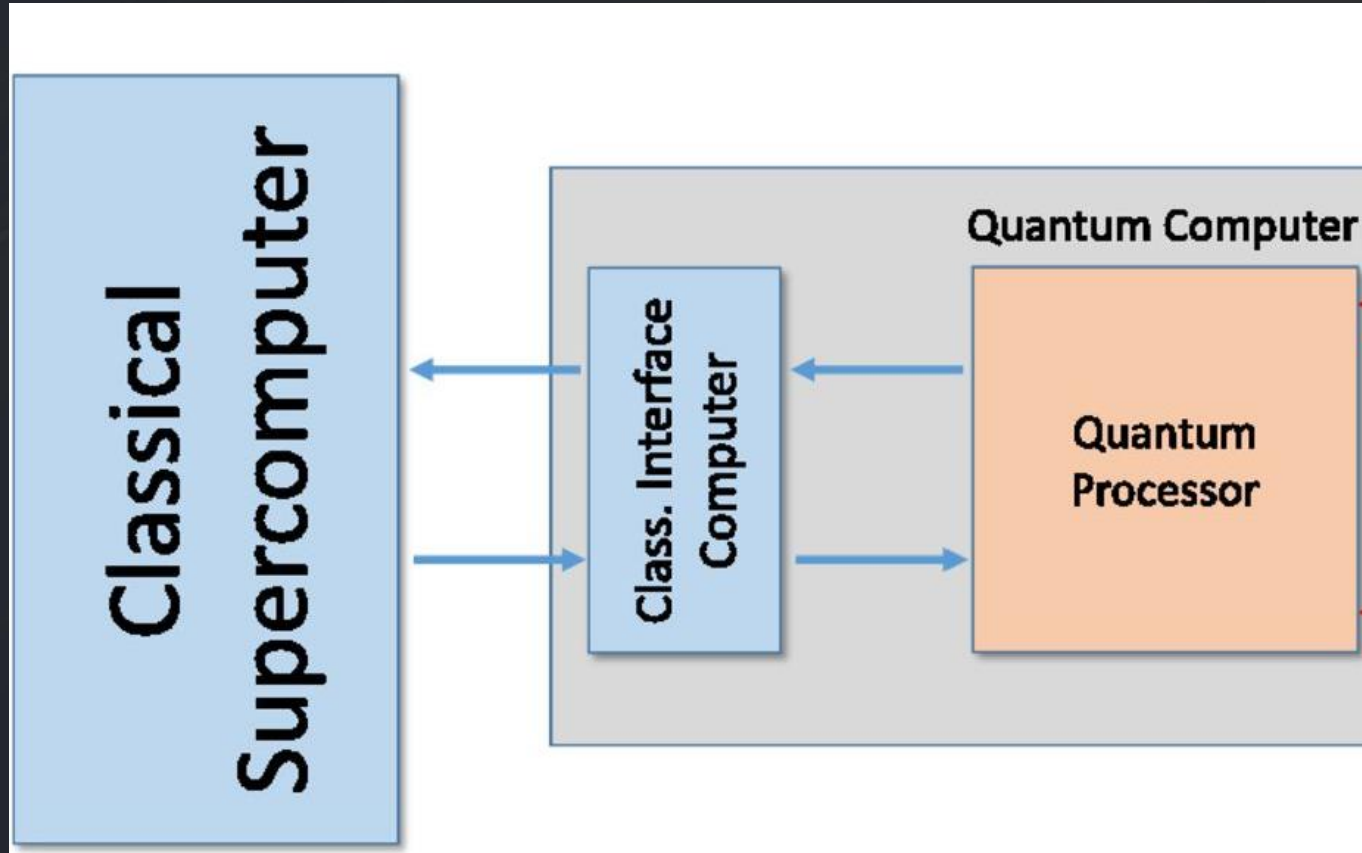


The Hardware part



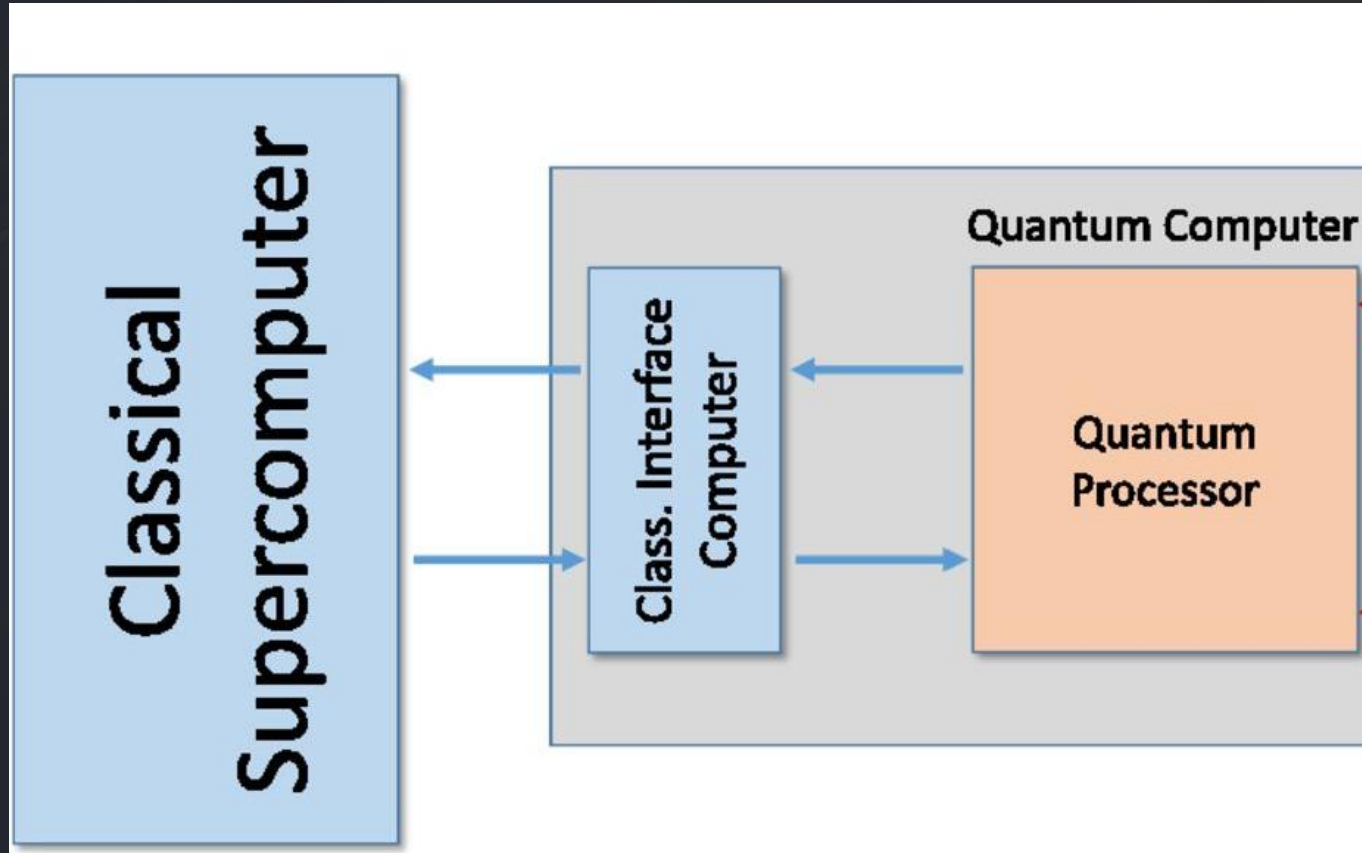
- Beginners: Connecting the qc to a node
 - A commercial qc usually is set up to be connected to a classic computer via an Ethernet cable – easy part!

The Hardware part



- Beginners: Connecting the qc to a node
 - A commercial qc usually is set up to be connected to a classic computer via an Ethernet cable – easy part!
- Advanced: Hijack the connection
 - To achieve a tighter connection and eliminate unnecessary latencies, one could also consider connecting the HPC node directly to the QPU (without going through the control computer present in the QC)

The Hardware part



- Beginners: Connecting the qc to a node
 - A commercial qc usually is set up to be connected to a classic computer via an Ethernet cable – easy part!
- Advanced: Hijack the connection
 - To achieve a tighter connection and eliminate unnecessary latencies, one could also consider connecting the HPC node directly to the QPU (without going through the control computer present in the QC)
 - This means installing firmware and operating systems for the QC on the HPC node, making it a de facto control system for the QPU

The Software part



- Beginners: Use the QC without HPC
 - Usually the vendors that produce QC also develop SDKs that can talk to the control computer and consequently to the QPU
 - Installing and using such software is step 0 for integration

The Software part



- Beginners: Use the QC without HPC
 - Usually the vendors that produce QC also develop SDKs that can talk to the control computer and consequently to the QPU
 - Installing and using such software is step 0 for integration
- Advanced: Use the QC as a part of an HPC job
 - SDKs provided by vendors often do not include the use of MPI and/or CUDA to take advantage of HPC
 - One solution might be to explore existing software (Nvidia CUDA Quantum, Eviden Qaptiva)
 - Or work with the vendor to write a custom SDK

The Middleware part

```
#!/bin/bash
#SBATCH -A <account_name>
#SBATCH -p quantum_module
#SBATCH --time 00:10:00
#SBATCH -N 1
#SBATCH --gres=qpu
#SBATCH --job-name=my_batch_job

srun ./my_quantum_executable.x
```

- Beginners: Exclusive allocation
 - Exclusive usage of the QPU – other jobs have to wait
 - Control over the whole computation, not single shots (good for VQA, not for Error Mitigation)

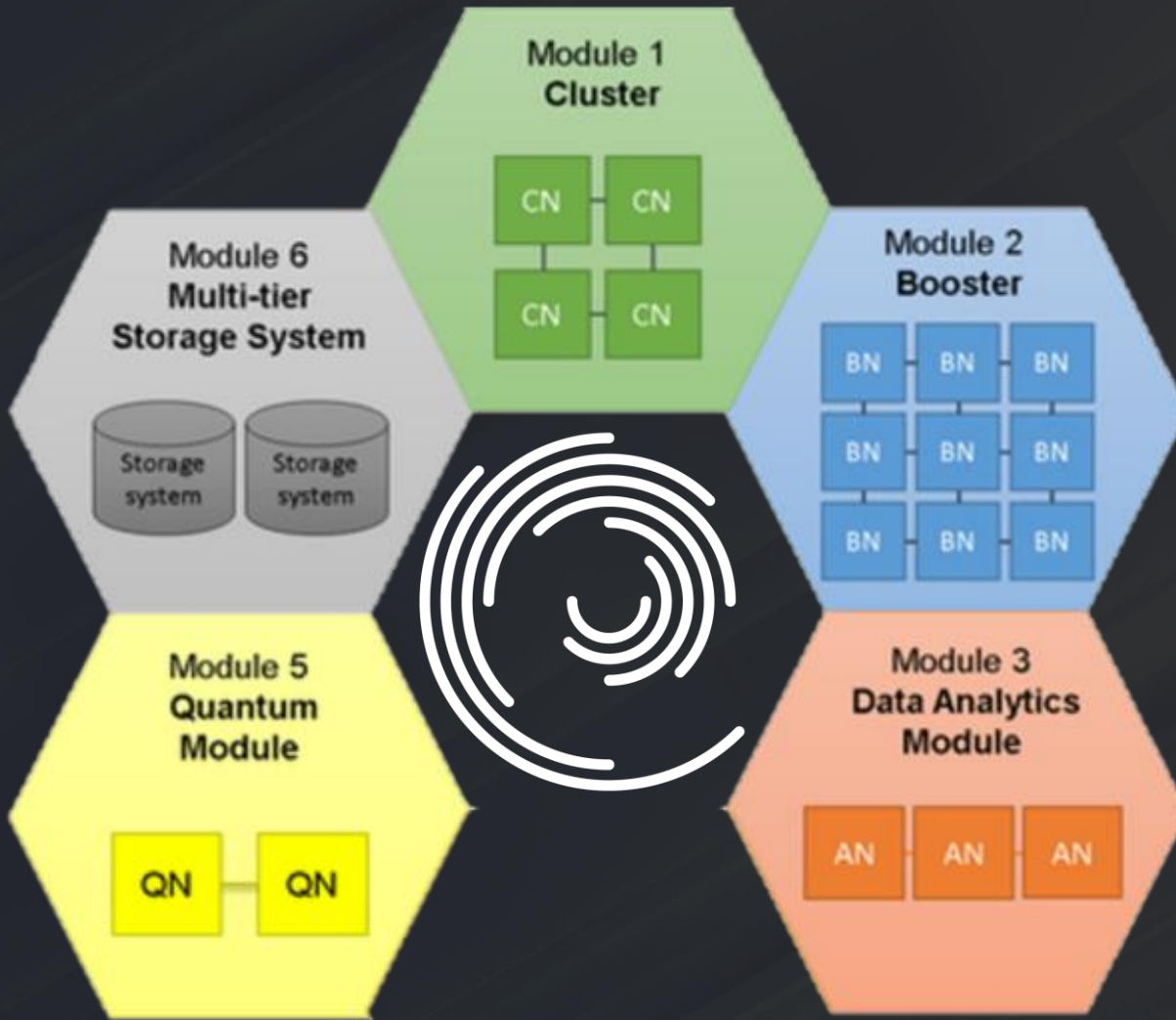
The Middleware part

```
#!/bin/bash
#SBATCH -A <account_name>
#SBATCH -p quantum_module
#SBATCH --time 24:00:00
#SBATCH -N 10
#SBATCH --gres=qpu
#SBATCH --gres=gpu:4
#SBATCH --job-name=my_batch_job

mpirun -np 10 ./my_hybrid_executable.x
```

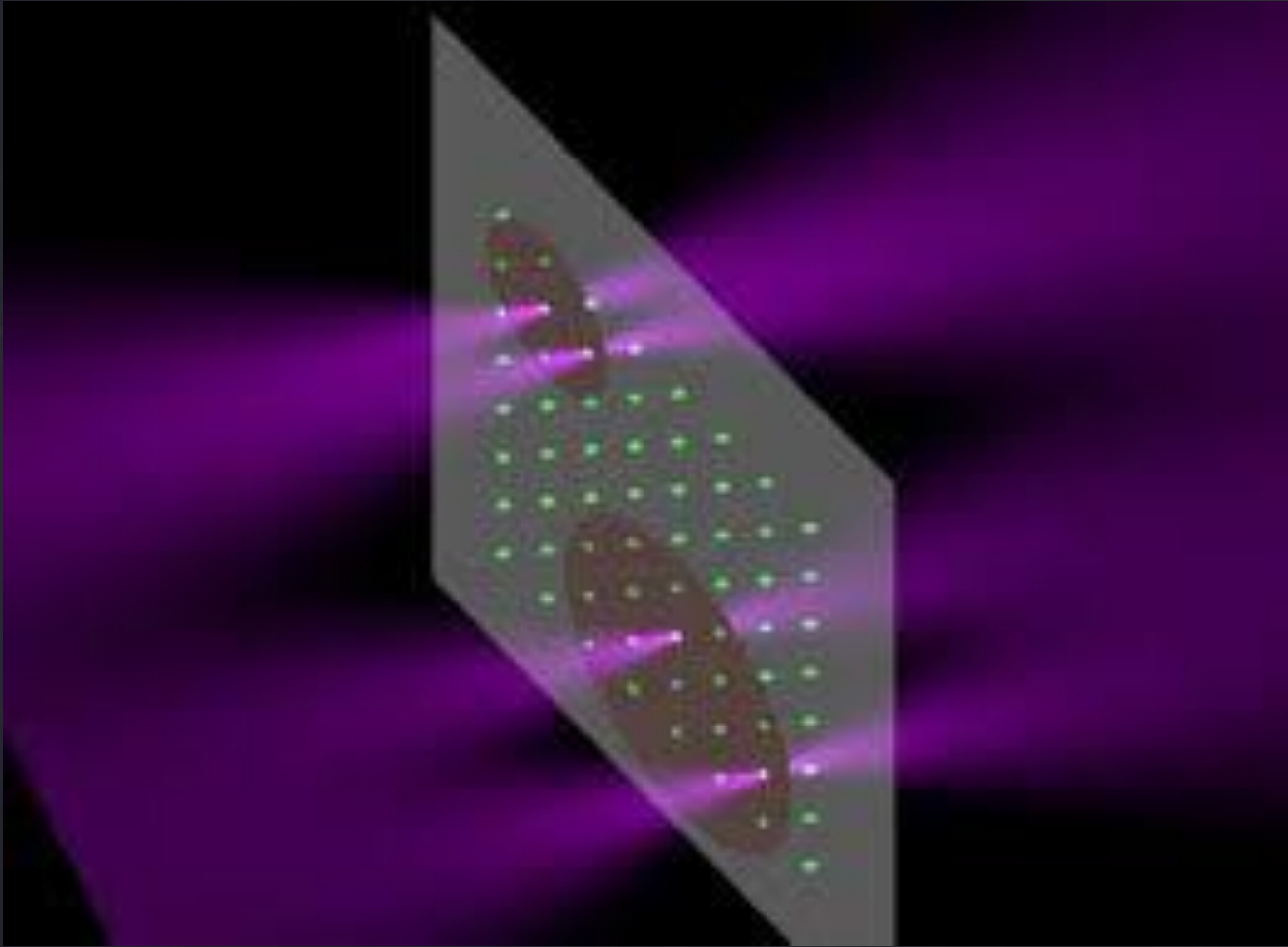
- Beginners: Exclusive allocation
 - Exclusive usage of the QPU – other jobs have to wait
 - Control over the whole computation, not single shots (good for VQA, not for Error Mitigation)

The Middleware part



- Beginners: Exclusive allocation
 - Exclusive usage of the QPU – other jobs have to wait
 - Control over the whole computation, not single shots (good for VQA, not for Error Mitigation)

The Middleware part



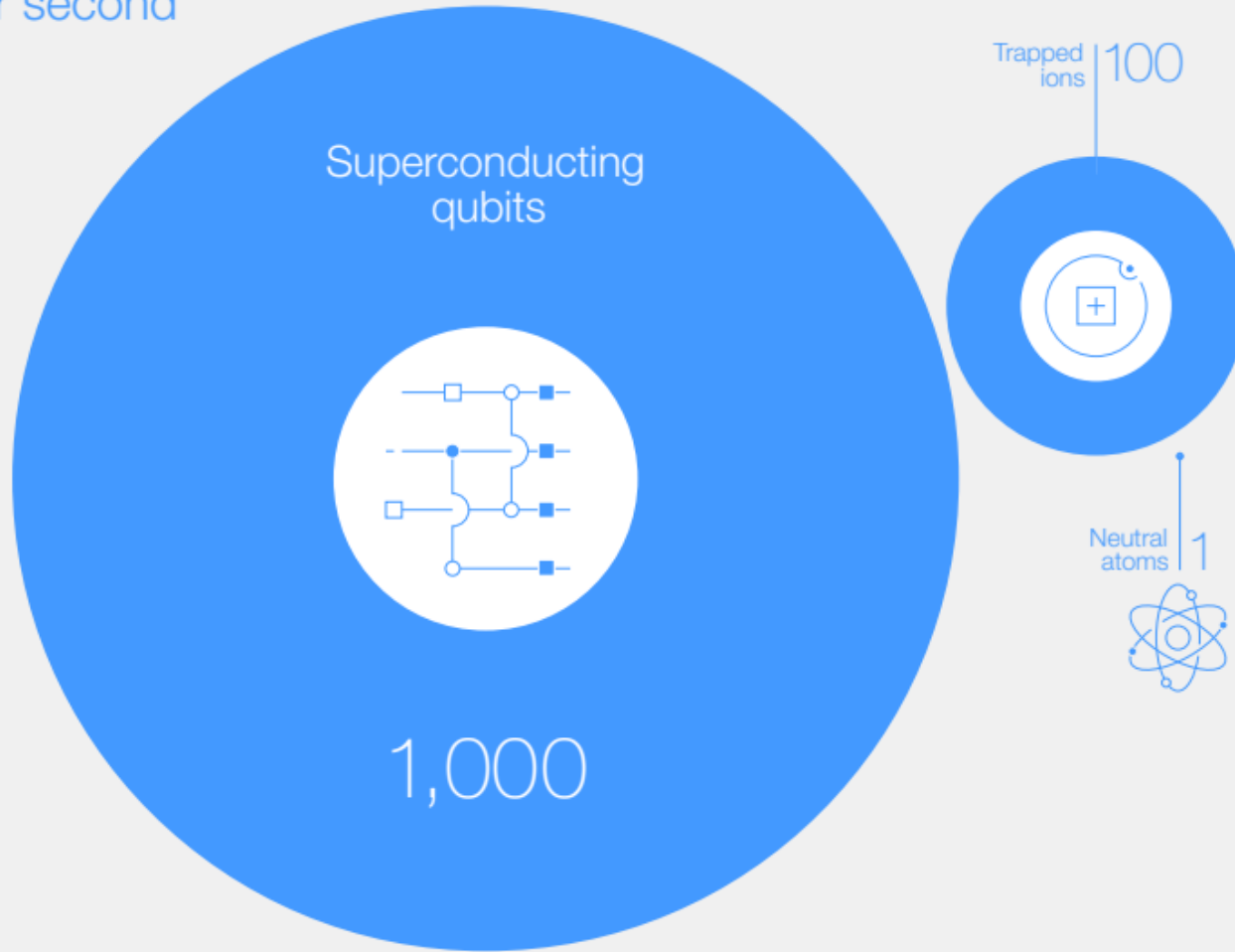
- Beginners: Exclusive allocation
 - Exclusive usage of the QPU – other jobs have to wait
 - Control over the whole computation, not single shots (good for VQA, not for Error Mitigation)
- Advanced: Efficient allocation
 - Non-exclusive usage – merging jobs

QUANTUM COMPUTING WITH NEUTRAL ATOMS

Loïc Henriët, Lucas Beguin, Adrien Signoles, Thierry Lahaye, Antoine Browaeys, Georges-Olivier Reymond and Christophe Jurczak

The Middleware part

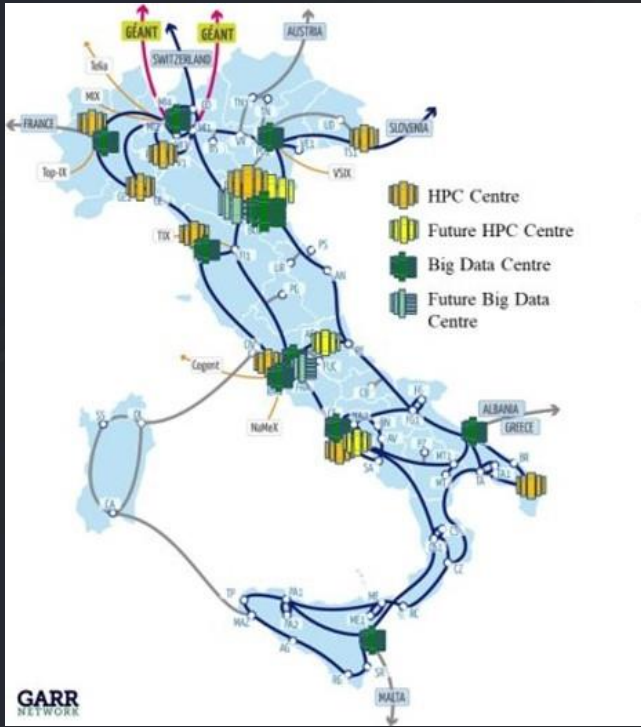
Calculations
per second



- Beginners: Exclusive allocation
 - Exclusive usage of the QPU – other jobs have to wait
 - Control over the whole computation, not single shots (good for VQA, not for Error Mitigation)
- Advanced: Efficient allocation
 - Non-exclusive usage – merging jobs
 - Control over the single shots
 - Shots frequency very low (neutral atoms, trapped ions) – Free the HPC resources during the QPU computation
 - Shots frequency very high (superconducting QC) – Be sure that your scheduler is able to catch the shots!

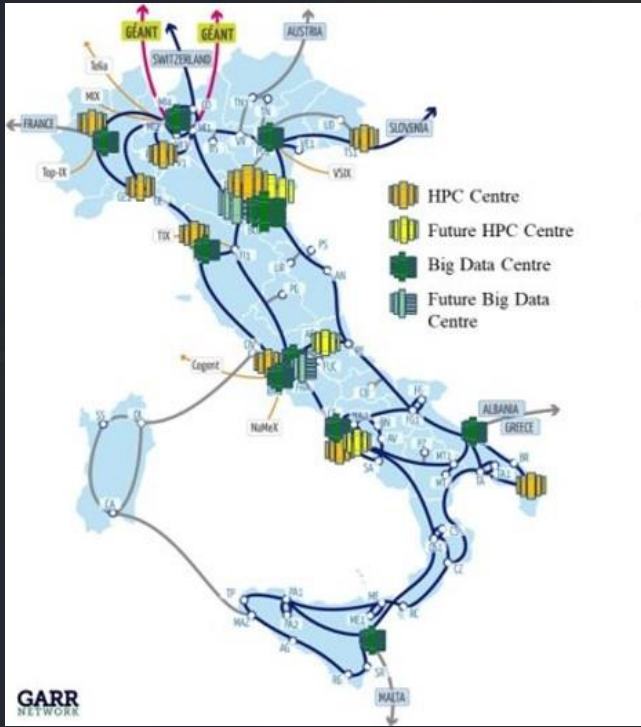
https://www3.weforum.org/docs/WEF_State_of_Quantum_Computing_2022.pdf

Italian and European QC Environment



 **Fondazione
ICSC**
Centro Nazionale di Ricerca in HPC,
Big Data and Quantum Computing

Italian and European QC Environment



 **Fondazione ICSC**
Centro Nazionale di Ricerca in HPC,
Big Data and Quantum Computing



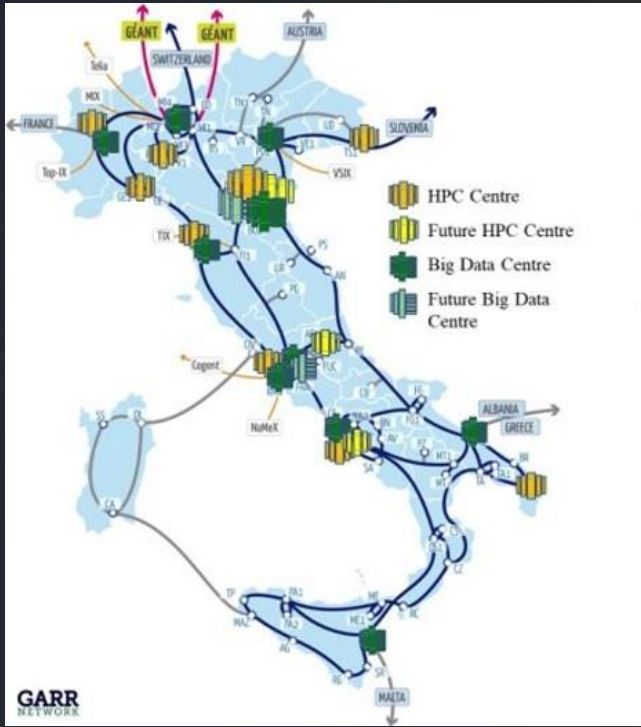
EuroHPC
Joint Undertaking



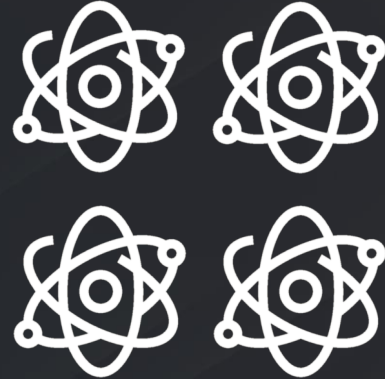
CINECA

 **QUANTUM
COMPUTING LAB**

Italian and European QC Environment



Fondazione ICSC
Centro Nazionale di Ricerca in HPC,
Big Data and Quantum Computing



QUANTUM
COMPUTING
AND
SIMULATION
CENTER



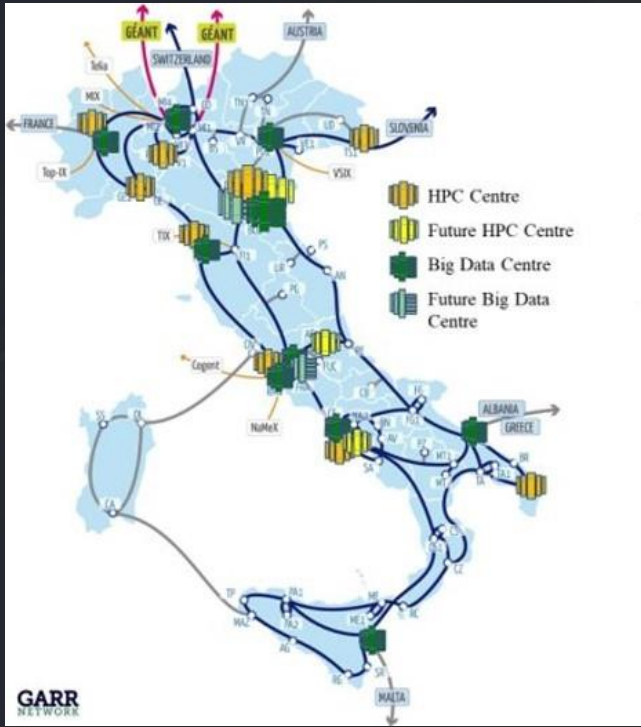
EuroHPC
Joint Undertaking



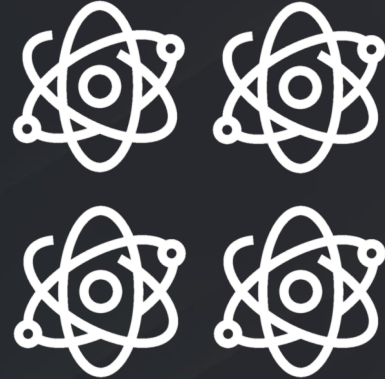
CINECA

**QUANTUM
COMPUTING LAB**

Italian and European QC Environment



Fondazione ICSC
Centro Nazionale di Ricerca in HPC,
Big Data and Quantum Computing



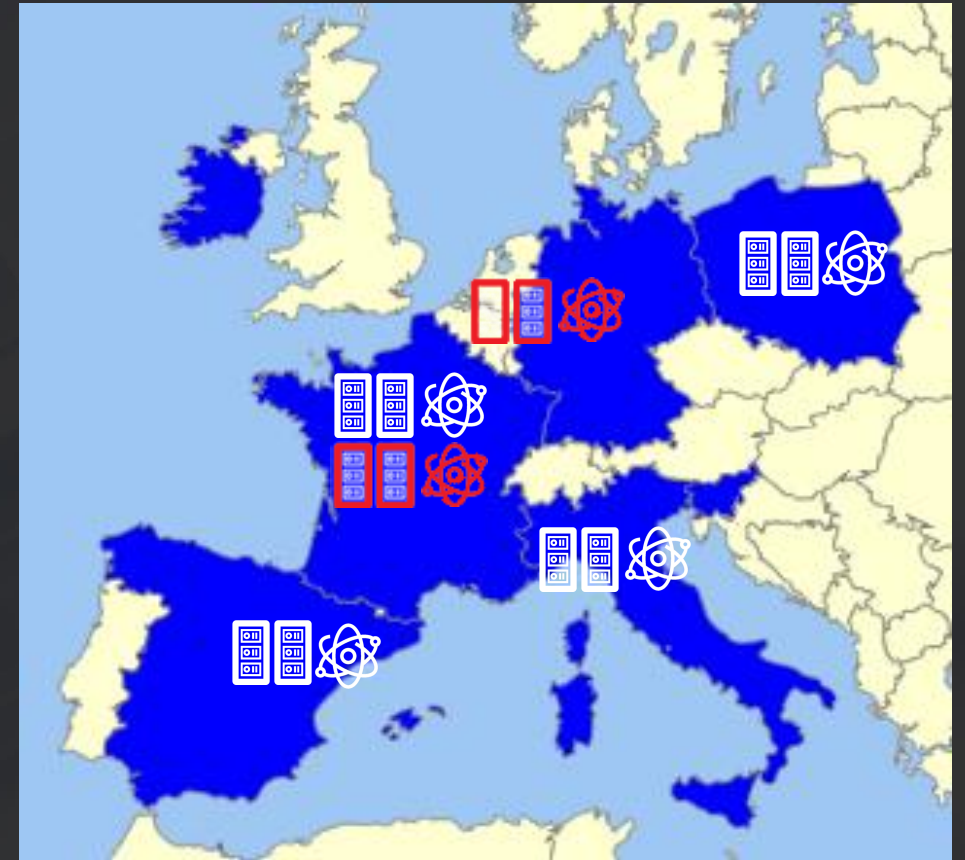
QUANTUM
COMPUTING
AND
SIMULATION
CENTER



EuroHPC
Joint Undertaking



<HPC|S> EuroQCS



CINECA

**QUANTUM
COMPUTING LAB**

Enjoy the Workshop!

Thank
you!

CINECA

 QUANTUM
COMPUTING LAB