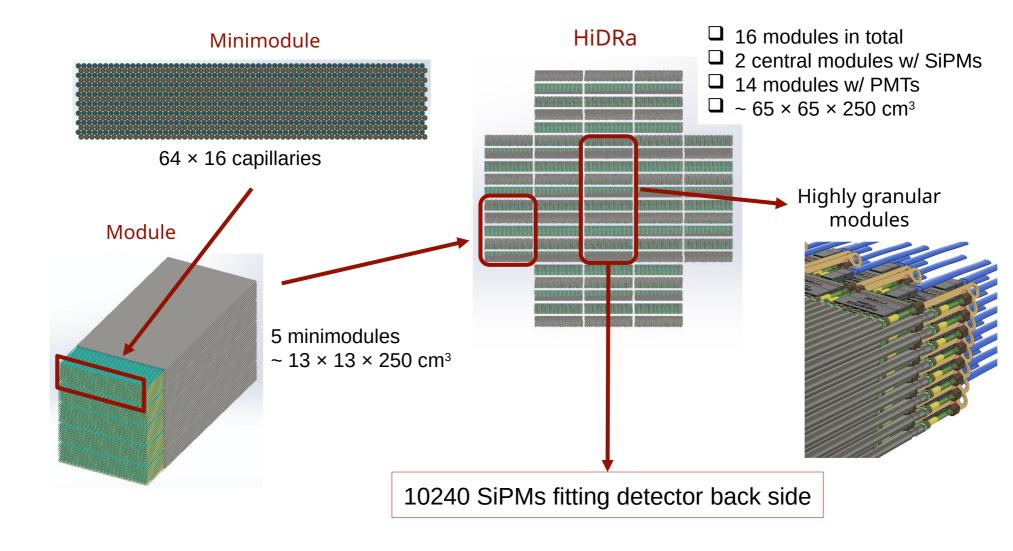
IDEA dual-readout calorimeter

RD_FCC referee meeting 26.07.2024

Roberto

Dual-Readout Calorimeter: Layout

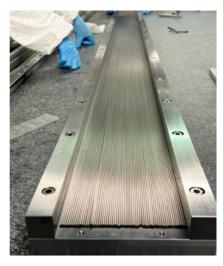


Construction technique



High quality tube selection:
Accurate measurement of thickness,
straightness, length, and internal diameter
(pass/fail test with fibre insertion)

Structure anchored to granite table for stacking layers of tubes





Vacuum + double-sided tape for tube handling



Glue dispensing and tube alignment and positioning





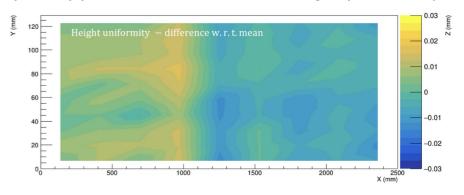
Construction technique and mechanical precision

Semi-automatic system for planarity measurement: 90 measurements per minimodule



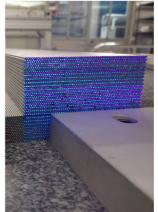


O(10 µm) precision on minimodule height (calor2024)



Production started in November 2023: 38/80 minimodules assembled First test beam with 36 modules planned in August 2024 (PMT readout only)

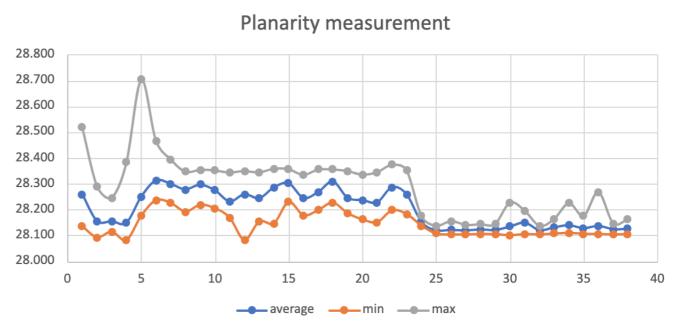


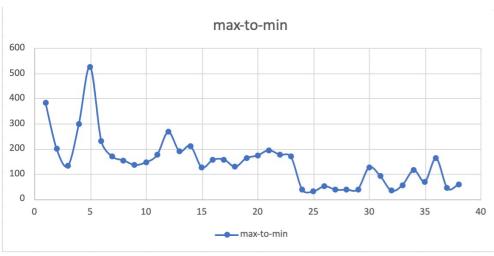


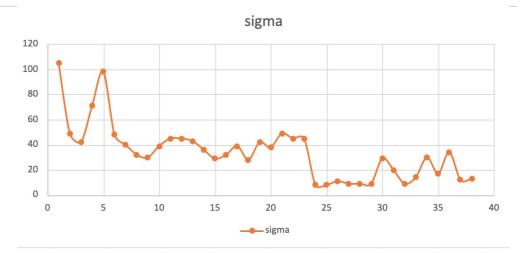
Planarity measurements

Pretty stable results

Well within requirements







Status

After some delay, production in steady state: rate ~ 8 minimodules / month

Target: finish ~ end 2024 / beg. 2025

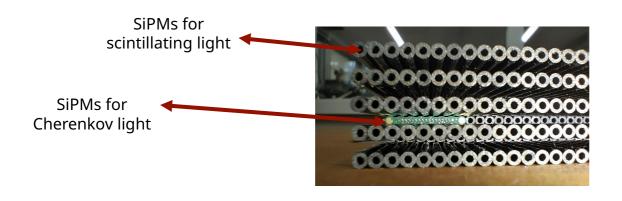
Tube and fibre quality quite good but rejection close to threshold (5%)

- Fibres → ok (replacement at no cost)
- Negotiations ongoing for tube "refurbishing"

Fibre: limiting factor in assembly procedure

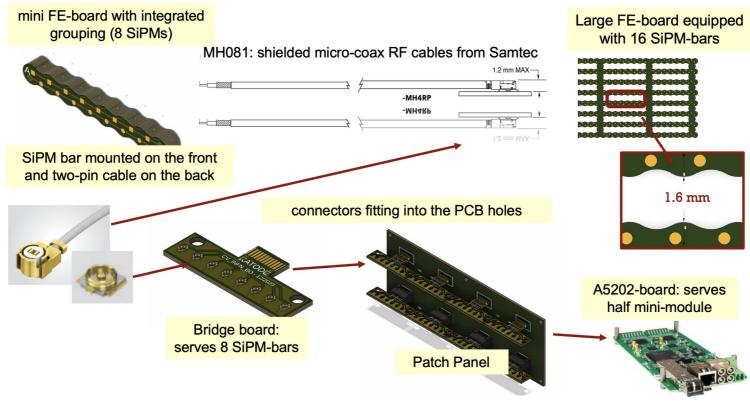
- 1) fibre cutting → automatic machine now in operation
- 2) fibre insertion (?) at present 1 minimodule / 12-16 h

Integration of highly granular modules



High precision required for SiPM alignment

PCB designed according to tube shape → self-alignment w/ fibres



Preproduction and first qualification

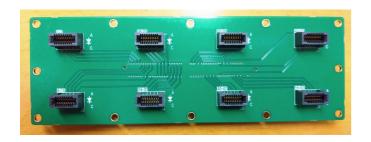
☐ Mini front-end board (40 prototypes)

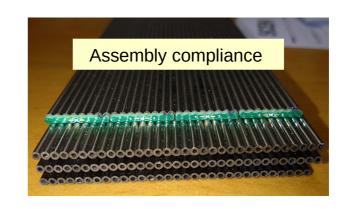


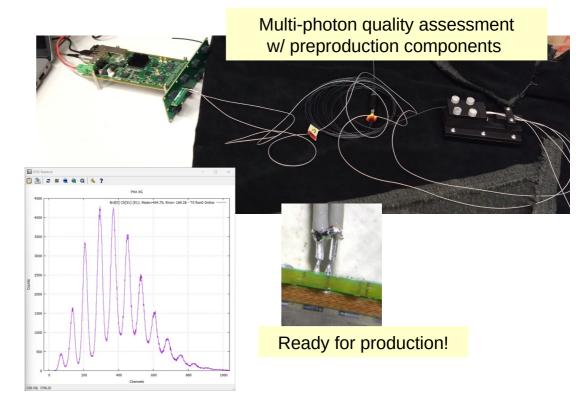
☐ Bridge board (10 prototypes)



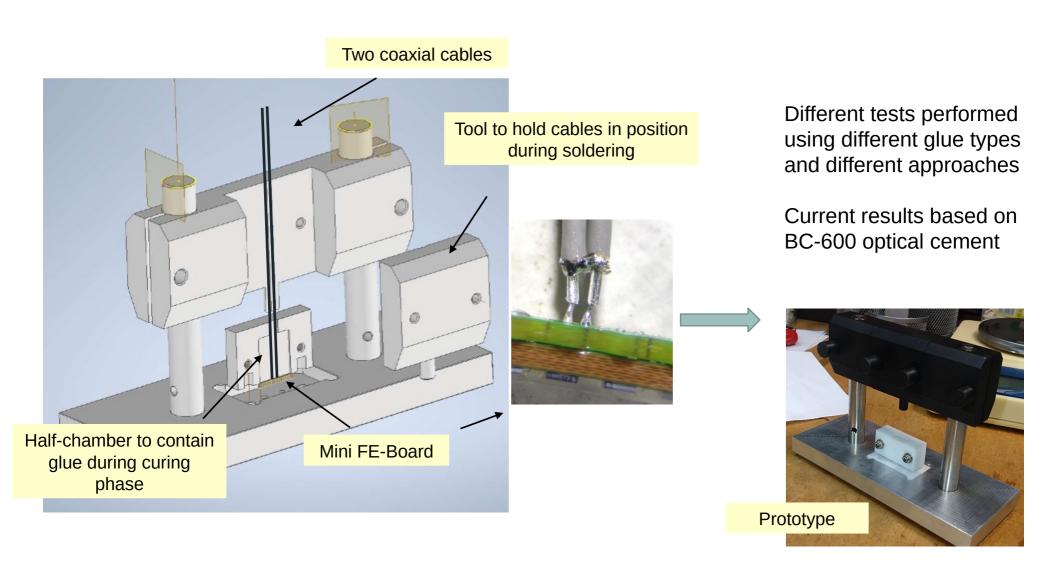
□ Patch panel (4 prototypes)







Mini FE-board: assembly station

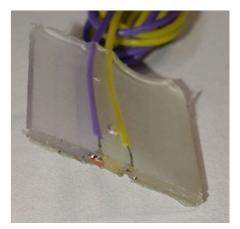


Different strategies tested with dummy components

- Strategy 1
 - Glue-chamber manufactured in Teflon
 - Glue filled with syringe
 - Tests w/ waiting time (from glue mix to displacement) up to 3 h
 - Glue curing time 24h

Final consideration: very difficult to fully control leakage and guarantee proper reference plane





Different strategies tested with dummy components

- Strategy 1
 - Glue-chamber manufactured in Teflon
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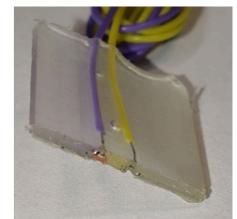
Final consideration: very difficult to fully control leakage and guarantee proper reference plane

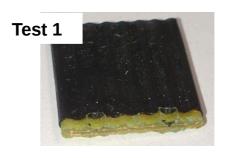


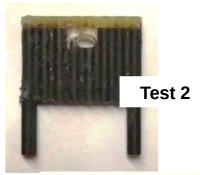
- 3D-printed components to obtain good reference plane
- Optimise 3D-component design and material
- Optimise gluing technique

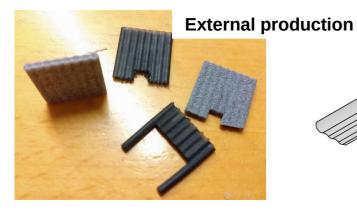
Final consideration: way to go

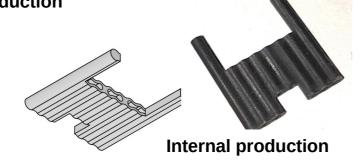


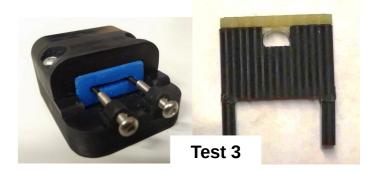












Schedule (high-granularity modules)

Procurement ongoing after some delay

SiPM delivery scheduled for week 36 (September 2)

Preproduction:

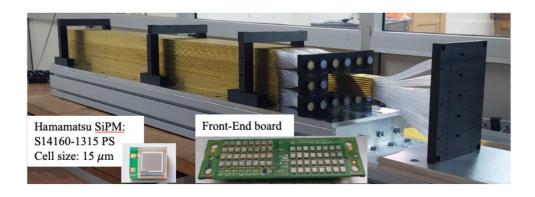
Mounting on PCBs within ~ end of October

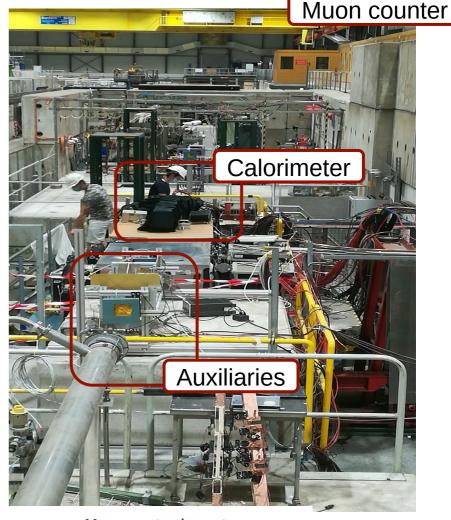
Fully qualified within ~ winter 2025

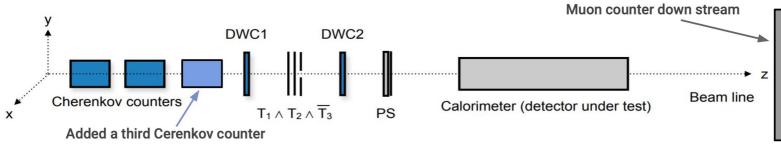
Beam tests in 2021 and 2023

CERN-SPS H8 beam line

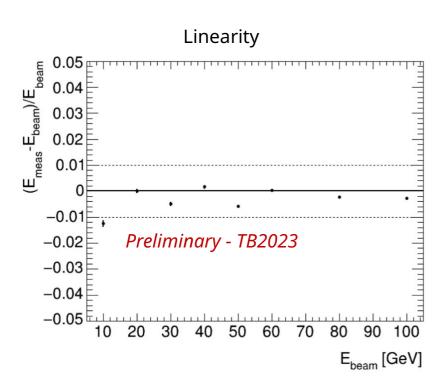
- □e⁺ beam in energy range of 10-100 GeV
- Energy and position scan
- Purity issues (critical in 2021)

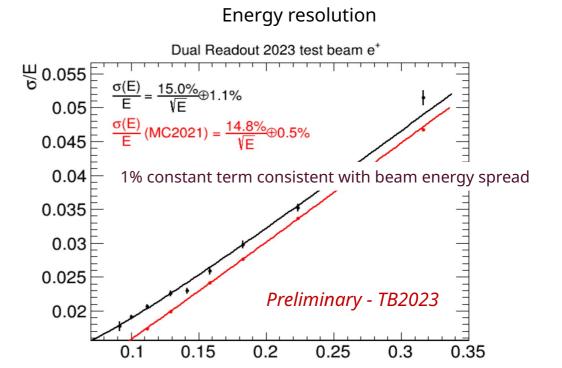






Final results





1/√E [GeV^{-1/2}]

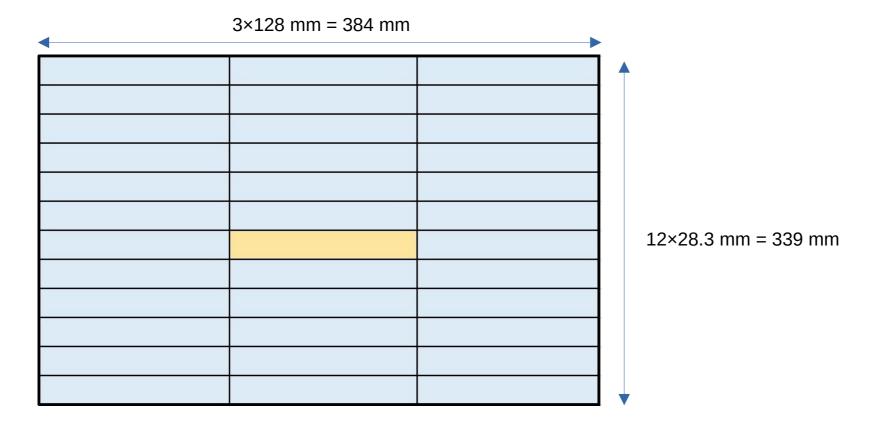
Results well in agreement with G4 simulations

Testbeam 2024

36 minimodules in 3×12 arrangement (+ integrate position measurement w/ ATLAS_PIX3 sensors)

PMT-only: 36 + 36 PMT signals to read out

Focus on: understand/assess calibration procedure, operation and G4 validation



Testbeam 2024 - timeline



~10 of 12 layers already piled up

35/36 modules ready, 1 more to be finalised with fibre loading

Mechanics to be finalised

Module will arrive at CERN on August 5th / 6th

1st week (August 7th →):

- Daq setup
- Elx checks

Last week (August 28th →):

- Physics measurements

Personnel

New people (part of ATLAS LAr Milano group) joining Milano group:

Leonardo Carminati Laura Nasella Ruggero Turra

Synergy

New proposal in CSN 5 for digital SiPM development (ASPIDES) informal feedback: well received

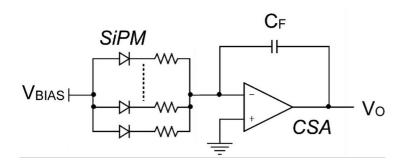
National coordinator: Lodovico Ratti

Collaboration: BA-BO-MI-NA-PD-PV-TIFP-TO

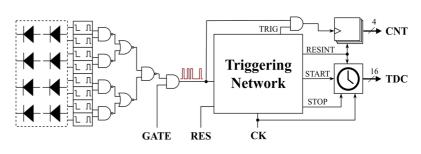
36 people, ~8 FTE

About dSiPMs

SiPMs: analogue signal proportional to number of fired cells, readout performed externally



Digital (CMOS) SiPMs: readout functionalities implemented in sensor substrate (e.g. binary counters, SPAD masking, TDCs ...)



M. Perenzoni et al. 2017 - IEEE JSSC

- CMOS SPAD arrays may offer different benefits:
 - Monolithic structure simplifies assembly for large area detectors
 - Front-end optimised to preserve signal integrity (especially useful for timing)
 - Easier linearisation and calibration direct digital output
 - Simplified DAQ → lower costs (at least for designs based on standard processes)

ASPIDES – proposta di sigla in CSN 5

Requests for 2025 (material only)

RD_FCC:

BO: Cavi, minuteria e materiale test elettronica dual readout 5 k€

MI: acquisto 2 schede readout spare per il dimostratore Hidra 15 k€

PV: schede di readout per moduli aggiuntivi 3 k€

PI: acquisto PMT con basi per integrazione prototipo con moduli di RD52 44 k€ → s.j.

HiDRa2:

BO: integrazione elettronica di front-end 15 k€

PV: allestimento stazione per incollaggio e saldatura cavi e connettori 15 k€

PI: acquisto PMT con basi per integrazione prototipo con moduli di RD52 44 k€ → s.j.

Summary

After some delay, production in steady state: rate ~ 8 minimodules / month

- Target: finish ~ end 2024 / beg. 2025
- Bottleneck: fibre loading

High-granularity modules

- SiPMs expected early September
- Mounting strategy tuned
- Preproduction qualification expected within 1Q 2024

HiDRa2 asked for one year program extension

Beam test with a (PMT-only) 36 minimodule setup → tune calibration procedure

Backup

26.07.2024 **21**

AtlasPix3





ATLASPix3 - Features

- ATLASPix3 general features
 - Depleted Monolithic Active Pixel Sensor (DMAPS)
 - HVCMOS technology
 - o full-reticle size **20×21 mm**² monolithic pixel sensor
 - TSI 180 nm process on 200 Ωcm substrate
 - o 132 columns of 372 pixels
 - o pixel size 50×150 μm²
 - breakdown voltage ~-60 V
 - o up to 1.28 Gbps downlink
 - 25 ns timestamping
 - designed by I. Peric at KIT
- INFN, KIT, China, UK collaboration

