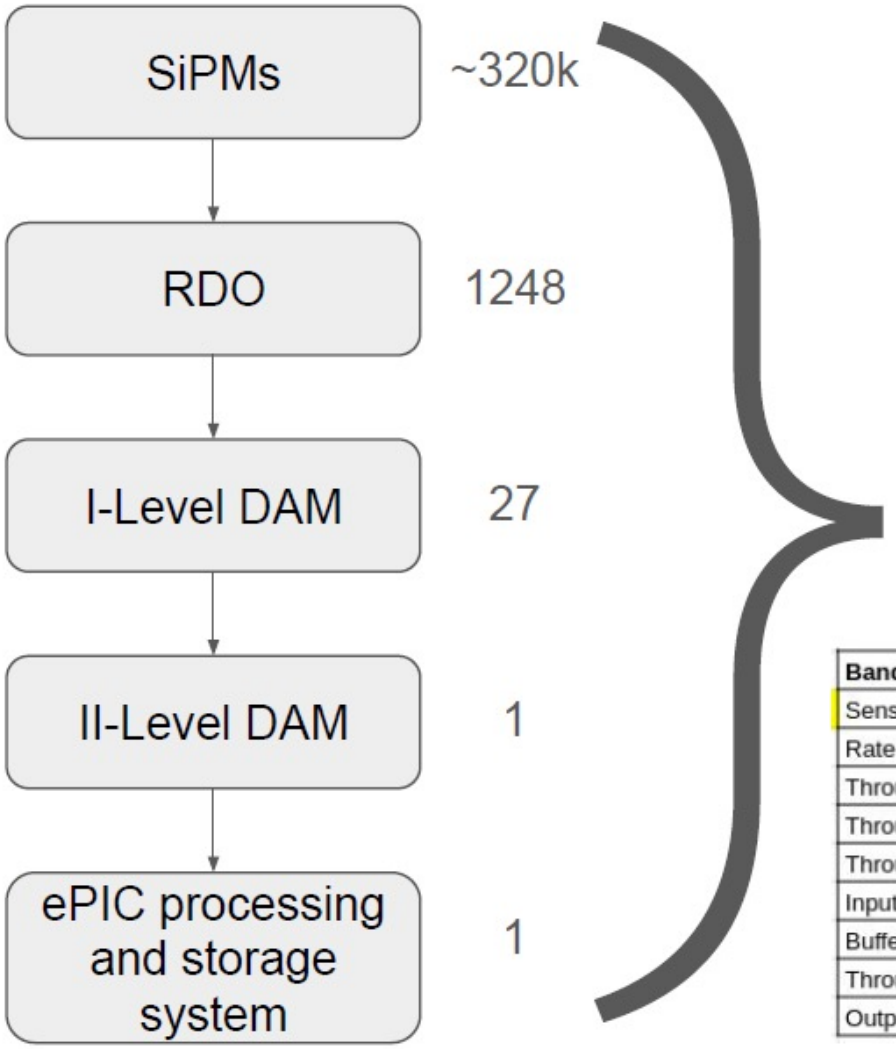
dRICH: data reduction on FPGA

Alessandro Lonardo

for the ePIC Roma1/2 team

Incontro ePIC con i referee INFN, Bologna 16 Luglio 2024

Analysis of dRICH Output Bandwidth



dRICH DAQ parameters	
RDO boards	1248
ALCOR64 x RDO	4
dRICH channels (total)	319488
Number of DAM L1	27
Input link in DAM L1	47
Output links in DAM L1	1
Number of DAM L2	1
Input link to DAM L2	27
Link bandwidth [Gb/s] (assumes VTRX+)	10
Interaction tagger reduction factor	1
Interaction tagger latency [s]	2,00E-03
EIC parameters	
EIC Clock [MHz]	98,522
Orbit efficiency (takes into account gap)	0,92

Bandwidth analysis		Limit
Sensor rate per channel [kHz]	300,00	4.000,00
Rate post-shutter [kHz]	55,20	800,00
Throughput to serializer [Mb/s]	34,50	788,16
Throughput from ALCOR64 [Mb/s]	276,00	
Throughput from RDO [Gb/s]	1,08	10,00
Input at each DAM I [Gbps]	50,67	470,00
Buffering capacity at DAM I [MB]	12,97	
Throughput from DAM I to DAM II [Gbps]	50,67	10,00
Output to each DAM II [Gbps]	1.368,14	270,00

Sensors DCR: 3 - 300 kHZ (increasing with radiation damage → with experiment lifetime).

Detector throughput: 14 - 1400 Gbps.

EIC beams bunch spacing:10 ns → bunch crossing rate of 100 MHz.

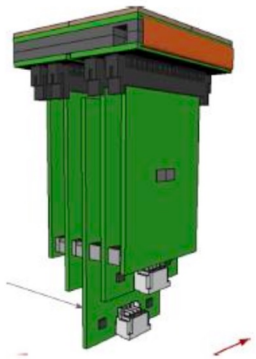
For the low interaction cross-section → one interaction every ~ 200 bunches → interaction rate of 500 kHz

Throughput Issue:

1. **Develop a dedicated sub-detector tagging relevant interactions.**
2. **This proposal.**

RDO and ePIC DAQ

P. Antonioli
https://indico.bnl.gov/event/20457/contributions/80658/attachments/49752/85138/20230914-DAQ.pdf



1248

- PDU: 1248
- RDO: 1248
- FEB: 4992

1248

I-level DAM (27)

FELIX

- 47 links to PDU
- 1 link to II-level DAM

27

in exp. hall, rack mounted

PC with 4 FELIX each (??)

27

II-level DAM (1)

FELIX

- 27 links to I-level DAM
- link from central ePIC [clock/trigger]

ePIC interaction tagger
able to reach our DAMS in 10 μs!

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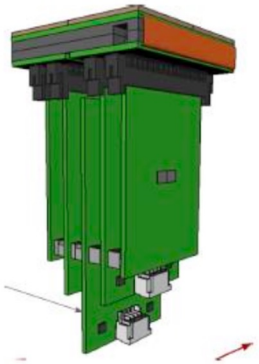

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Data reduction on FPGA

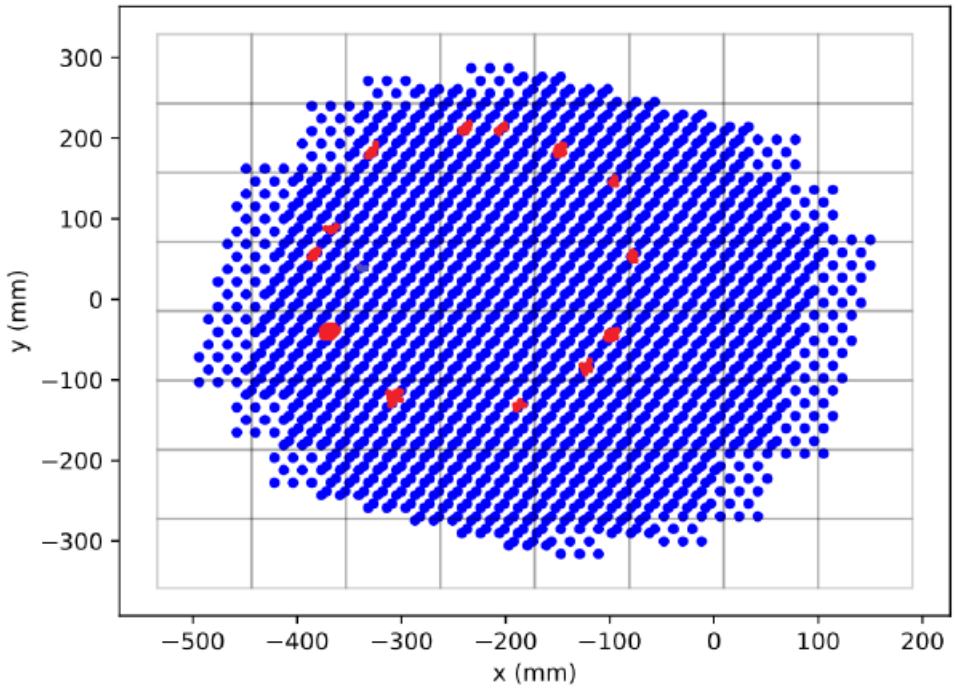
dRICH Data Reduction Stage on FPGA

- Objective: design of a data reduction stage for the dRICH with a ~100 data bandwidth reduction in DAM-I level output to DAM-II level input.
- Make exclusive use of DAQ components (Felix DAMs)
  - Add few DAM units wrt the bare minimum needed to readout the 1248 RDO links to implement a distributed processing scheme.
  - Integration with the Interaction Tagger (or other detectors) to boost performance and enable other features.
- Online Signal/Background discrimination using ML
  - Collecting datasets using data available from simulation campaigns
    - Background:
      - e/p with beam pipe gas
      - Synchrotron radiation
    - Merged: signal + e/p with beam pipe gas background (full)
    - SiPM Noise
      - DCR modelled in the reconstruction stage

dRICH Data Reduction Stage on FPGA

- Online Signal/Background discrimination using ML (continued)
  - Study of Inference Models
    - Restricting our study to inference models that can be deployed on FPGA with reasonable effort (using a High-Level Synthesis workflow)
      - MLP, CNN, GNN NN Models (HLS4ML)
      - BDT (Conifer)
    - Inference throughput (98.5 MHz) is the main concern.
    - HDL optimized implementation is an option.
    - Not necessarily ML-based.
  - Deployment on multiple Felix DAMs directly interconnected with the APE communication IPs.

Background: NN model Used in NA62 (actually one of them…)

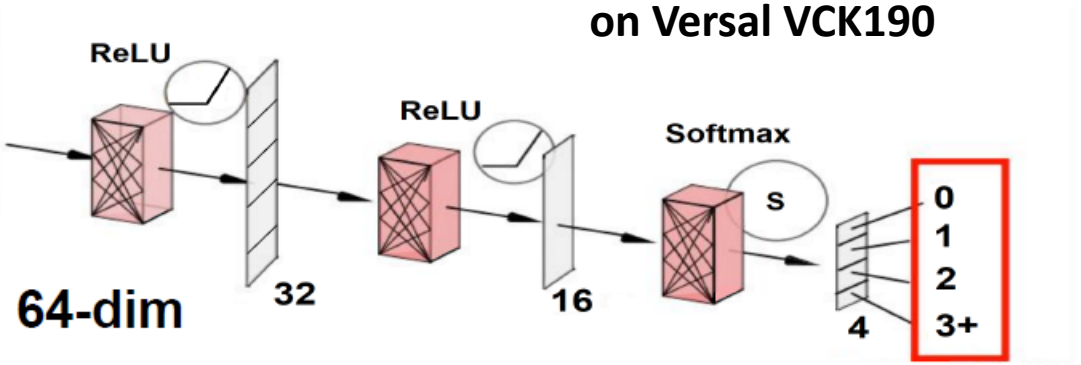


8 x 8 cells

Unrolled

hit-PMTs per cell

0
0
0
⋮
1
0
3
⋮
0
0



Number of rings

FPGA Resources:
LUT = 14%
Flip–Flop = 6%
DSP = 7%
BRAM = 3%
on Versal VCK190

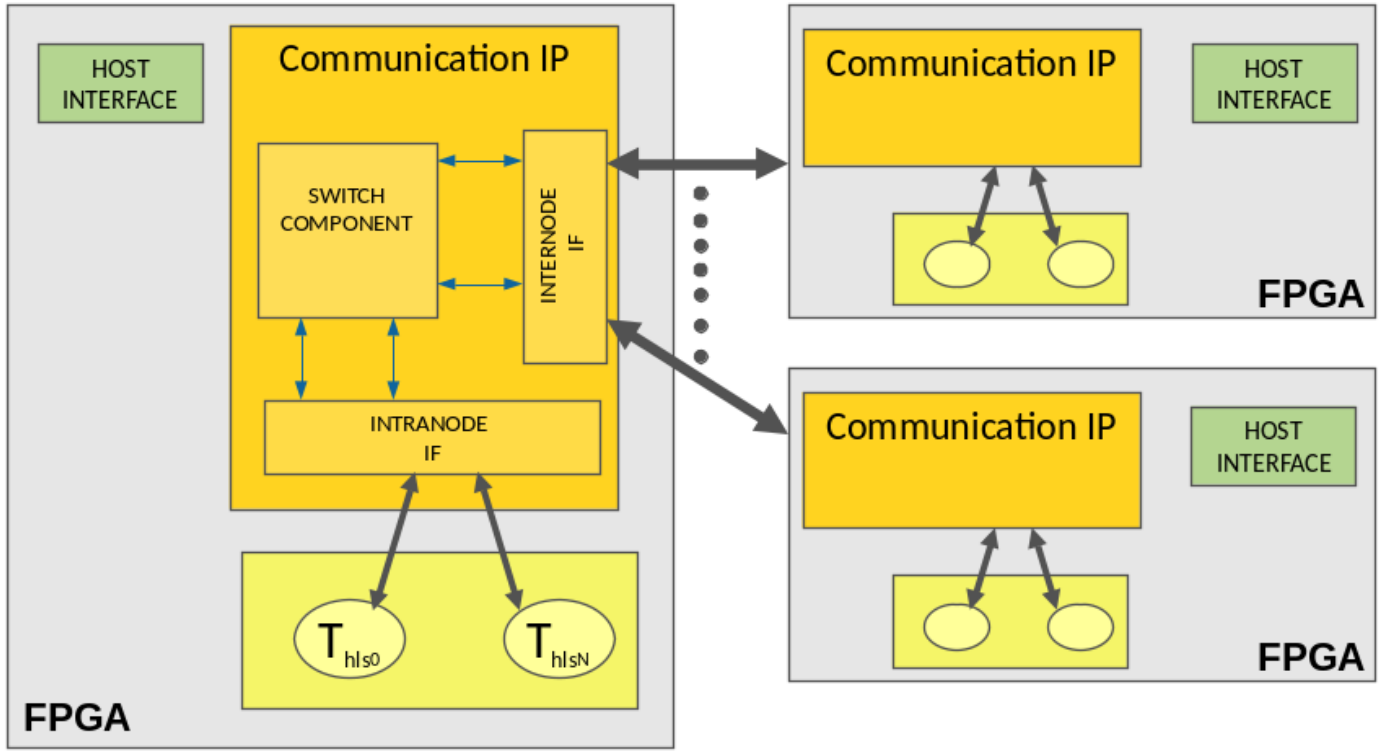
- **Encoding of the 1952 PMTs geometrical positions in the input layer.**

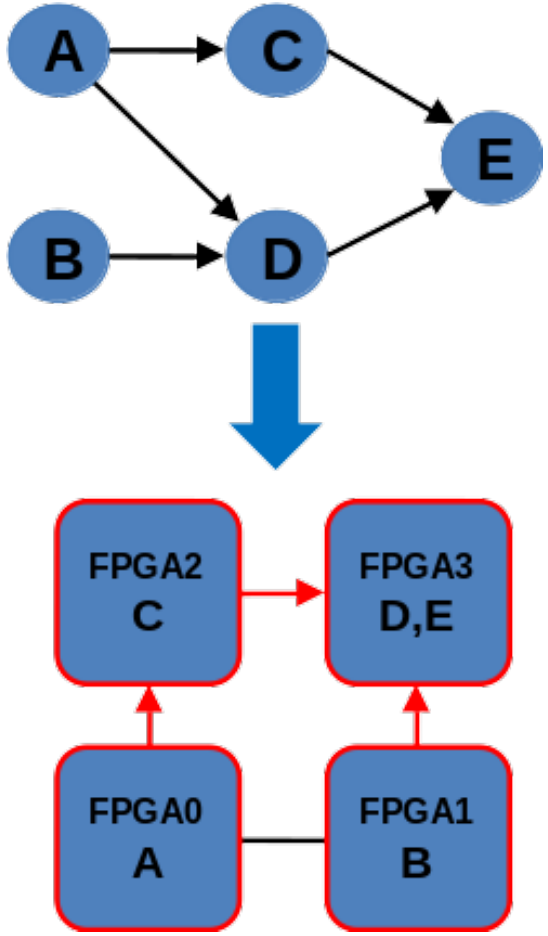
Performance (@300 MHz)

- **Avg. throughput: 21 MHz**
- **Latency: 160 ns**

Background: APEIRON Communication IP

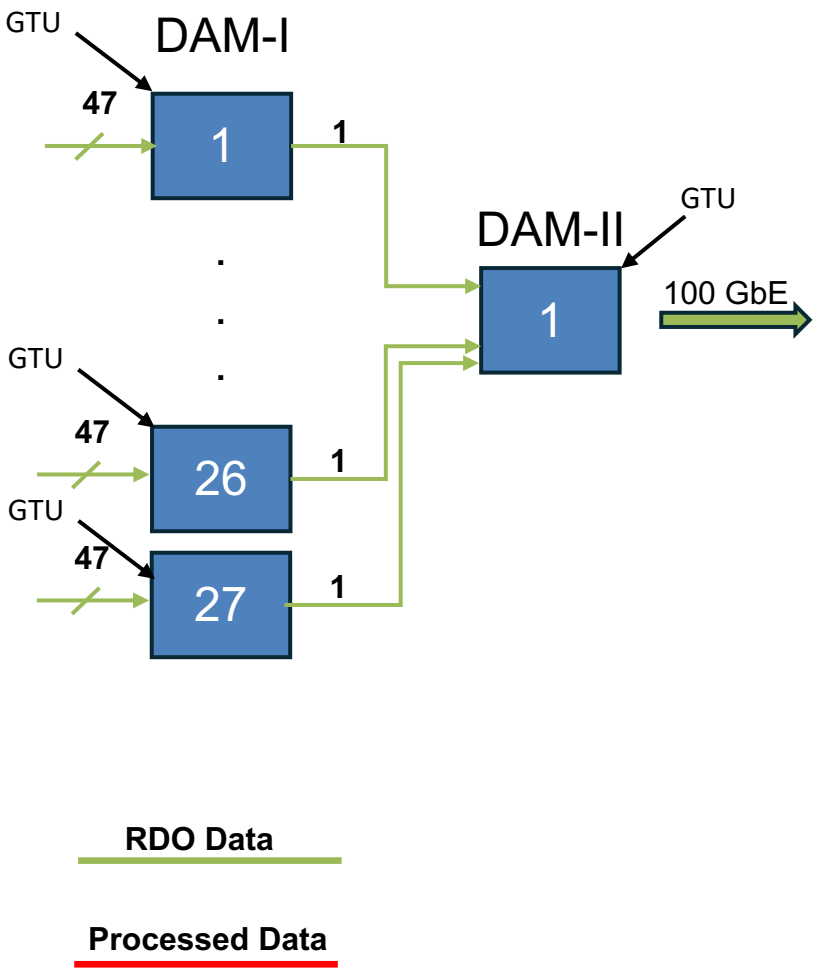
- INFN APE Lab has developed the IPs implementing a **direct network** that allows **low-latency** data transfer between HLS processing tasks deployed on the same FPGA (intra-node communication) and on different FPGAs (inter-node communication).

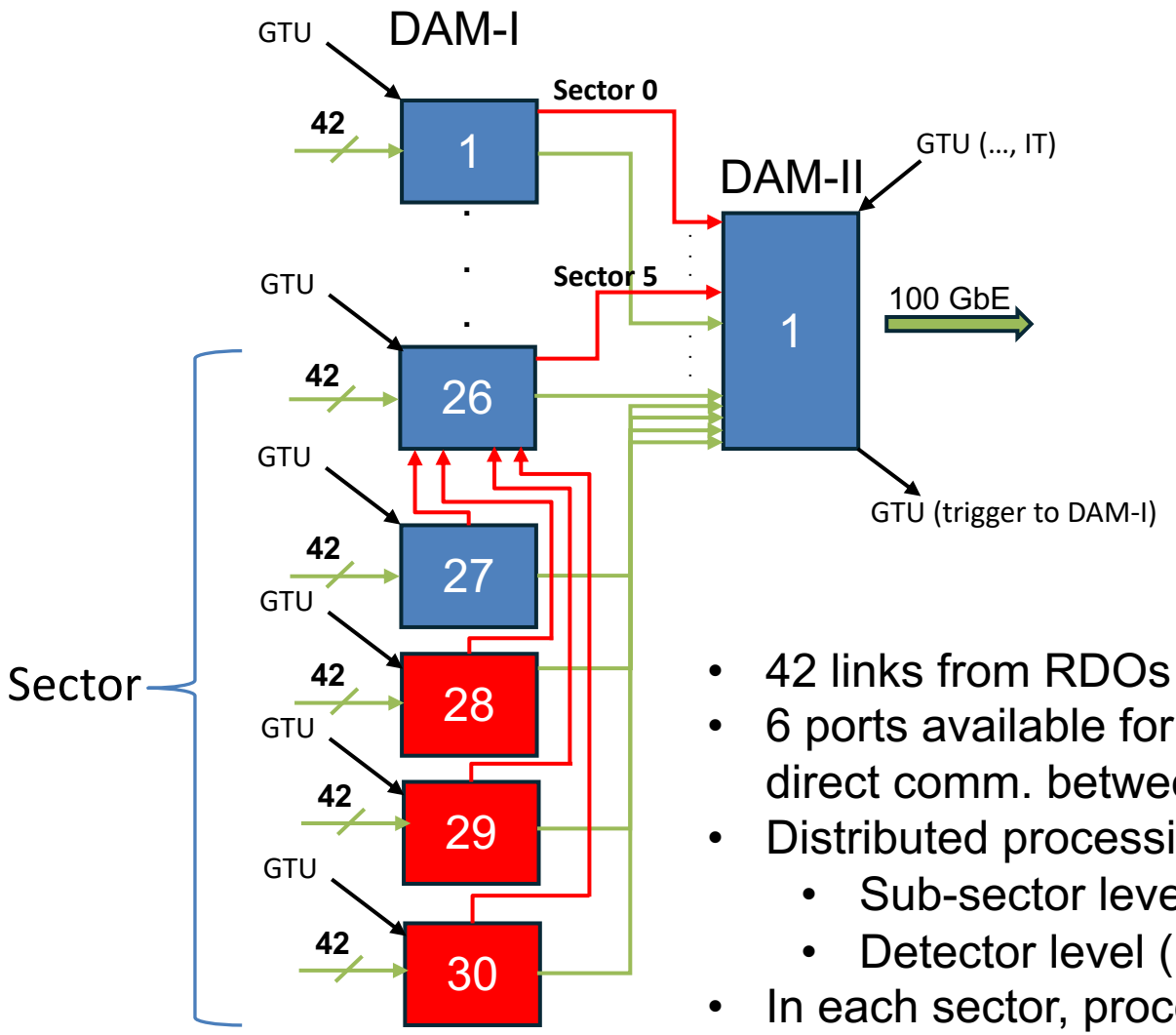




Communication latency < 1 us up to 1kB message size

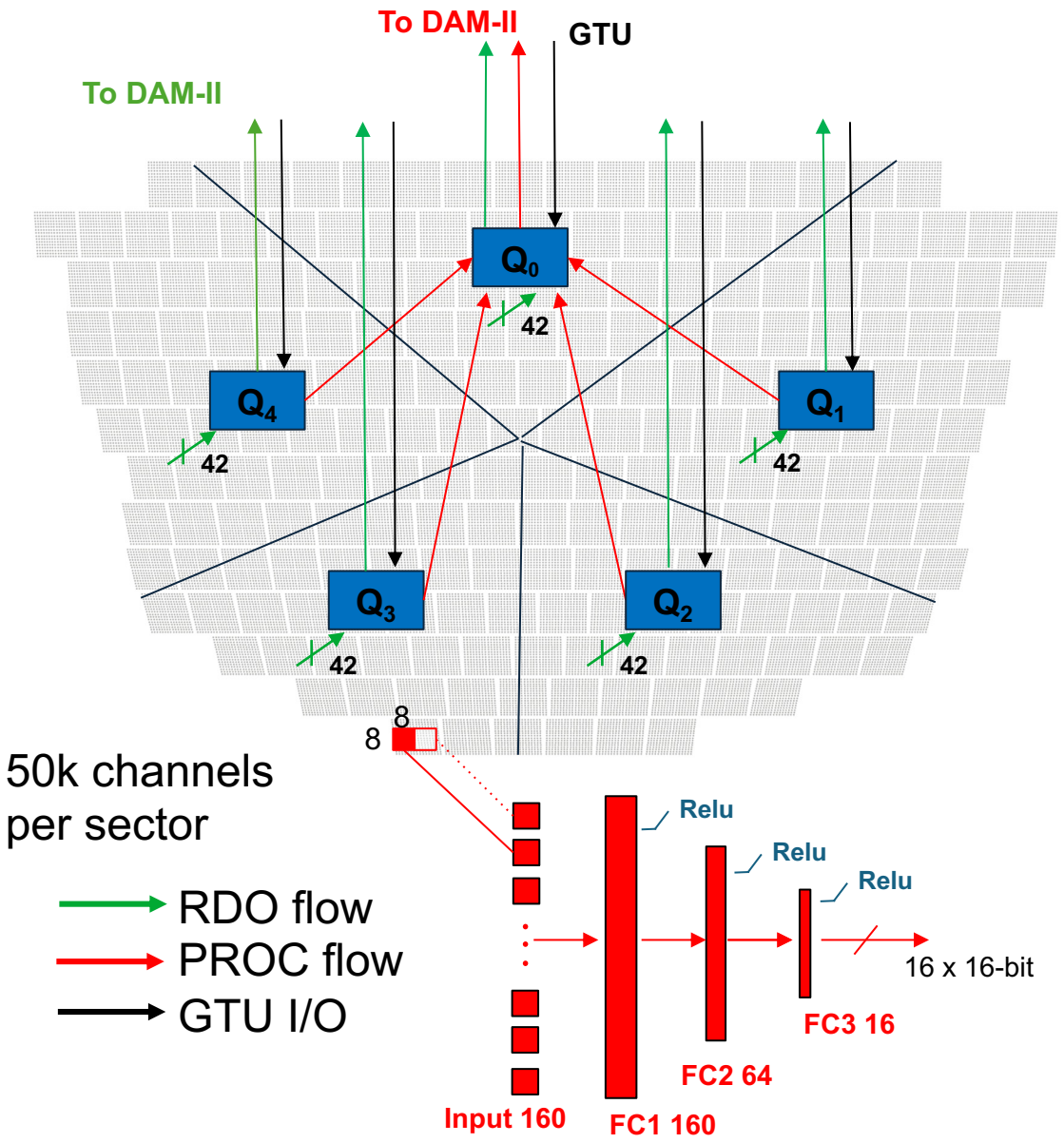
dRICH Data Reduction Stage on FPGA: example deployment

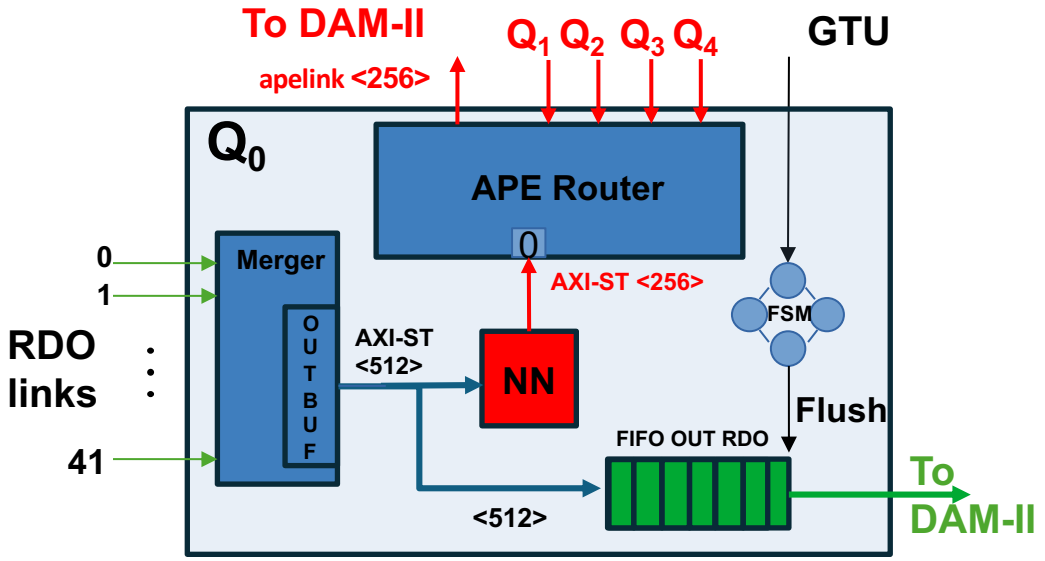


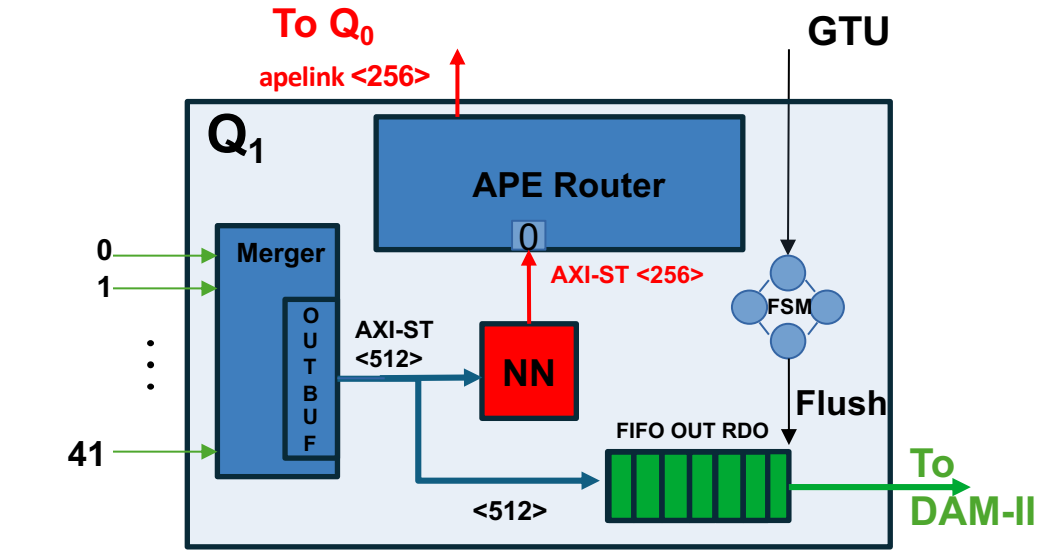


- 42 links from RDOs
- 6 ports available for direct comm. between DAMs
- Distributed processing
  - Sub-sector level (DAM-I)
  - Detector level (DAM-II)
- In each sector, processed data routed by one DAM-I to DAM-II

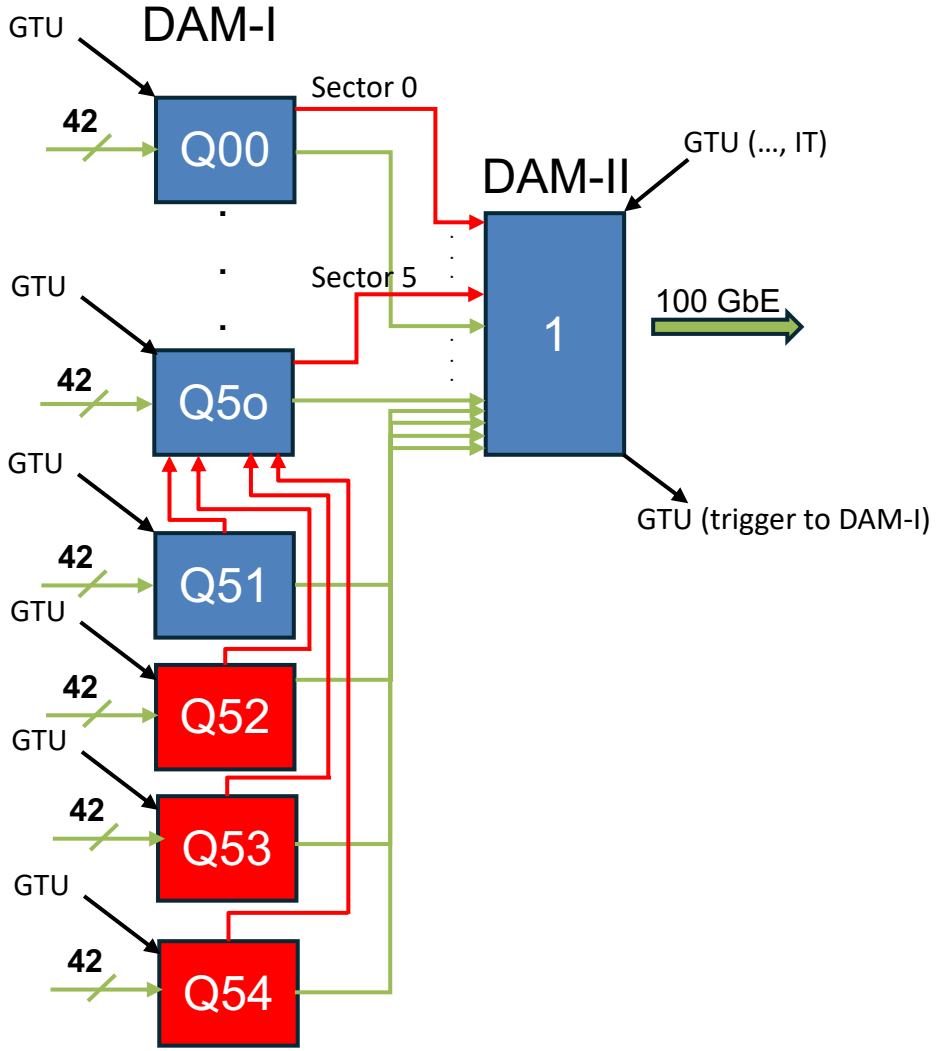
dRICH Data Reduction Stage on FPGA: example deployment

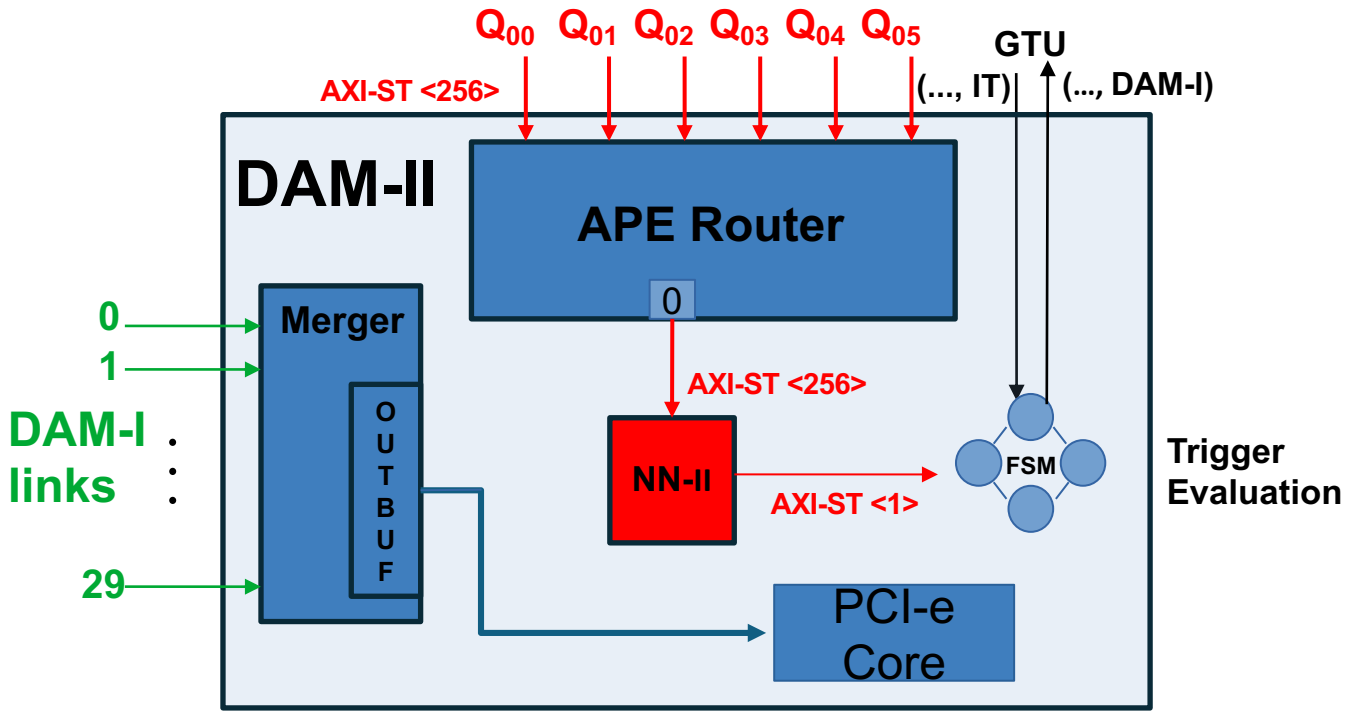


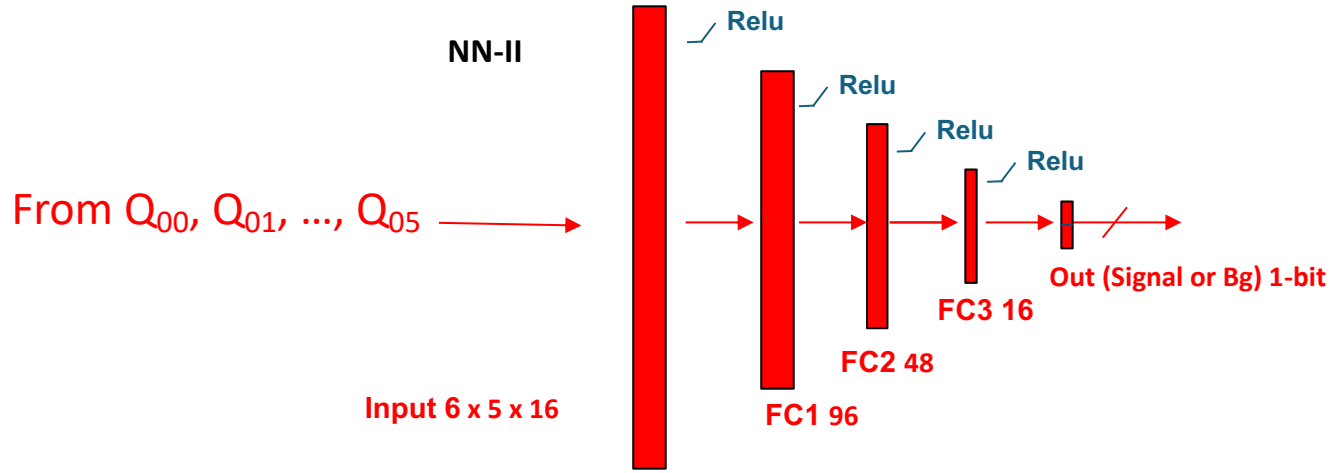




dRICH Data Reduction Stage on FPGA: example deployment







Current status and outlook

- We have started collecting datasets and experimenting with inference models.
- Details of the final deployment will be affected by several factors
    - Final selection on the inference model(s): BDT, MLP, CNN, GNN, …
    - Actual additional DAQ resources (DAMs, …) dedicated to the data reduction system.
    - Net amount of FPGA resources available (discounting the “standard” DAQ firmware) in DAMs to implement processing and communication.
- Having two Felix-155 boards available in our labs (BO, RM1/2) is crucial for the smooth continuation of the activities
    - Design and development of the DAQ firmware
    - Integration in the DAQ FW design of processing and communication features
    - Deployment of processing pipelines
    - Test of inter-dam communication for the data reduction distributed processing

ePIC RM1 - Anagrafica 2025

	FTE %	Posizione	Attività/Responsabilità
A. Biagioni	0.1→0.2	Tecn. III Livello	APE group, NN FPGA PID development, integration in the DAQ . Exploit the APEIRON framework and the NA62 RICH experience
F. Capuani	0.2	Ric. III Livello	
C. Chiarini	0.2	Dottoranda Sapienza	
O. Frezza	0.1	Tecn. III Livello	
F. Lo Cicero	0.2	Tecn. III Livello	
A. Lonardo	0.2	Tecn. II Livello	
M. Martinelli	0.2	Tecn. III Livello	
P. Perticaroli	0.2	Dottorando INFN	
F. Simula	0.1 → 0.2	Ric. III Livello	
P. Vicini	0.1 → 0.2	Tecn. II Livello	
L. Pontisso	*0.2*	Tecn. III Liv. TD	sinergia con PNRR/*, NN FPGA PID developers
C. Rossi	*0.4*	Ass. Ric. INFN	
A. Ciardiello	0.1	RTDA Sapienza	MC analysis, test, support APE group developments (E.C. resp. locale)
E. Cisbani	0.1	Dirigente ISS	
G. M. Urciuoli	0.1	Associazione Senior INFN	
Totale	2.2		non include sinergie

Incremento FTE di 0.5 rispetto a 2024

ePIC RM1 – Richieste per il 2025

Capitolo	kEuro	Voce
Missioni	2	Riunioni di collaborazione nazionale (4 persone x 3 giorni ~ 2 keuro)
	6	Incontri tecnici Furlev/JLab group and Felix FPGA developers: 2 persone x 10 giorni ~ 6 keuro
	4	Incontri tecnici gruppo Genova (Tagger dRICH), Bologna (Readout) e Trieste (analisi dati): 3x2 persone x 5 giorni ~ 4 keuro
	2	Partecipazione international collaboration meeting EIC-EPIC (TorVergata), sola iscrizione: 6 persone x 0.3 keuro ~ 2 keuro
Consumo	2	Consumabile per interfaccia con dRICH readout
Attrezzature	24	1 Felix FPGA 155

Le FPGA Felix saranno condivise con il gruppo di Bologna che si occupa del readout