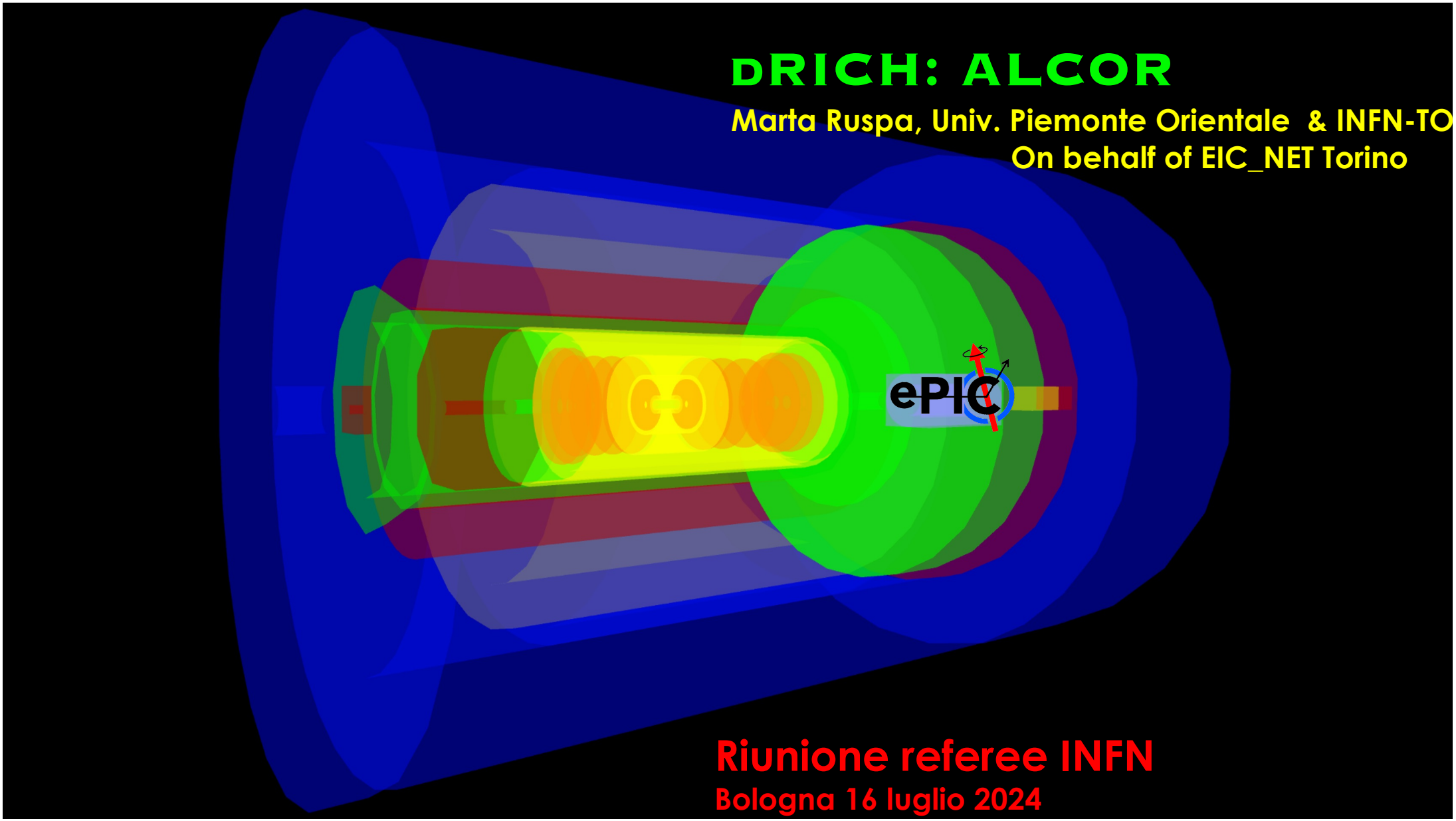


dRICH: ALCOR

Marta Ruspa, Univ. Piemonte Orientale & INFN-TO
On behalf of EIC_NET Torino

Riunione referee INFN

Bologna 16 luglio 2024

dRICH @Torino: ALCOR ASIC!

Sviluppato da INFN-TO per lettura SiPM a **DARKSIDE** a 77K

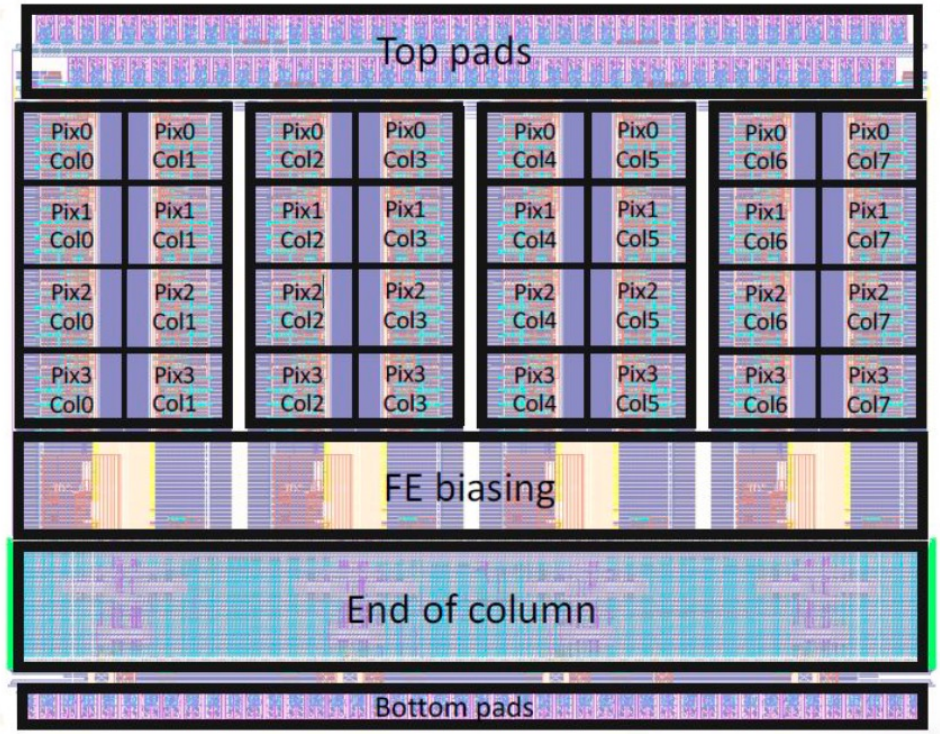
Scelto per lettura SiPM del dRICH di EPIC-EIC

INTRODUZIONE

ALCOR (A Low Power Chip for Optical Sensor Readout)

http://personalpages.to.infn.it/~fcossio/projects/ALCOR/ALCOR_user_guide.pdf

- **32-pixel** matrix (8x4) mixed-signal ASIC (4.95 mm × 3.78 mm), new version will be **64-pixel** matrix (8x8)
- Single-photon time tagging + **Time-over-Threshold** or **Slew-Rate** measurements for time walk correction
- On-chip **signal amplification**, **conditioning** and **digitization**, 32-bit event word
- Fully digital output: 4 LVDS 320 MHz DDR Tx links
- Power consumption **~10-12 mW/channel**
- 0.11 µm CMOS technology



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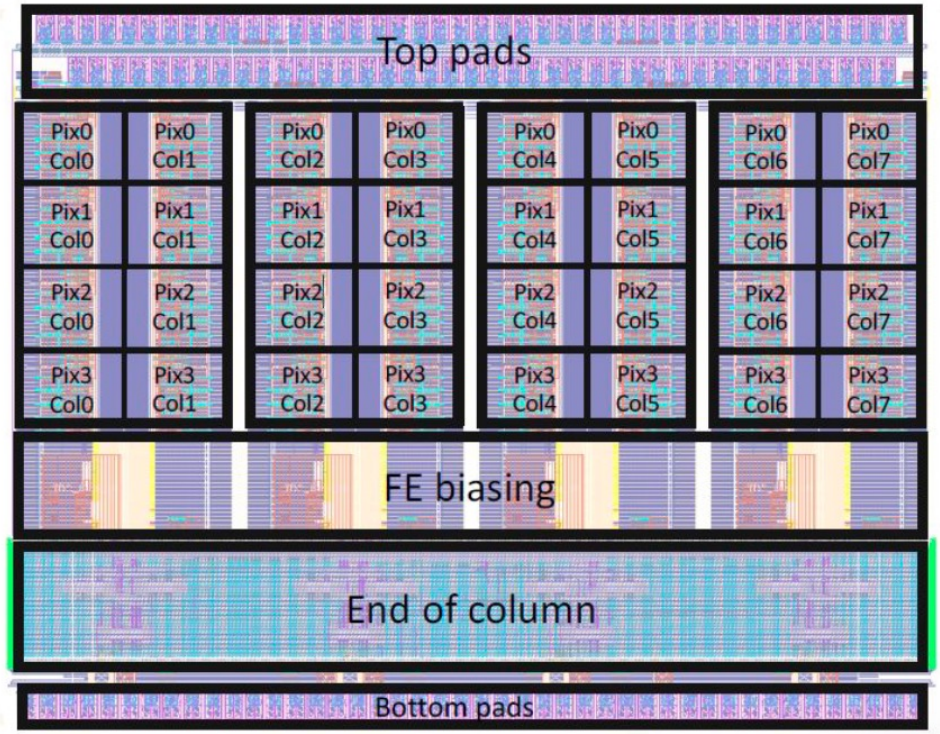


- ALCOR must provide **single-photon time tagging** of signals coming from SiPM sensors
- ALCOR must cope with **SiPM DCR: 300 kHz/channel** (at max SiPM radiation damage)

La storia di ALCOR

Sviluppato da INFN-Torino per lettura SiPM a **DARKSIDE** a 77K

Scelto per lettura SiPM del dRICH

- **v1** disponibile a **inizio '21**
- Successivo sviluppo di una **nuova versione ottimizzata per EIC-dRICH**

  → **v2** disponibile a **giugno '23**
- Attualmente **in disegno** la versione **v3** (64 canali, flip-chip BGA package)
- v1 e v2 utilizzate per **test irradiazione e test su fascio** (ultimo beam test **maggio '24**)

Reminder: ALCOR v2

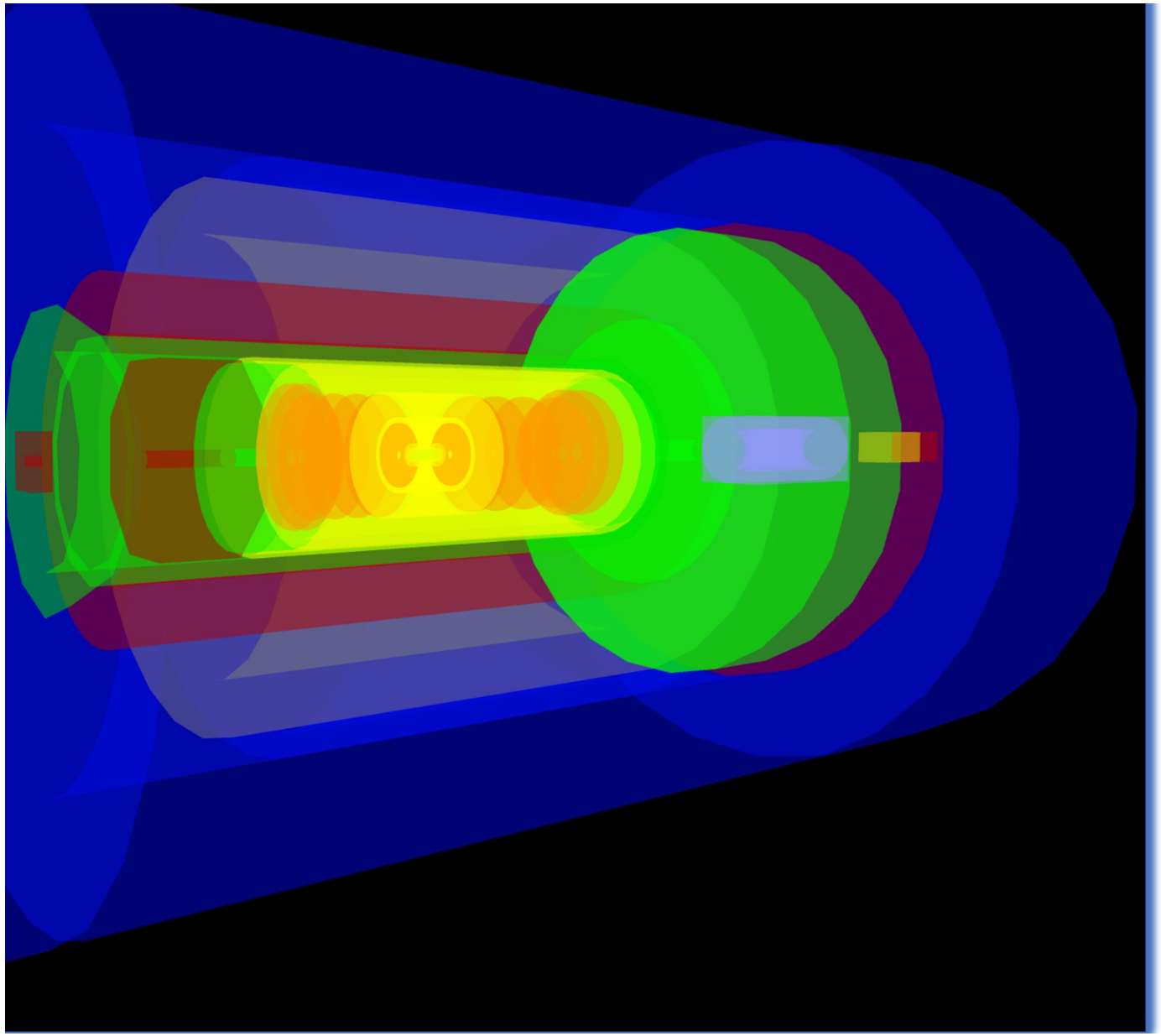
v2 marks the start of a specific branch of the ASIC devoted to EIC application

ALCOR v2

- MPW, submitted in Dec 2022
- 60 chips, received in June 2023
- Includes new features targeted for EIC dRICH and bug fixes:
  - ✓ TDC logic critical error at high rates solved also for DCR rate at room temperature
  - ✓ New FE gain settings more suited for singl photon applications
  - ✓ On-chip test-pulse also for EIC SiPM polar
- Successfully validated in 2023 beam test

ALCOR v2.1

- INFN internal engineering run, chips received in Jan 2024
- Includes small bug fixes w.r.t. ALCOR v2
- Very high number of chips available to increase instrumented area for dRICH prototype and assemble other test setups
- Version currently used: beam test (May-June 2024) to validate ALCOR-based dRICH readout and evaluate its performance



Attività nel 2024

- Disegno di ALCOR v3
- Disegno dell’interposer per BGA packaging
- Preparazione e presa dati test beam fine maggio

Disegno di ALCOR v3

- **64 channel version** inside a **BGA package** (256 IO pins)
- Small revisions of FE design to **improve time resolution** and rate capability of the SIPM+ALCOR system
- **Digital shutter:** inhibit pixel digital logic for data reduction (EIC bunch crossing 10 ns, about 300 ps bunch lenght → 2-3 ns time window provides factor 3-5 data reduction before digitization)
- Operation with multiple of EIC clock frequency (98.52 MHz): digital logic, TDCs and serializers re-implemented and verified at 394.08 MHz
- Protection for Single Event Upset (SEU) extended to periphery configuration registers

Ready for submission to Multi-Project Wafer (MPW) at the end of 2024

ATTIVITÀ NEL 2024

ALCOR v3, MPW

Coperto da fondi 2024

Run del 25 novembre cancellato da UMC

Ordine verrà comunque fatto nel 2024

- Ordine verrà comunque fatto quest'anno

From Svetlana Kazachenko (imec) <Svetlana.Kazachenko@imec.be>
To Cossio Fabio <fabio.cossio@to.infn.it> 10/07/2024, 16:46
Cc salesops <imeclink.salesoperations@imec.be>,
Paul Malisse (imec) <Paul.Malisse@imec.be>
Subject **Re: RFQ MPW and NTO eng run ALCOR64 project UMC L110AE**

Dear Fabio,

I will create quotes for you end of next week.

Our finance team can make down payment invoices for you to pay already in advance, for that you need to place POs for MPW and for NTO accordingly after receiving quotations from us.

Is that okay for you?

FYI I will be OOO from tomorrow till 18th July.

Thank you.

Best regards,
SVETLANA KAZACHENKO
Business Development Manager
M +32 475 39 22 19 I T +32 16 281154
svetlana.kazachenko@imec.be I http://www.imec-int.com/ I LinkedIn imec
Kapeldreef I 3001 Leuven I Belgium
imec e-mail disclaimer

Old schedule

UMC

MPW | € MPW | mini@sic | € mini@sic

UMC MPW	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
UMC 28N Logic/Mixed-Mode – HPC		19		22			22	26	30	28		
UMC 40N Logic/Mixed-Mode – LP			11			24	29	26			18	
UMC 65N Logic/Mixed-Mode/RF – LL	2	26							2	21		
UMC L110AE Logic/Mixed-Mode/RF		26				3			2		25	
UMC L180 Logic GII, Mixed-Mode/RF			4					26				

New schedule

UMC

MPW | € MPW | mini@sic | € mini@sic

UMC MPW	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
UMC 28N Logic/Mixed-Mode – HPC		19		22			22					
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UMC 65N Logic/Mixed-Mode/RF – LL	2	26							2			
UMC L110AE Logic/Mixed-Mode/RF		26				3			2			
UMC L180 Logic GII, Mixed-Mode/RF			4					26				

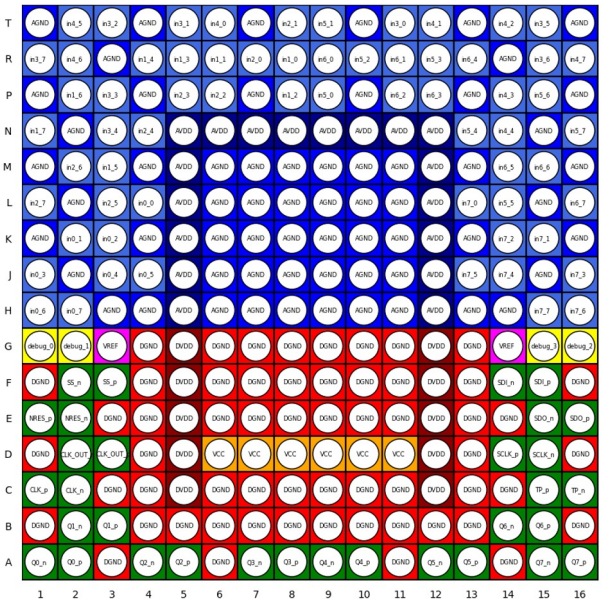
ATTIVITÀ NEL 2024

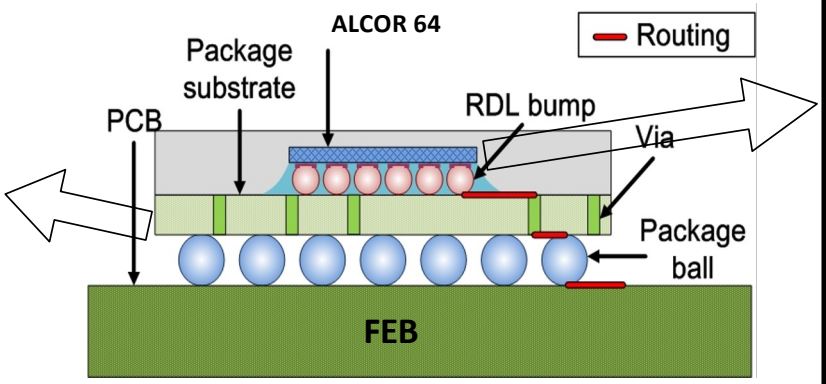
ALCOR v3, BGA package

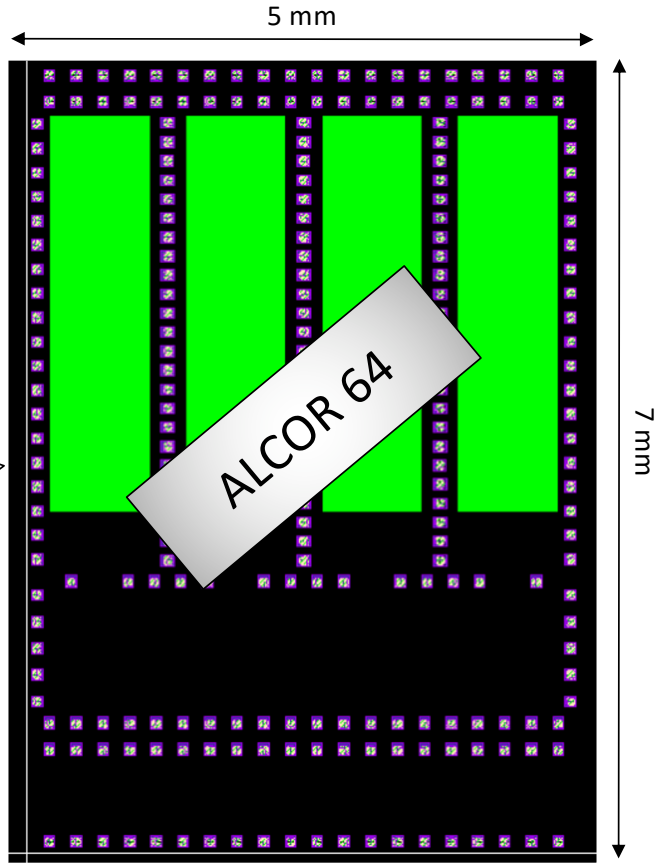
Fondi 24, SJ (50keuro)

BGA: ball grid array

- Substrato disegnato da INFN Torino
- Flip-chip assembly e packaging finale eseguito da ALTER TECHNOLOGY (https://wpo-altertechnology.com/flip-chip-assembly/)







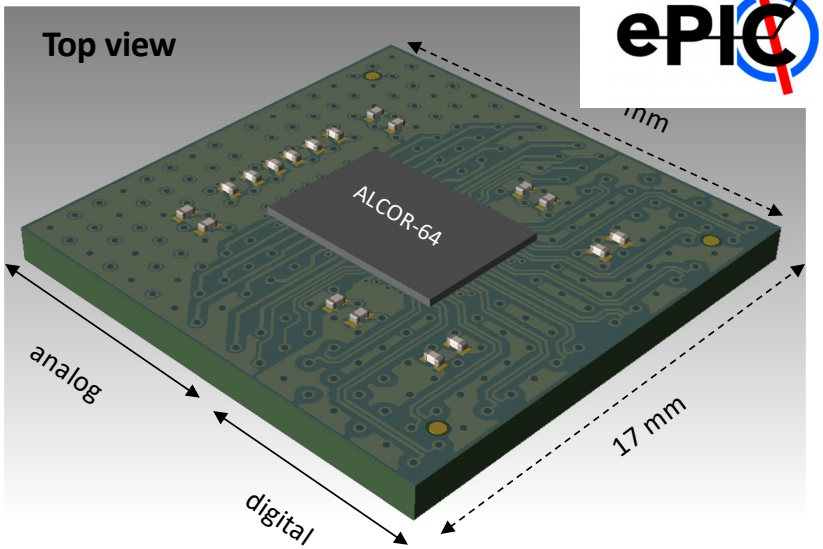
ATTIVITÀ NEL 2024

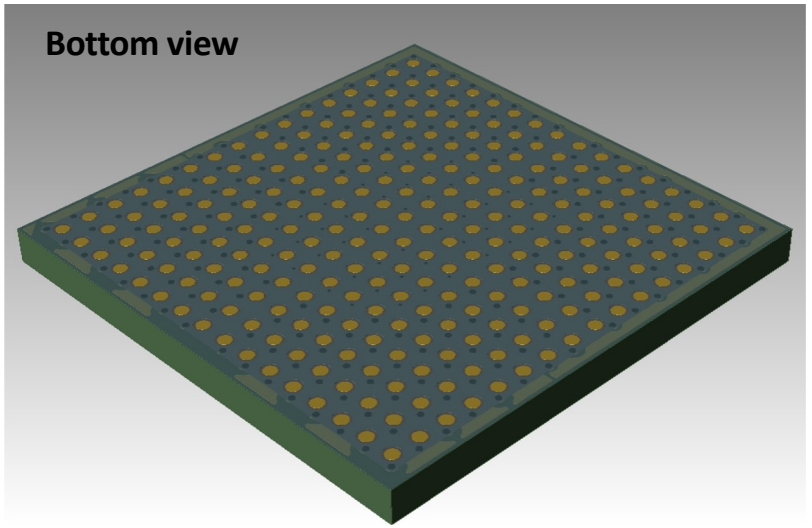
ALCOR v3, BGA package

Fondi 24, SJ (50keuro)

BGA: ball grid array

- Dimensioni package: 17 x 17 mm^2
- Numero di connessioni: 256 balls (16x16)
- Passo: 1 mm
- Materiale substrato: BT Epoxy (Isola G200)
- Numero di layer = 10
- Spessore totale = 1.27 mm

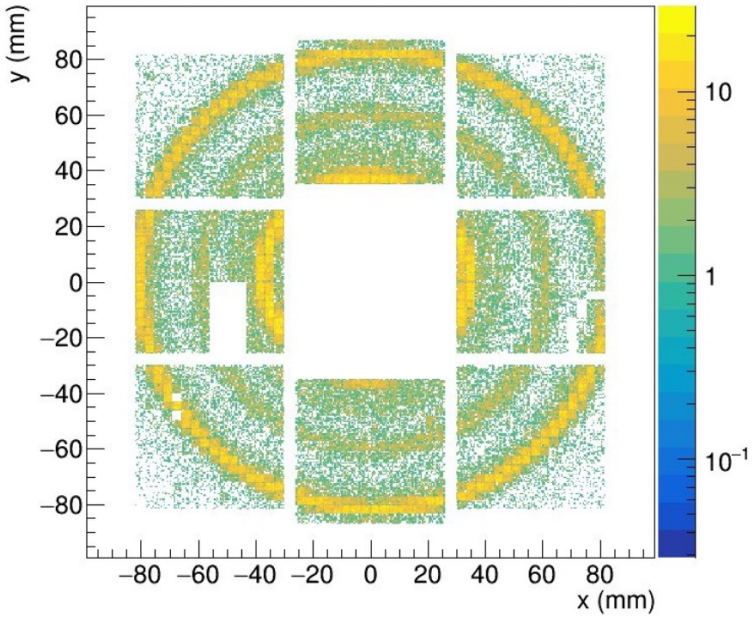




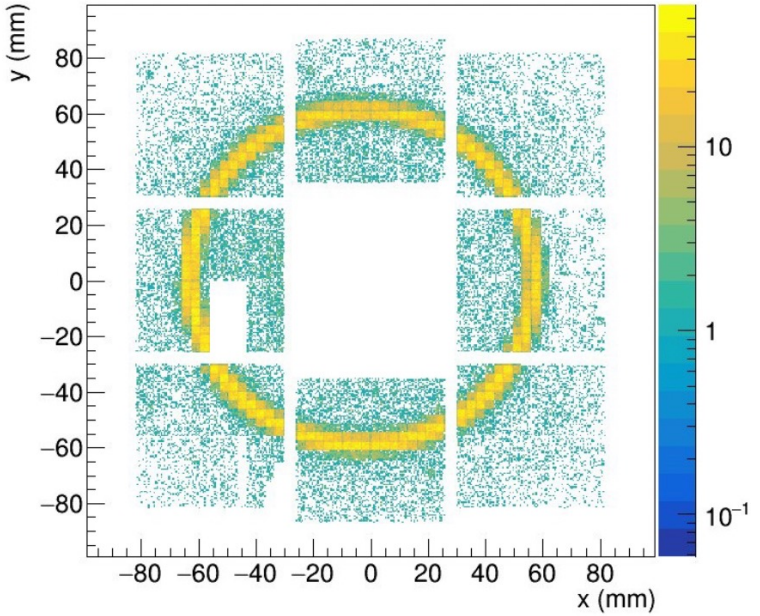
Layout quasi completo, pronto per richiesta offerta nelle prossime settimane e sblocco SJ a settembre

Test beam di fine maggio

Aerogel + C_2F_6 radiators, positve beam, 8 GeV/c

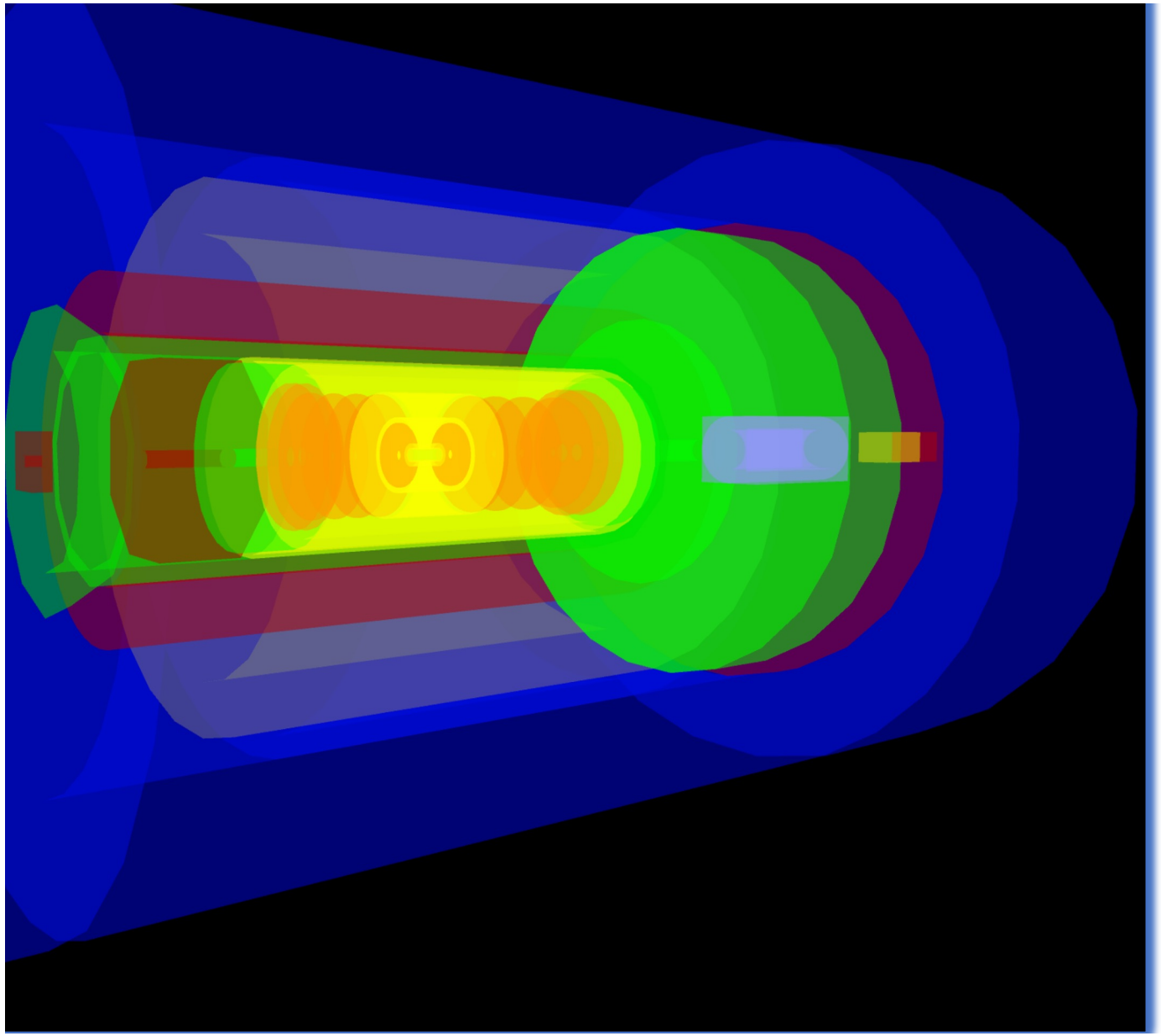


C_4F_{10} radiator, negative beam, 11 GeV/c



64 ALCOR v2.1,
2048 canali

→ talk di R. Preghenella



Attività nel 2025

- Validazione di ALCOR v3
- **Produzione di ALCOR v3!**
- Sviluppo schede di front-end (FEB)

Engineering Run (ER)

- First complete electrical characterization and validation of ALCOR v3 on several samples

→ v3 ready for **ER** at the end of 2025

Richiesta 270 keuro

ALCOR production, engineering run (ER)

Richiesta 270 keuro

Quotation for masks, engineering lot

[redacted]

To: INFN - SEZ. DI TORINO
Via Pietro Giuria 1
10125 Torino, Italy

Attn.: Manuel Dionisio Da Rocha Rolo

Dear Mr. Manuel Dionisio Da Rocha Rolo,

IMEC is pleased to provide the following offer (hereinafter "Quotation") to INFN - SEZ. DI TORINO (hereinafter "Client") to support the project [redacted] with tape-out and prototype wafers in UMC's L110AE technology (hereinafter "Project").

1 Deliverables and price

UMC L110AE 1P8M 1.2V/2.5V Mixed Signal process, 8 Inch Triple Well - MiM Cap - HR - HS, SP, LL devices 39L 40kA top metal[redacted]		
NRE: Mask Set	174,820 USD	set
NRE: Pilot / Engineering Wafer lot - 8 inch Lot based charge	33,370 USD	12 wfrs/lot

Notes

- *(*) Upon receipt of this quotation customers should inform imec on the usage of Faraday IP inside the tapeout.*
- *Customer should inform the imec team at least on a monthly basis about the tapeout plan to ensure a smooth tapeout preparation.*
- *An engineering lot of 12 8 Inch wafers (the pilot lot) is started with the new maskset. 6 wafers are guaranteed to pass all quality and WAT tests. All good wafers are delivered.*
- *The engineering lot charge is lot based and will be invoiced in full - and needs to be paid - before wafer start.*
- *All pilot wafers that are fabricated till the end of process, run in a HOT lot processing scheme*

Vecchia offerta del 22, siamo in attesa di una offerta aggiornata

ATTIVITÀ NEL 2025

Non solo ER

- First complete electrical characterization and validation of ALCOR v3 on several samples. To be designed and produced an «ad hoc» **socket test board**

Richiesta 5 keuro

→ v3 ready for **ER** at the end of 2025

Richiesta 270 keuro

- Start development of automated test system in view of the ASIC mass production – will use **socket test board**

- Design of the **final Front End Board (FEB)** in parallel with the RDO and SiPM carrier board design. Production of about **20** such boards.

Richiesta 10 keuro

- **Production of Fake FEB (around 40)** to be used in test of RDO-ALCOR v2

Richiesta 5 keuro

INFN TORINO

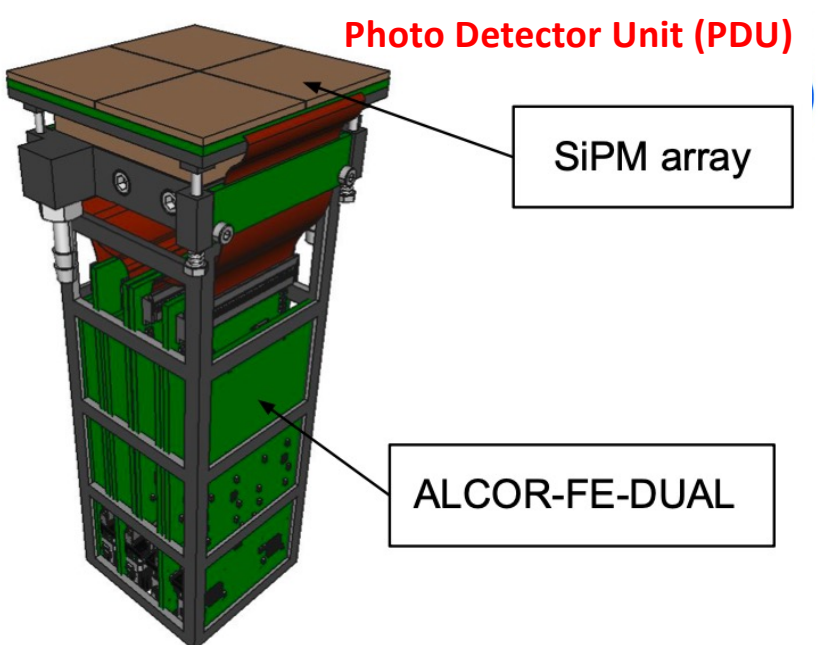
Current RO system

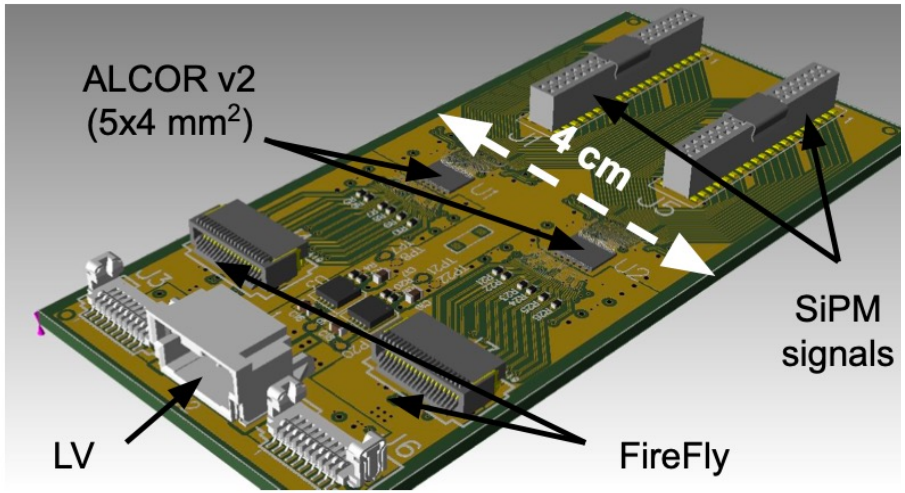
ALCOR FE-DUAL

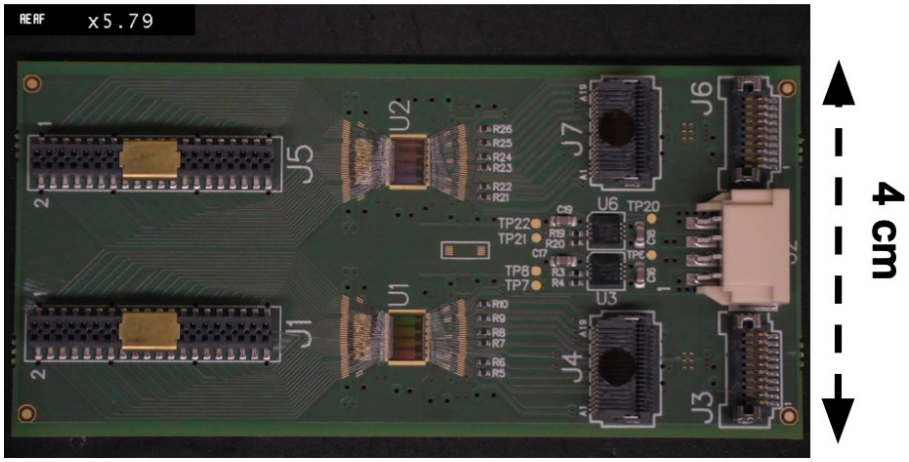
- Two 32-channel ALCOR v2 wire-bonded on the PCB

- 4 ALCOR FE-dual boards for each PDU

Used in 2023 and 2024 beam tests



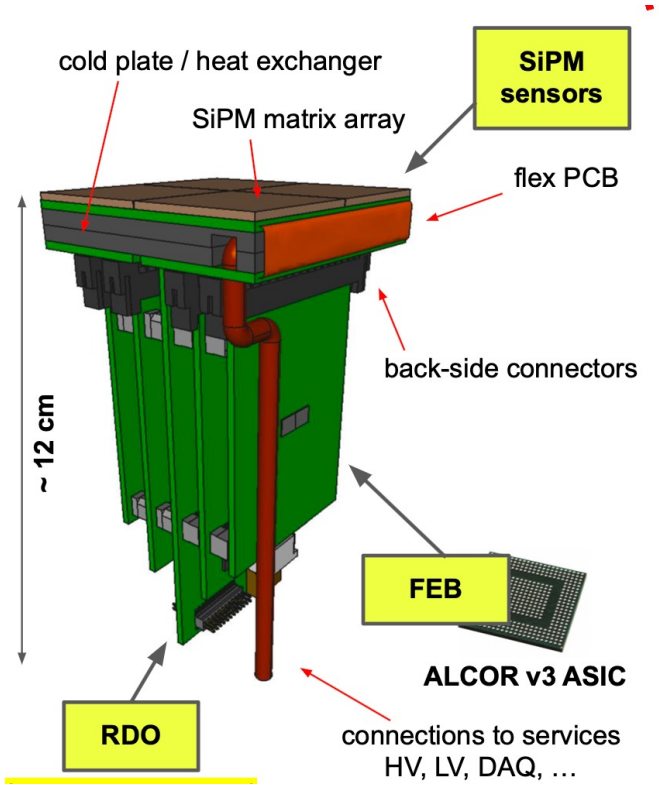


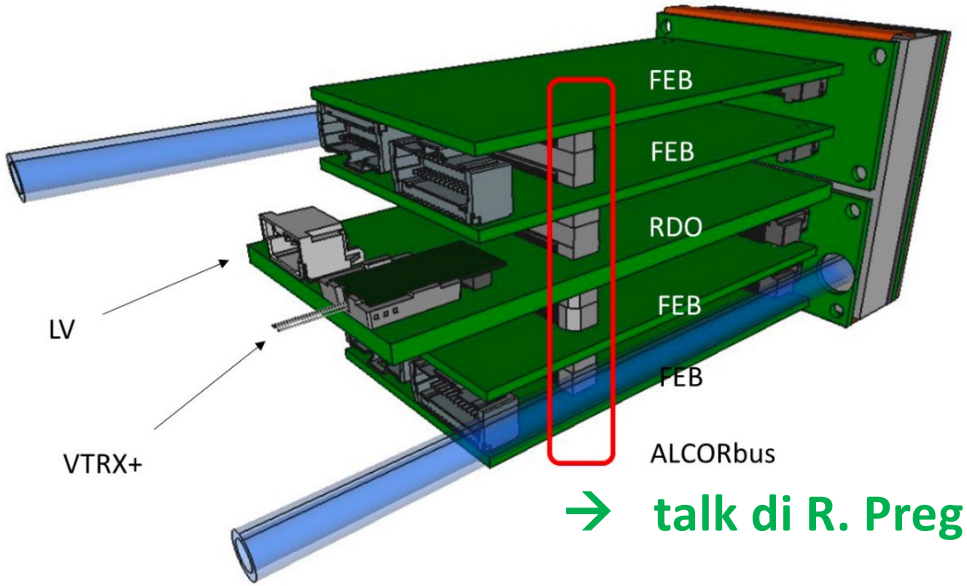


designed by INFN Torino (Marco Mignone)

Future RO system: final FEB

Photo Detector Unit (PDU)





→ talk di R. Preghenella

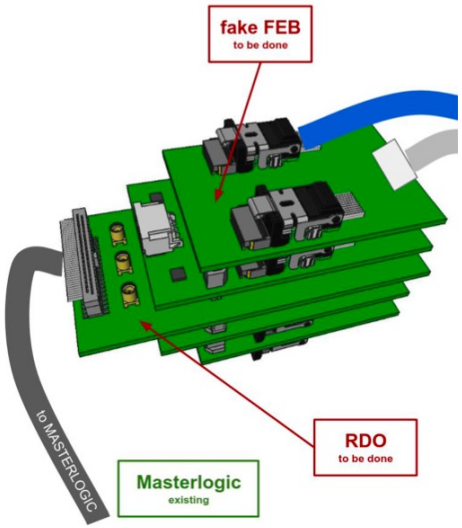
- **Produzione schede Front–End Board (FEB) dove montare gli ALCOR v3 in package BGA** Richiesta 10 keuro
- I due ALCOR a 32 canali wire-bonded sulla scheda ALCOR FE dual sostituiti da 1 ALCOR a 64 canali BGA
- Connettori FireFly sostituiti da interfaccia verso RDO
- 8 x 4 cm2 maximum area

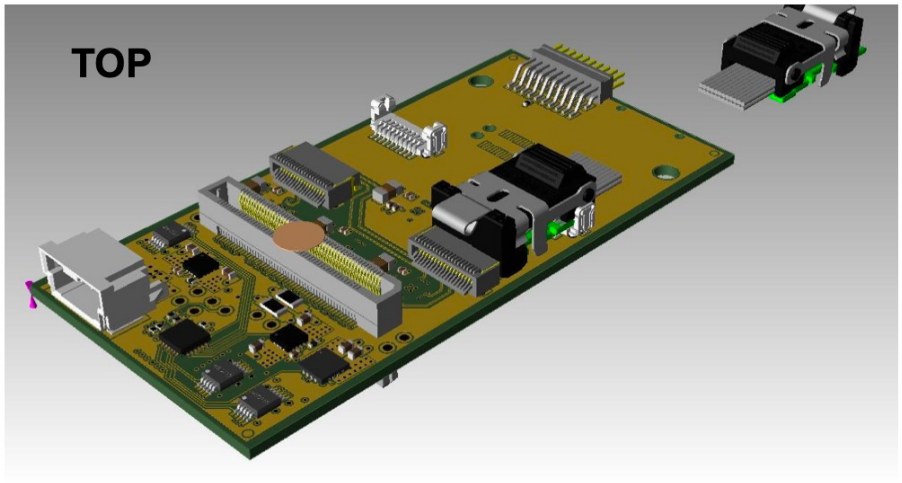
Fake FEB

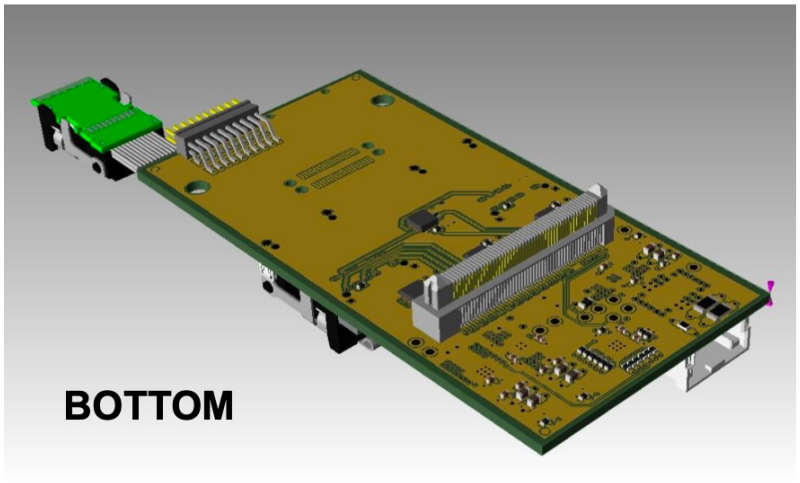
Richiesta 5 keuro

Support 2024-2025 dRICH activities when final FEB and ALCOR v3 are not available yet

- allows integration tests of RDO with current ALCOR-FE-DUAL boards (already available and validated)
- 4 fake-FEBs + 1 RDO (still off-detector)



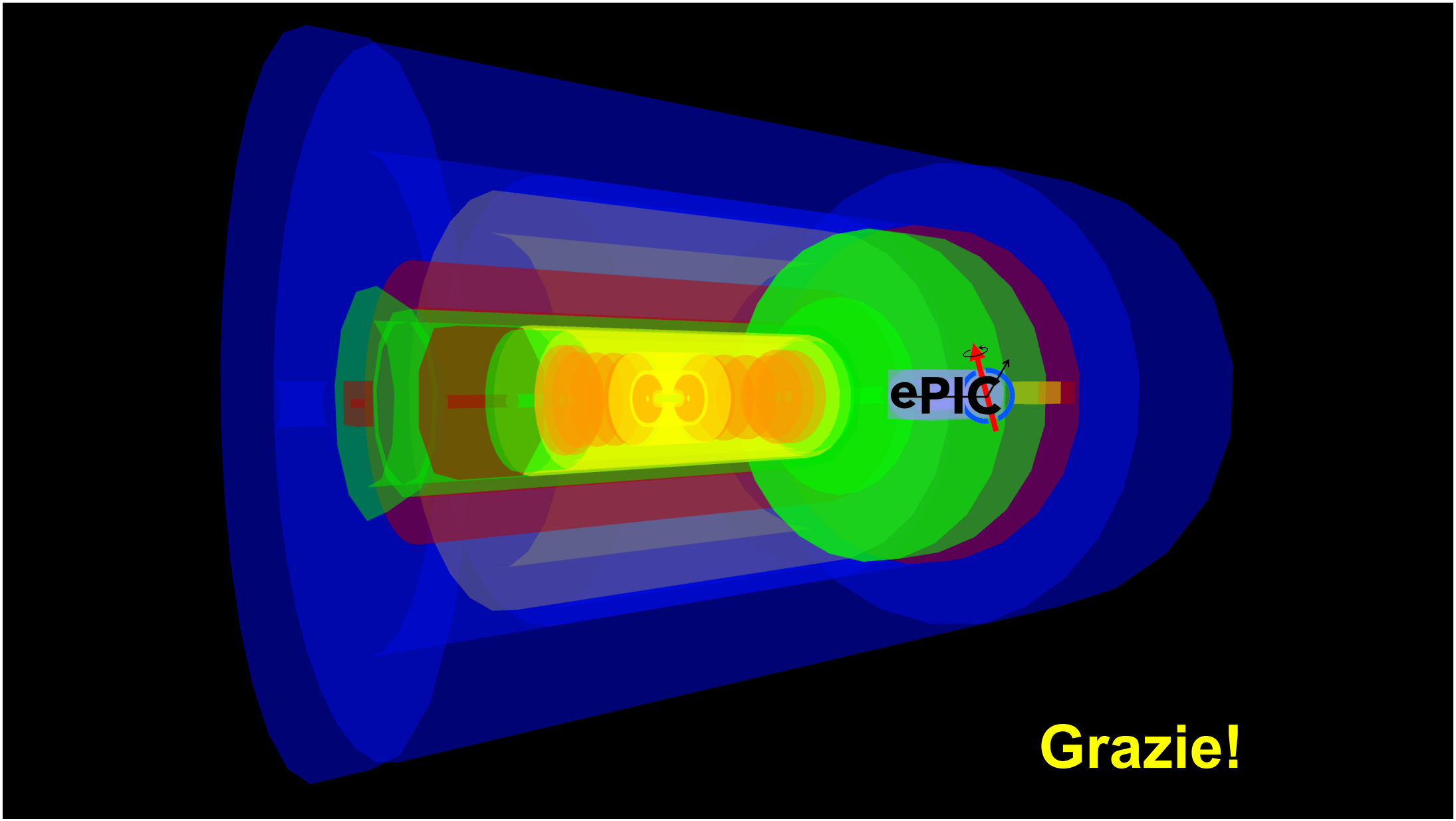




ATTIVITÀ NEL 2025

Sintesi delle richieste di Torino per 2025

Descrizione	RIchieste	SJ
Sottomissione Engineering Run (ER)		270
ALCOR fake FEB	5	
ALCOR final FEB	10	
Test board con zoccolo per BGA	5	



Grazie!