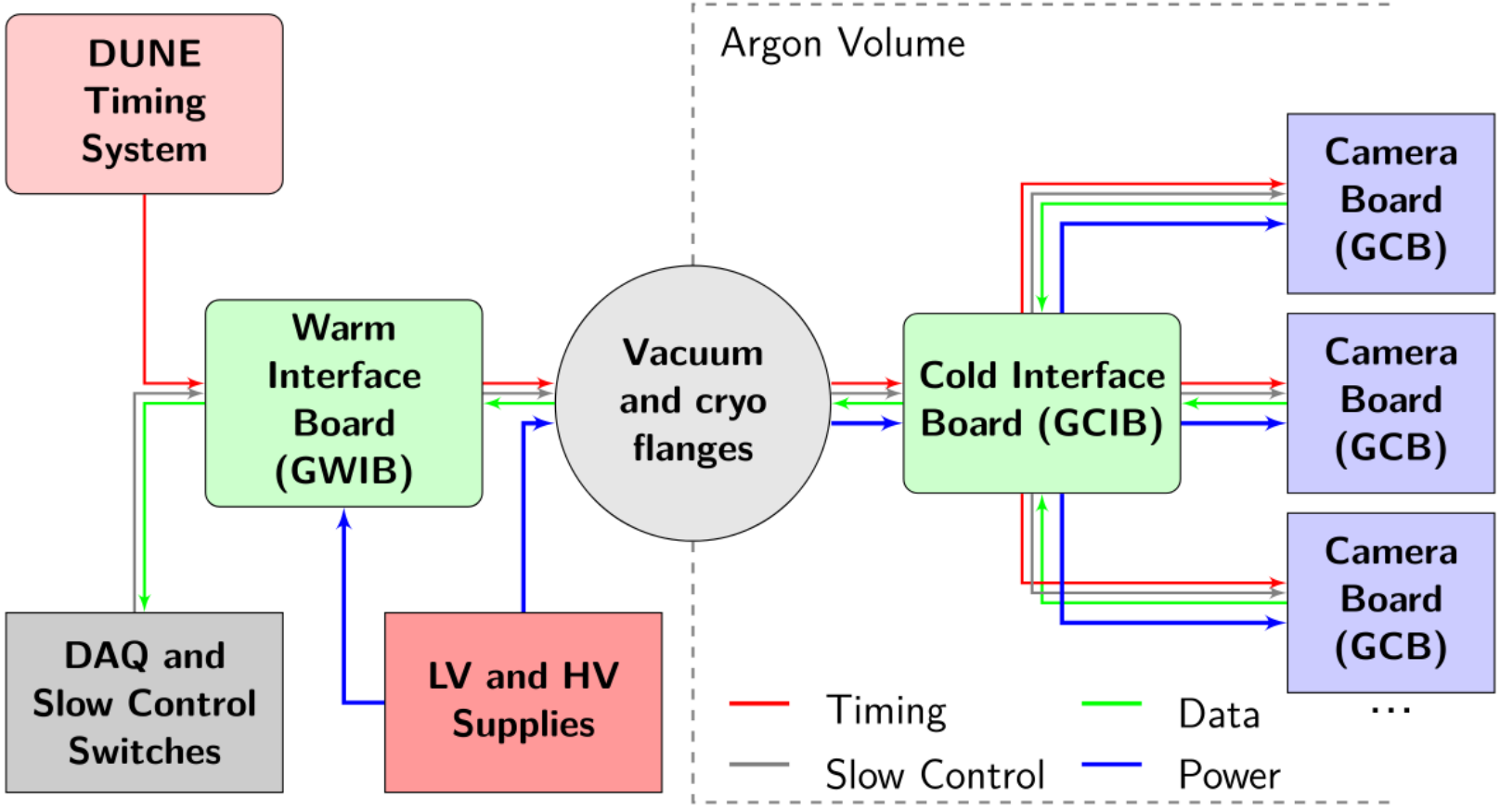
GRAIN readout overview and integration

Nicolò Tosi – INFN Bologna

GRAIN Readout Scheme



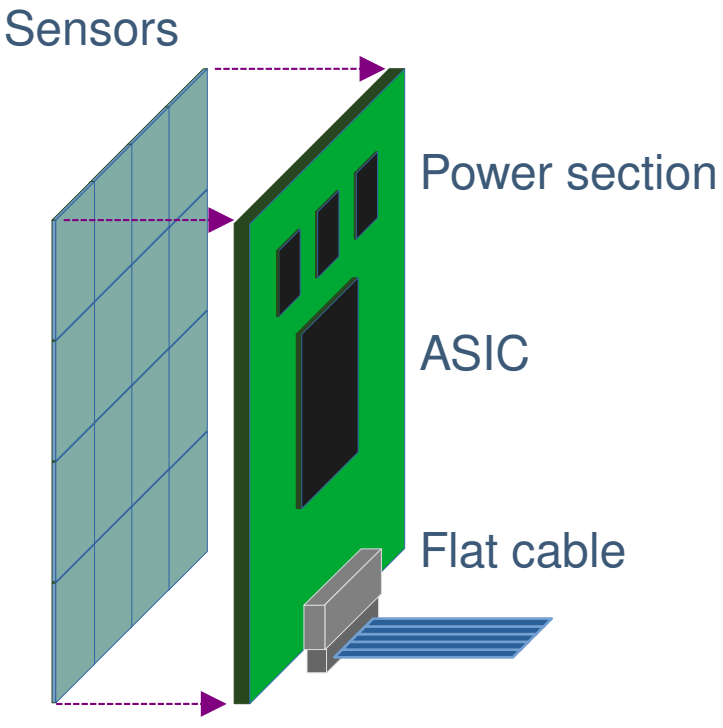
GRAIN Camera Board

GRAIN will be equipped with O(50-60) *cameras*:

- Regardless of optics choice, 1024 channel SiPM matrix
  - SiPM size may differ, lens 2x2 mm^2 vs mask 3x3 mm^2
- One cryogenic 1024 ch mixed signal ASIC
  - Dual TDC + charge integrator per channel
  - Low power
  - Optimized LVDS I/O

GRAIN Camera Board

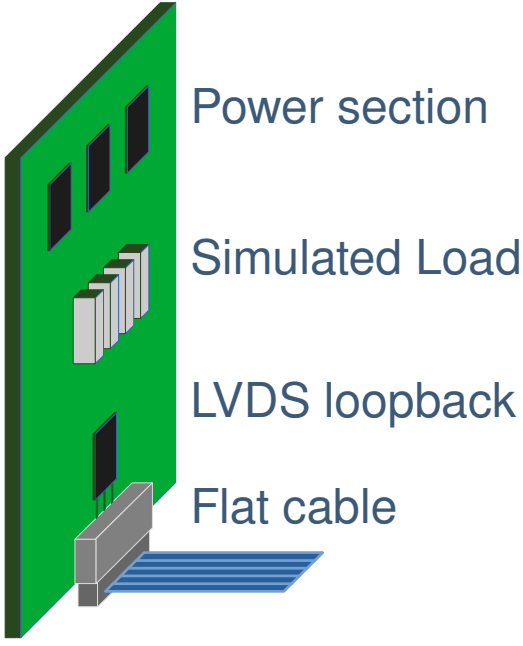
- On the front side:
  - VUV or WLS coated SiPM Matrices
- On the rear side:
  - One ASIC
  - A few LDO regulators
  - Connection



GRAIN Mock Up Camera Board

A test board for thermal and electrical tests

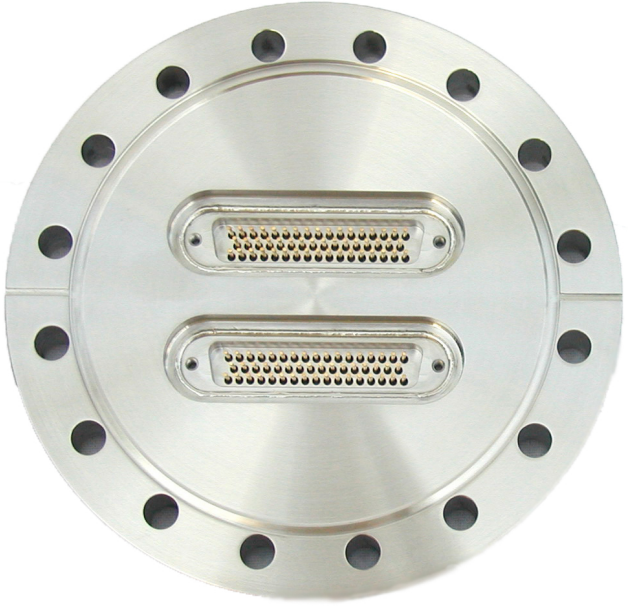
- Validate commercial LDOs
- Validate full I/O solution
- Study bubble formation and mitigation
  - ASIC simulated with equivalent power Resistors



Cold Interface Board and Flanges

A study is now in progress on the optimization of I/O considering:

- Availability of commercial feedthrough flanges with high density connectors (Sub-D or similar) vs custom flanges

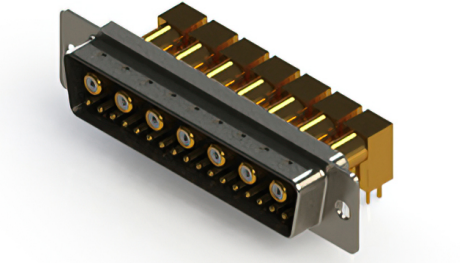


Example CF with 2x Sub-D 50 pin (Allectra GmbH)

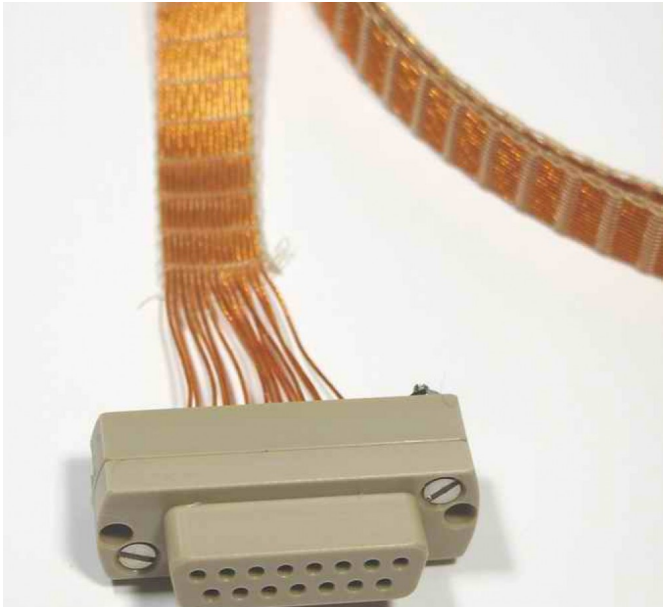
Cold Interface Board and Flanges

A study is now in progress on the optimization of I/O considering:

- Choice of cables and connectors as a compromise of signal integrity (for at least clk and data lines at 300+ MHz) vs cost



Example Sub-D with combined coax & pins

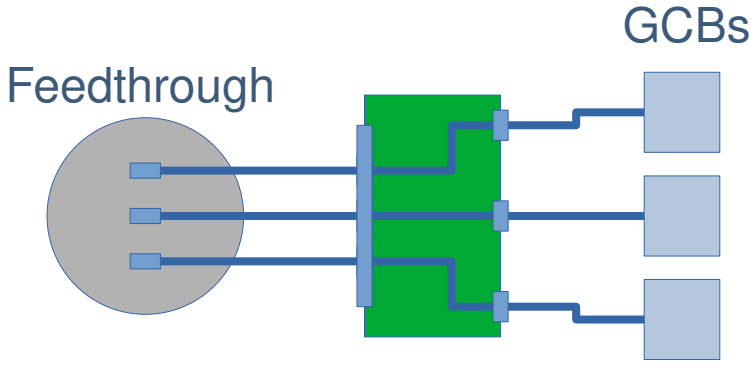


Example Sub-D with standard pins, Peek connector and polyimide cable

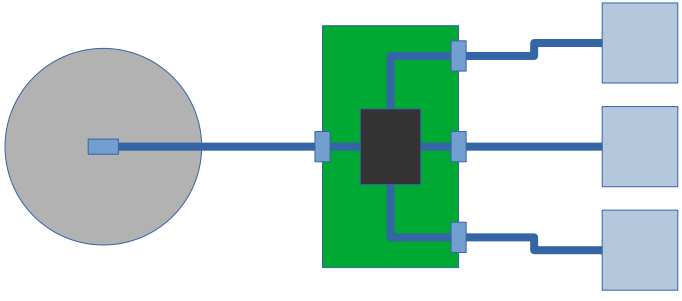
Cold Interface Board and Flanges

A study is now in progress on the optimization of I/O considering:

- Buffering signals inside the cryostat on the cold interface board to minimize I/O vs risk of losing multiple cameras to a single component failure



GCIB as passive adapter

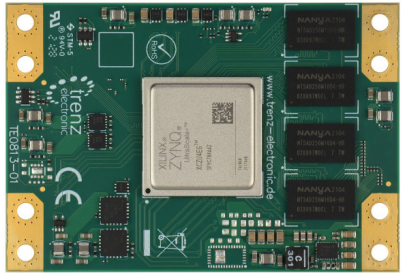


GCIB as active buffer

GRAIN Warm Interface Board

This board hosts an FPGA (and a CPU) to interface the ASIC with:

- The DUNE Timing System (dedicated fiber)
- DUNE-DAQ (10 GbE)
- DCS (1 GbE)

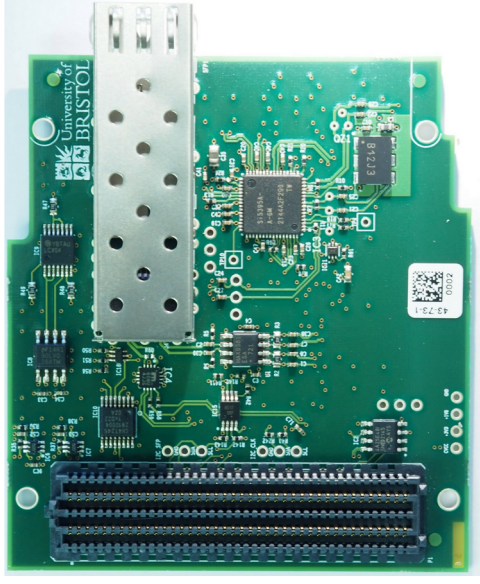


Each board (one per flange) will support up to 8 Camera Boards

Reduce PCB and FW development effort/risk and possibly exploit synergies with STT by using a commercial Zynq mezzanine with a custom base board

Timing system integration

- Bristol designed a reference Timing Endpoint
  - They provide an FMC mezzanine, FW and SW (uses Ipbus)
  - Acts as master or endpoint depending on loaded firmware
- We can plug these in our current VC707 DAQ boards
- Test integration of hardware and firmware and learn how to use software tools



Outlook

Activities that have started or will start in 2024:

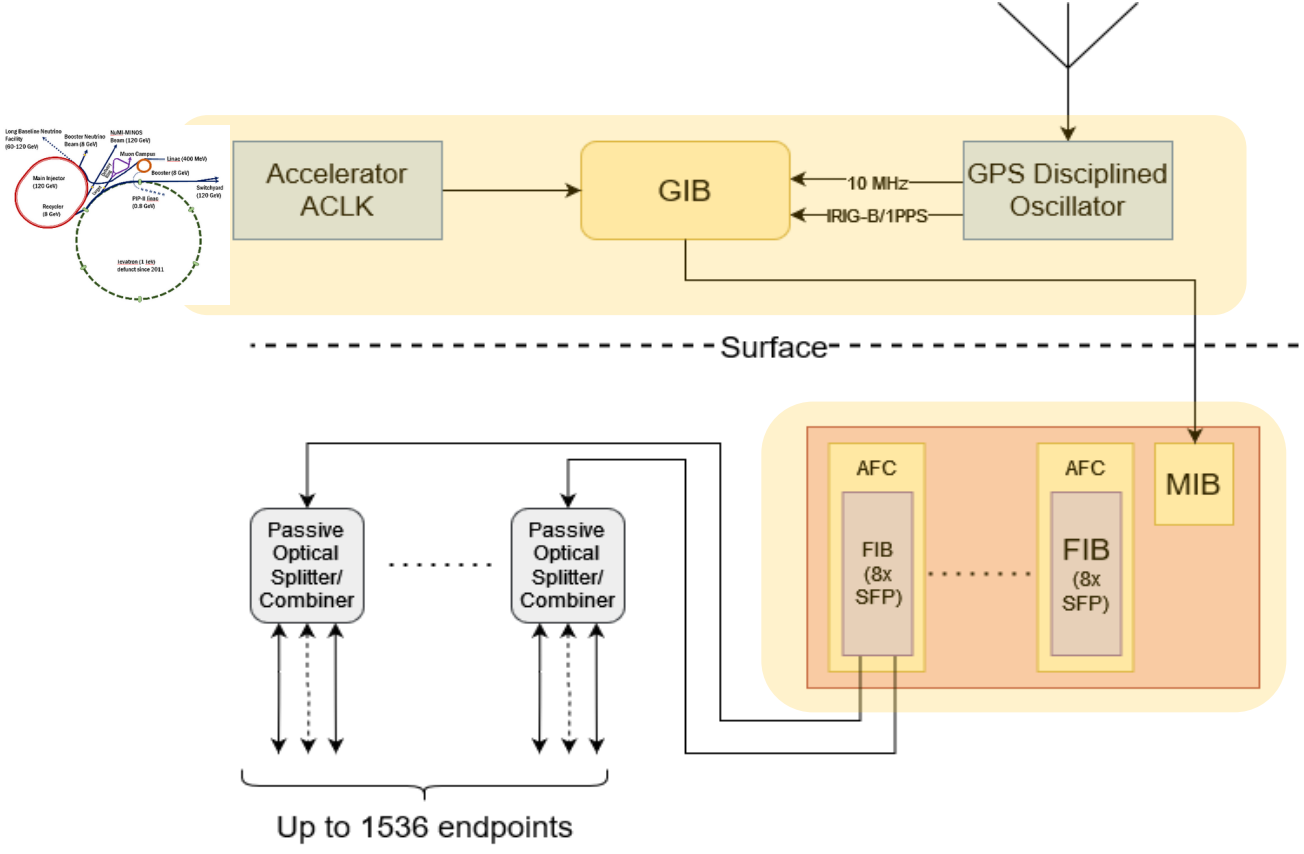
- ASIC development
- DUNE Timing System integration testing
- D-Sub connector tests with flanges

Plans for 2025:

- Design mock-up camera boards and cold interface board
- Begin design of Warm Interface Board

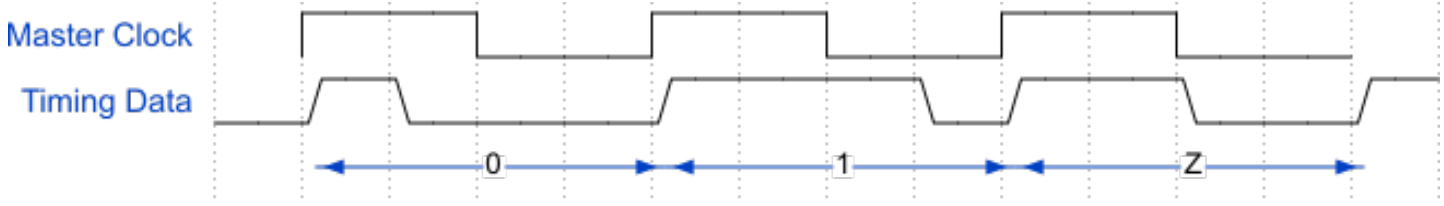
Backup slides

ND Timing System Overview



Dune Timing System signal

- Single mode fibre carrying clock and synchronization messages
  - 62.5 MHz clock (recovered from data stream)



  - Data carries periodic timestamps and synchronous commands
  - Syncs by timestamping an event and broadcasting a message
- Clock edges at timing endpoint aligned to each other to O(100ps), long term, over 1500 endpoints
  - Down to <10 ps within a spill and a small group of endpoints