The New ASIC for GRAIN

ASIC Specs, Architecture Validation and Project Timeline

INFN-LNF – Project Review
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Stefano Durando

Sofia Blua, Valerio Pagliarino, Angelo Rivetti

Parameter	Value
SiPM Size	2 x 2 mm^2 (140 pF) 3 x 3 mm^2 (500 pF)
# Channels/ASIC	1024
Operating Temperatures	300 K – 77 K
<Power Consumption>	5 W / cm^2 ◊
Duty Cycle	On ≥ 9.6 µs (50 µs) Off ◊◊ < 0.1 s
Measurements:	**Q – ToA - ToT**
Integrator Dynamic Range	> 100 PE
RMS_{ToA} (first PE)	100 ÷ 150 ps / 1PE
RMS_{ToT}	≈ ns
Threshold	0.5 x 1PE
SNR	30

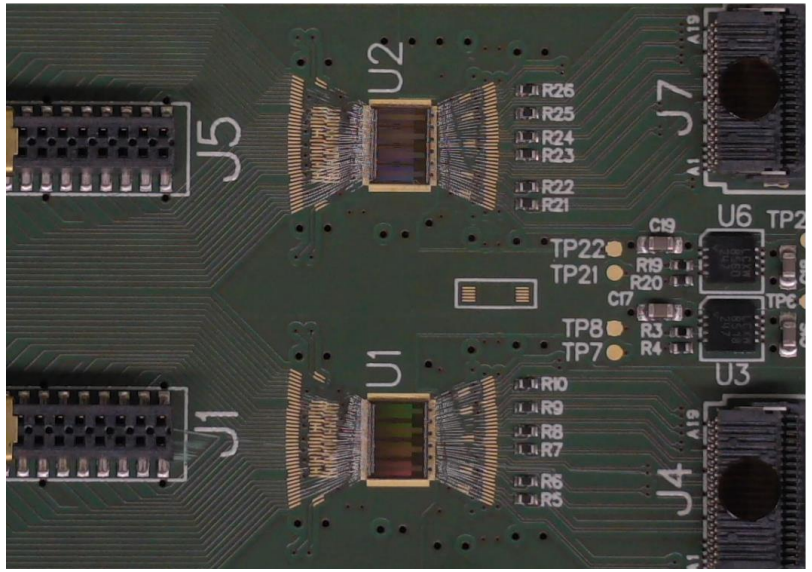
◊ Set by the cryogenic condition, still under study. ◊◊ Interspill = 1.2 ms - 9.6 µs

ALCOR Parent

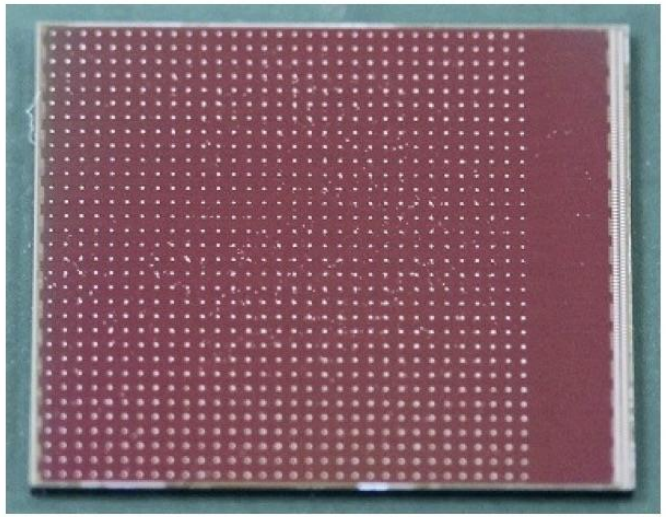
- **Parent ASIC:** R&D with an external company
  - UMC 110 nm
  - 1024 Channels, reading out silicon pixels
  - The ASIC is bump-bonded to the pixels
  - Key IP blocks like the TAC based TDC (30 ps)
  - Basis for the following prototypes

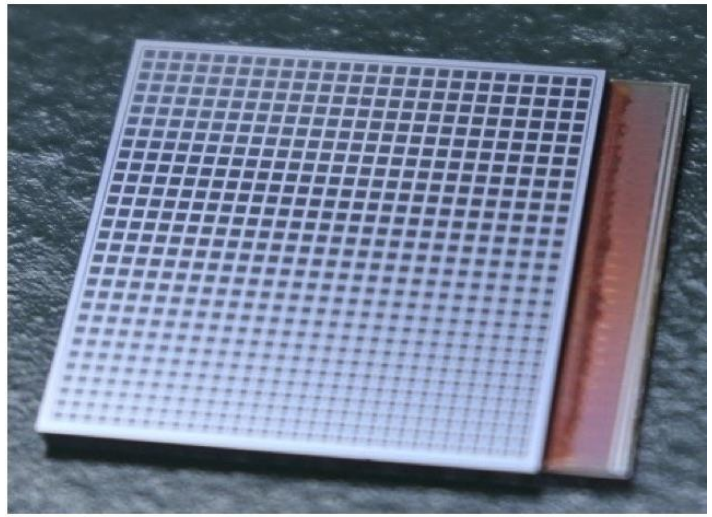
- **ALCOR v1**

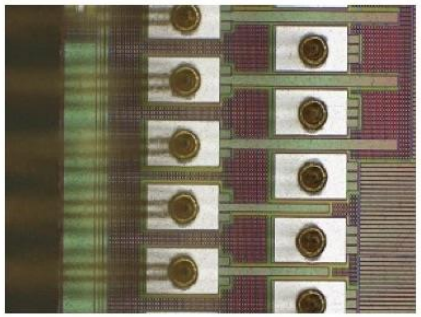
  A **L**ow power **C**hip for **O**ptical sensors **R**eadout

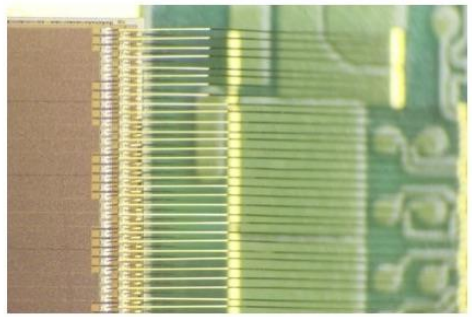


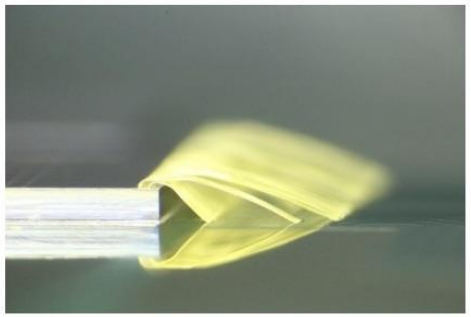
2 ALCOR chips wire bonded on the dedicated board
Courtesy of Fabio Cossio (INFN)









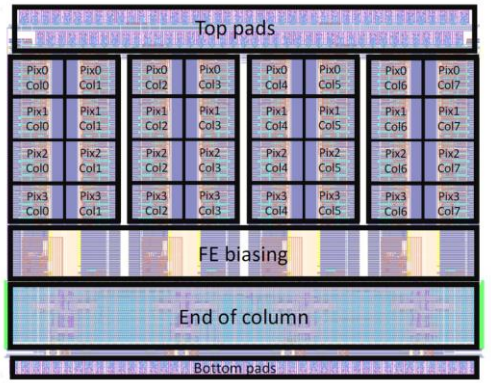


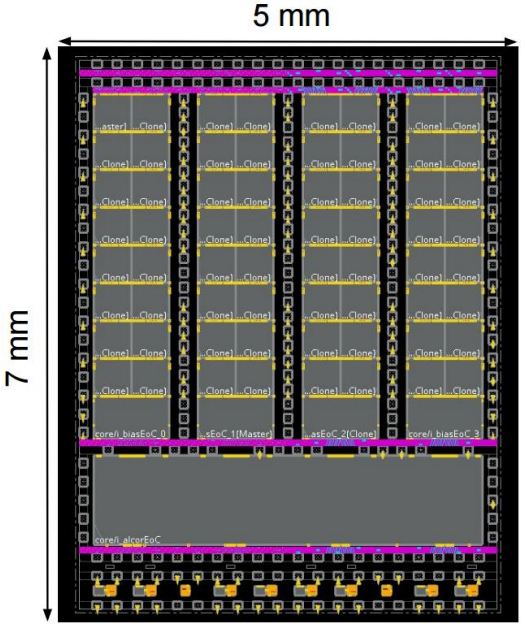
ALCOR's Parent: 1024 pixel channels were bump-bonded to the silicon pixels. The ASIC was wire-bonded on the board

SiPM Readout ASICs at INFN

- **ALCOR v1:** Mixed-signal ASIC for **SiPM** readout, *Darkside* framework (2019)
  (**A** **L**ow power **C**hip for **O**ptical sensors **R**eadout)
  (PhD Thesis, W. Cheng, Polito: https://iris.polito.it/handle/11583/2842529)
  - UMC 110 nm
  - 32 channels, 4.95 x 3.78 mm^2
  - 440 x 440 μm^2 pixel channel
  - Single-photon time tagging and ToT , compatible with both signal polarities
  - LVDS digital output, 320 MHz DDR Tx links
  - ≈12 mW/channel
  - Tested at room temperature and in liquid Nitrogen
- **ALCOR v2.0/.1 and v3** ASICs for the dRICH EIC Detector at BNL (NY, USA)
  (XII Front-End Workshop, Torino, link : https://agenda.infn.it/event/37033/contributions/228026/)
  - Scaled to 64 channels
  - V2.0: 2023 MPW and engineering run, Debugged and optimized for the EIC detector
  - V2.1: 2024 (Jan) Engineerig run, currently under test
  - V3 : Final version, Silicon available in 2025

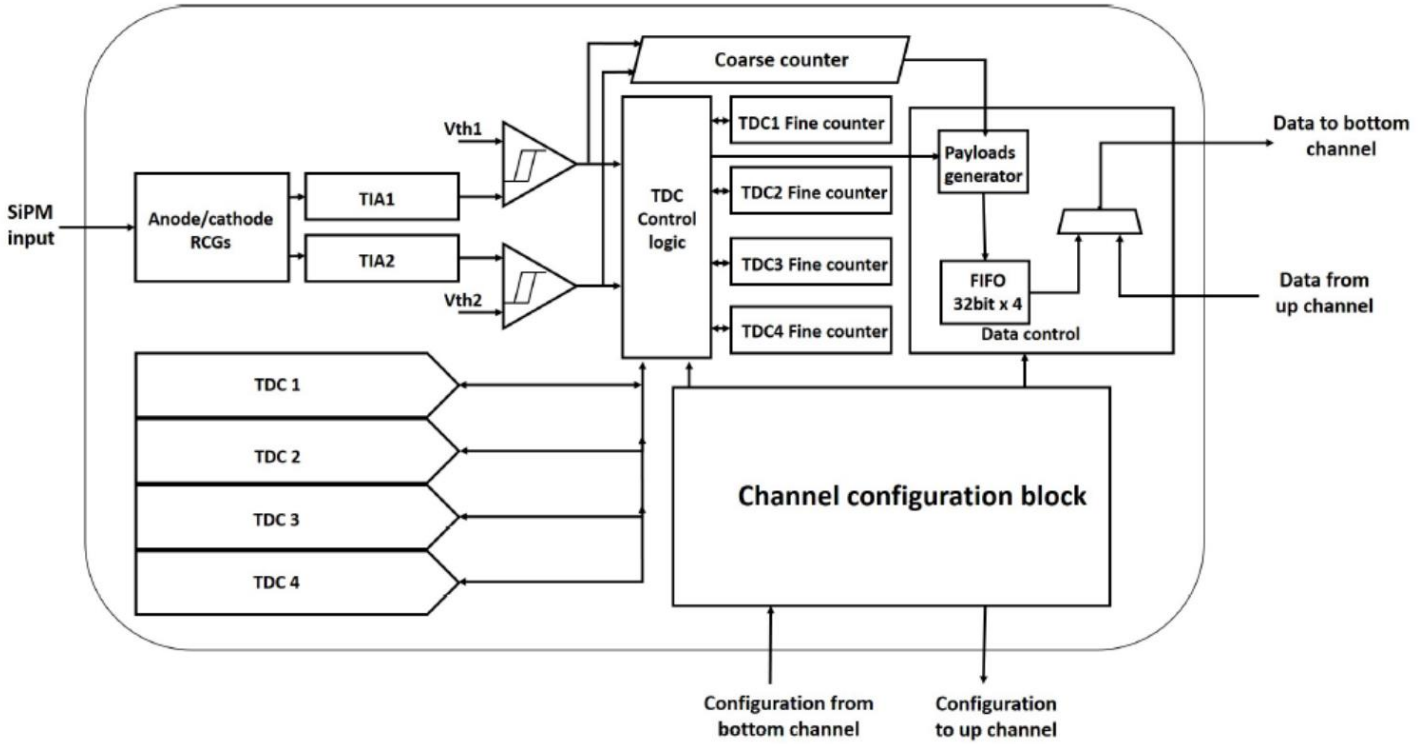
ALCOR v1 Top Cell Layout (F.Cossio)

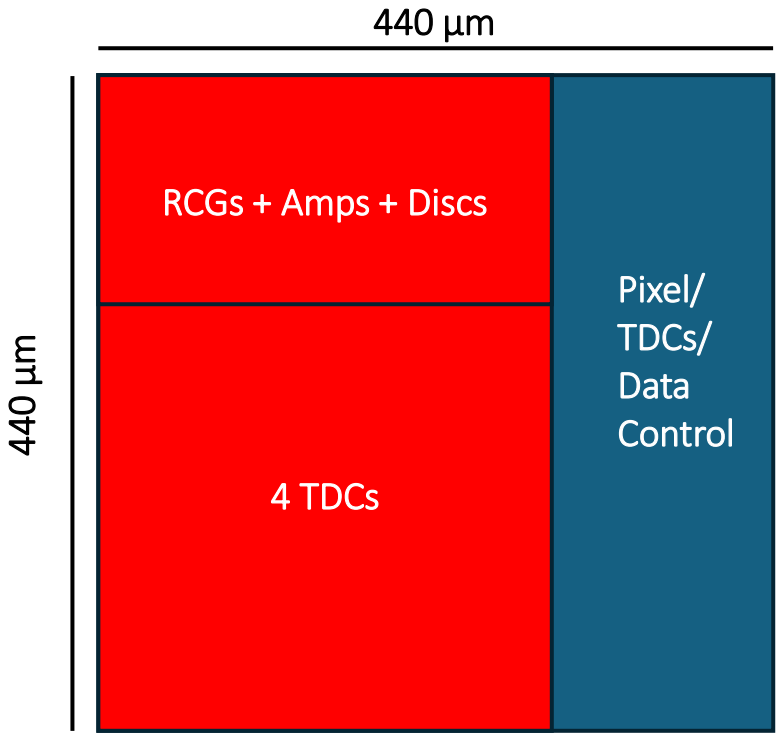




ALCOR v3 Top Cell Layout (F.Cossio)

ALCOR Pixel Scheme



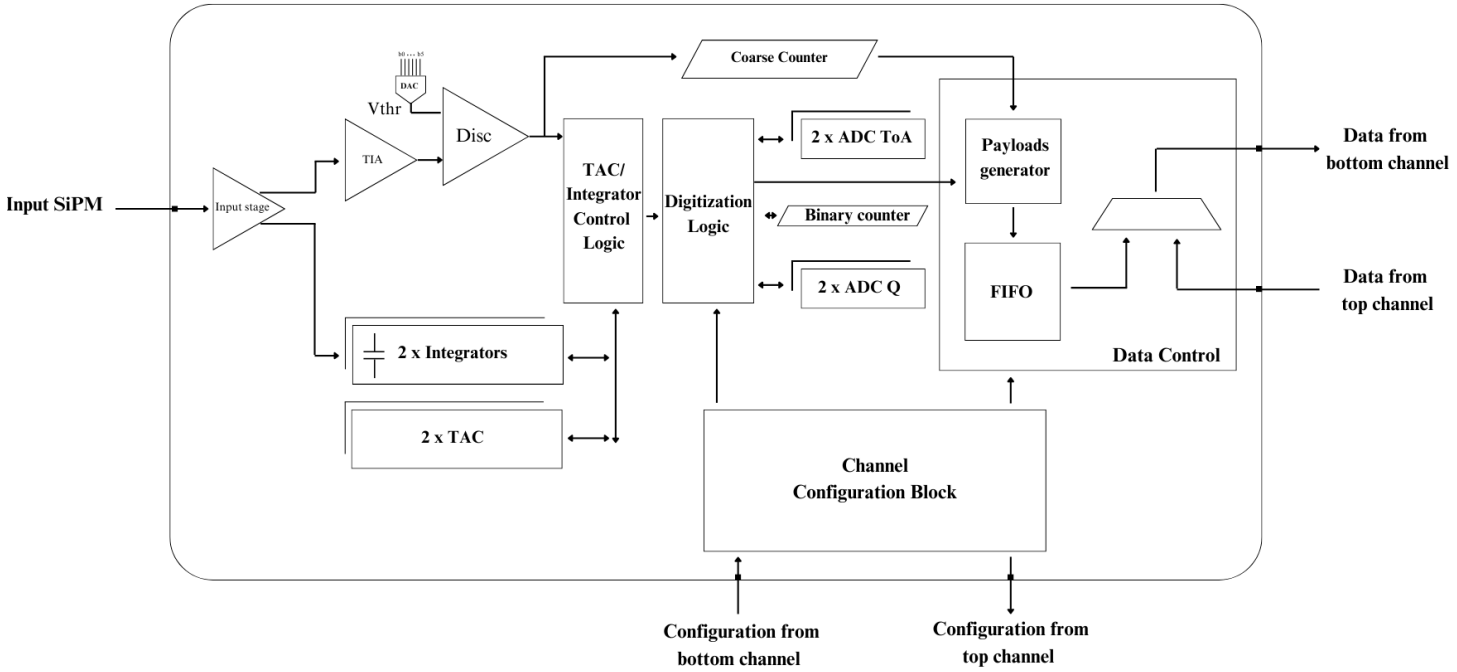


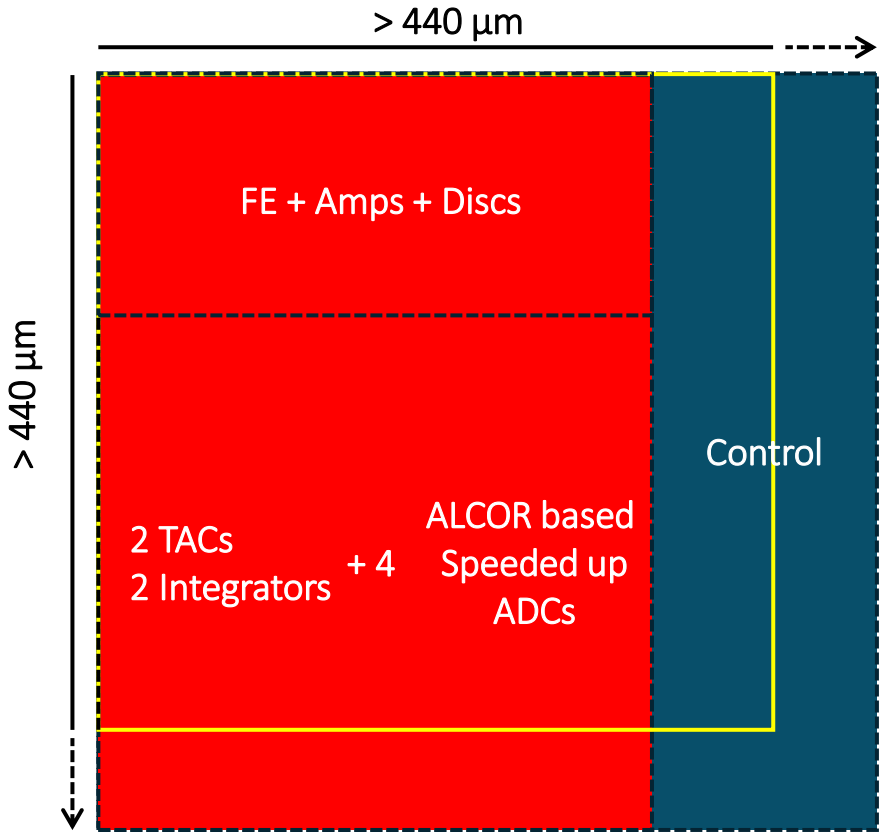
ALCOR v1 pixel

Dominated by the analog blocks (capacitors)

- 2 (Anode/Cathode) Regulated Common Gates (RCGs) Input stage
- 2 Independent Trans-Impedance Amplifiers (TIAs)
- 2 Leading Edge Discriminators (LE Discs)
- 4 TDCs = 4 x (TAC + Wilkinson ADC)
- Control Logic: pixel config, TDCs operation and data transmission

GRAIN ASIC Pixel Scheme





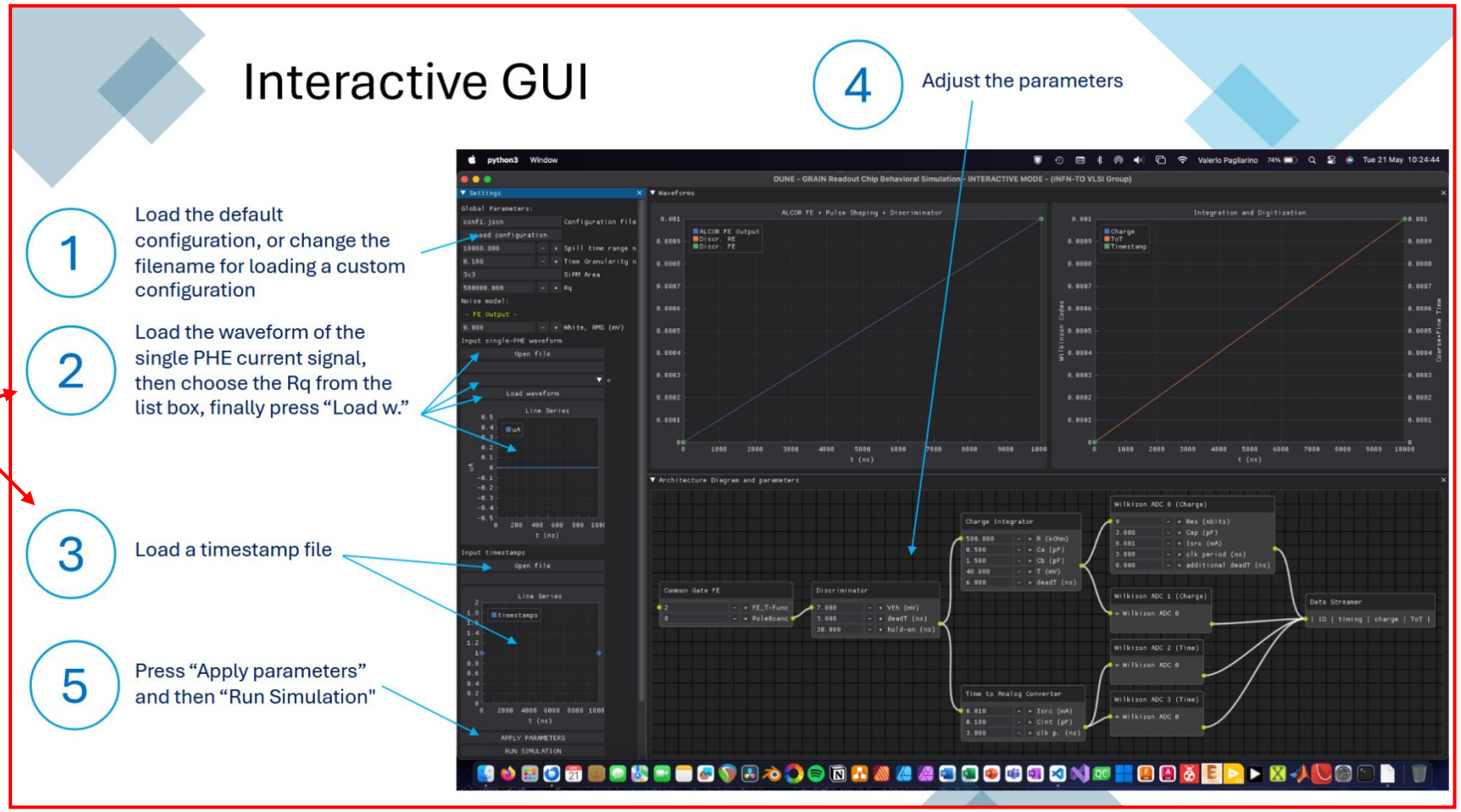
GRAIN ASIC pixel

Based on the ALCOR scheme, with minimum changes:

- Regulated Common Gate input stage
- Time branch:
  - TIA + LE Discriminators
  - 2 Time to Analog Converters (TACs)
- Charge branch
  - 2 Integrators
- 4 Analog to Digital Converters with speed increased up to 4/8 times
- Control: pixel config, ADCs/Integrators/TACs operation and data transmission

Architecture Validation

- **Ongoing validation of the architecture** by the collaboration for GRAIN detector's physics with:
  - Coded aperture masks
  - Lenses
- **Python software** designed in Torino by Sofia Blua and Valerio Pagliarino
  - Inputs: time domain reconstruction of a single spill SiPM event
  - Behavioural model: Ideal description of the pixel electronics' response
  - Output: numpy array (ASIC-like output)
- **First results suggest the proposed architecture meets the requirements**



Courtesy of Sofia Blua and Valerio Pagliarino

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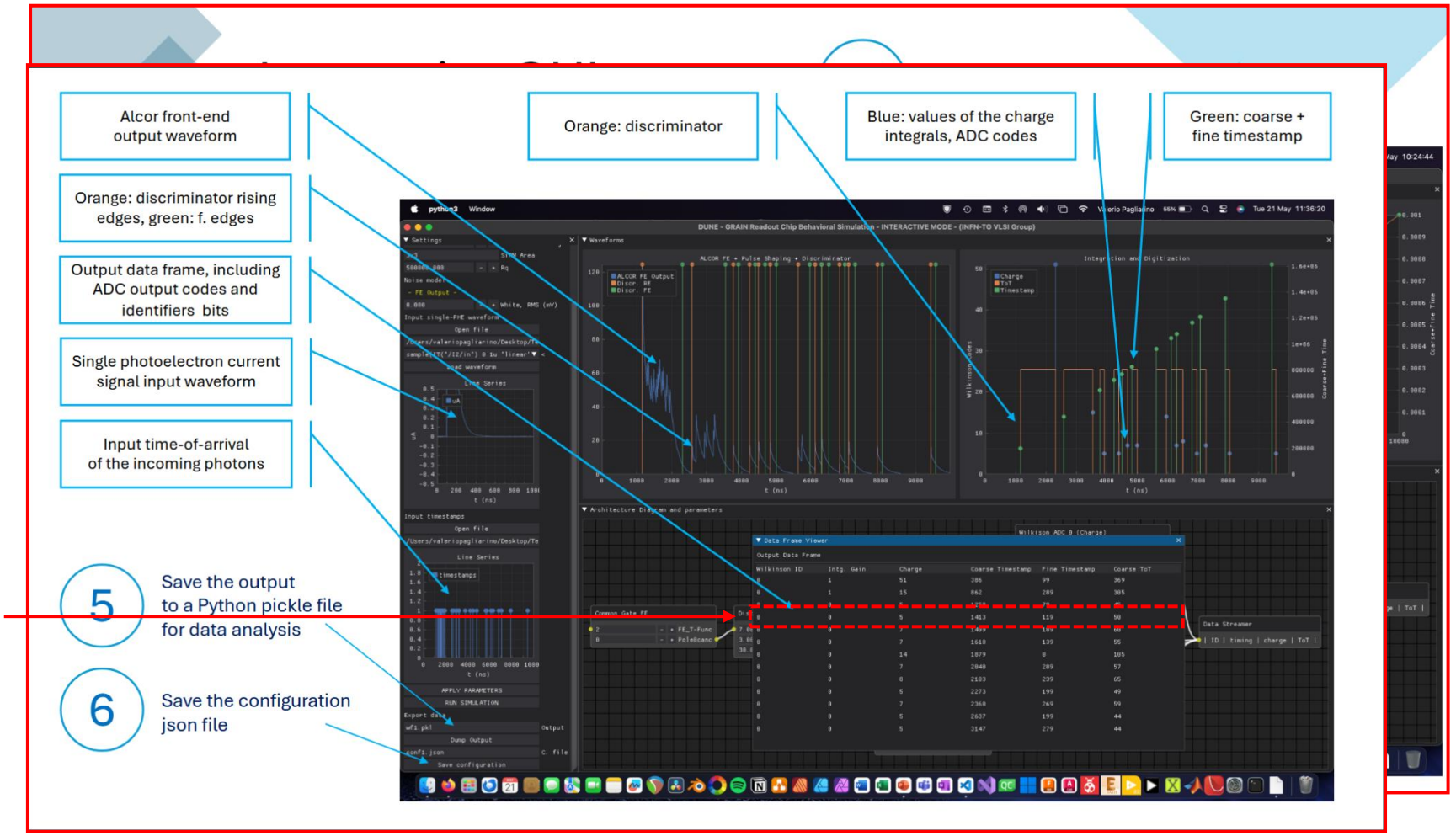
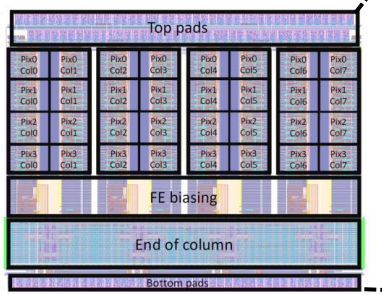


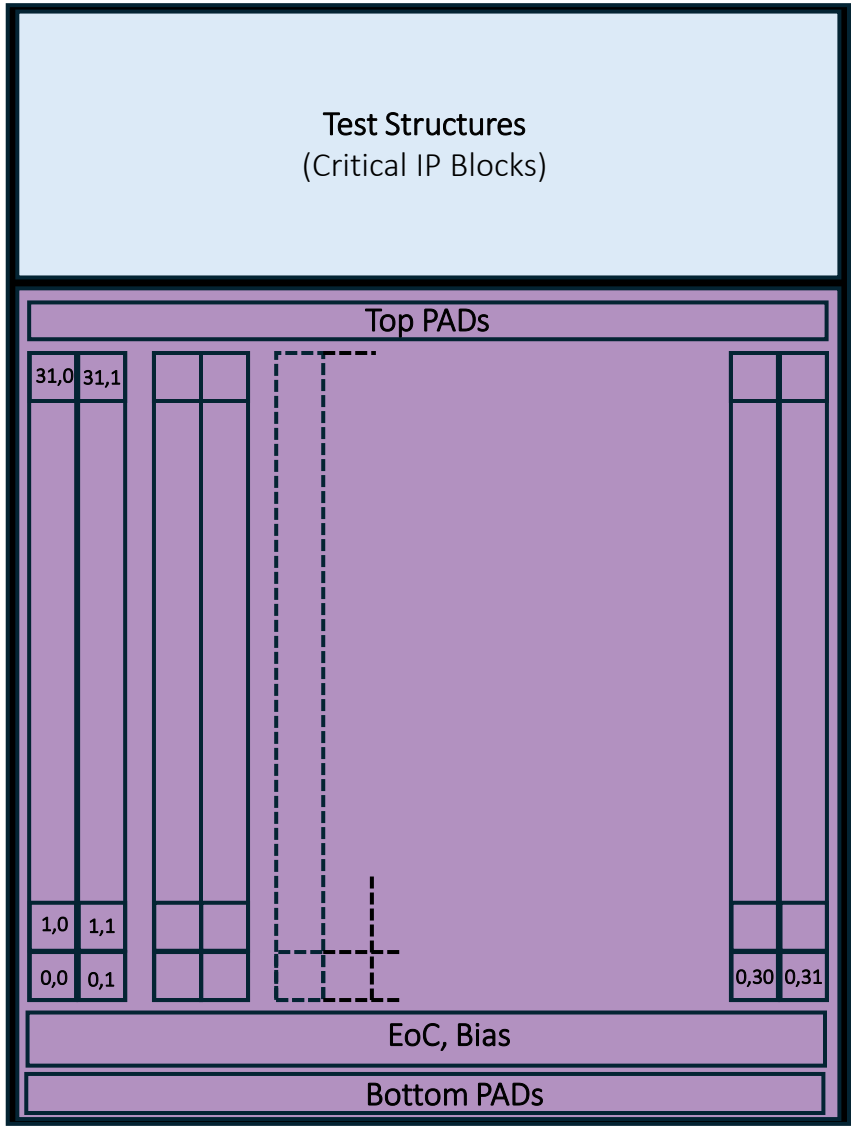
Courtesy of Sofia Blua and Valerio Pagliarino

GRAIN ASIC Floorplan

- ALCOR: 32 → GRAIN: 1024 channels = 32 x 32 pixels matrix
- Wafer reticle size : 20.340 mm x 31.840 mm
  - Safe circuit size < 20 mm x 20 mm
  - Hp: pixel channel pitch ≈ 500 µm
    → 32 x 500 µm = 16 mm + EoC, Biasing and PADFrame
- Advanced packaging techniques:
  - ASIC bump bonded to interposer for SiPMs and PCB board connection
    - On pixel PAD for SiPM
    - Inter-column supply and ground PADs to reduce IR drops
- Pin out under discussion:
  - Power Domains
    - 3 Analog + 3 Digital
  - Differential:
    - 1 Clk + 3 SPI
      + 1 trigger +2 Data
  - Single ended
    - 1 Reset + 1 Global_EN
      + 1 Low Power



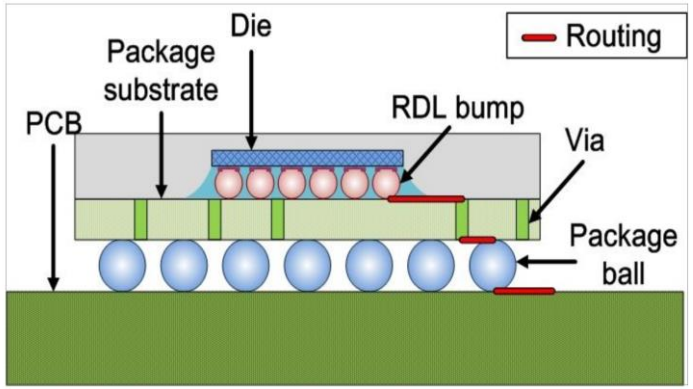
ALCOR v1



GRAIN ASIC

Flip-Chip BGA package

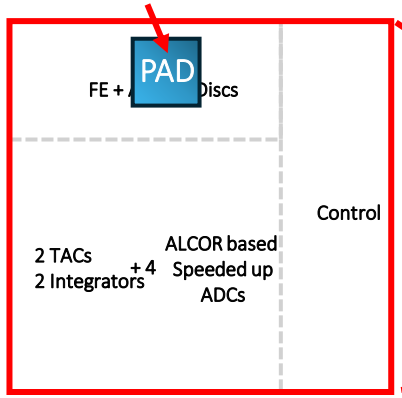
- The ASIC is bump-bonded to an interposer connected to the board with package balls
  - On-pixel PAD for SiPM
  - Inter-column supply and ground PADs for reduced IR drops
- Similar approach is followed for ALCOR v3 implementation for EIC



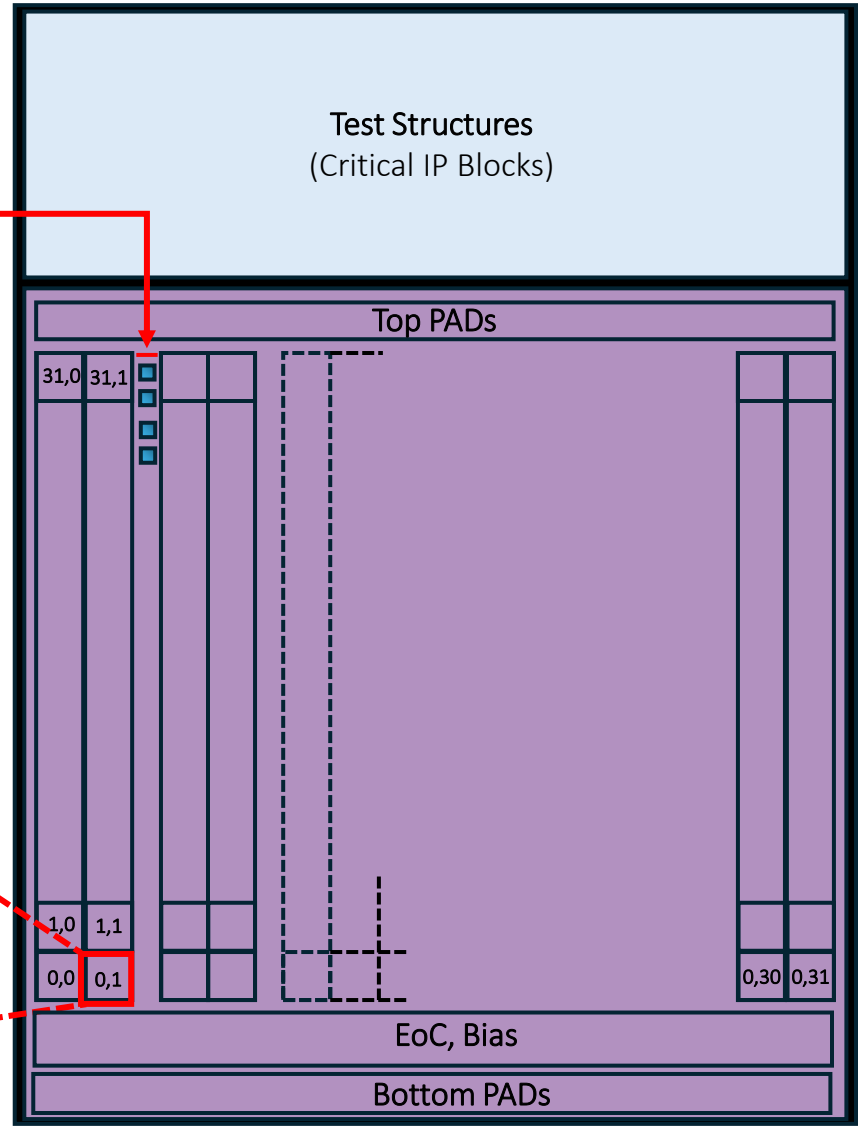
Flip-chip BGA working principle

Hsu, Hsin-Wu & Chen, Meng-Ling & Chen, Hung-Ming & Li, Hung-Chun & Chen, Shi-Hao. (2012). On effective flip-chip routing via pseudo single redistribution layer. 1597-1602.

10.1109/DATE.2012.6176727.

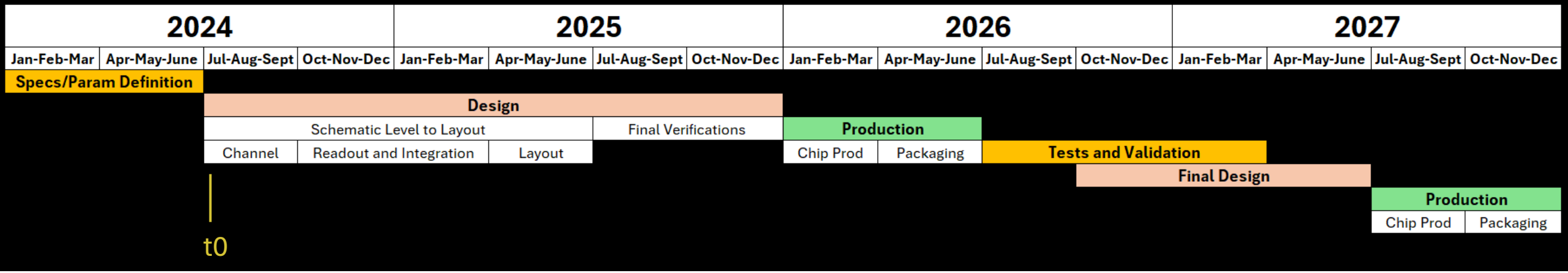


GRAIN ASIC : Pixel Channel

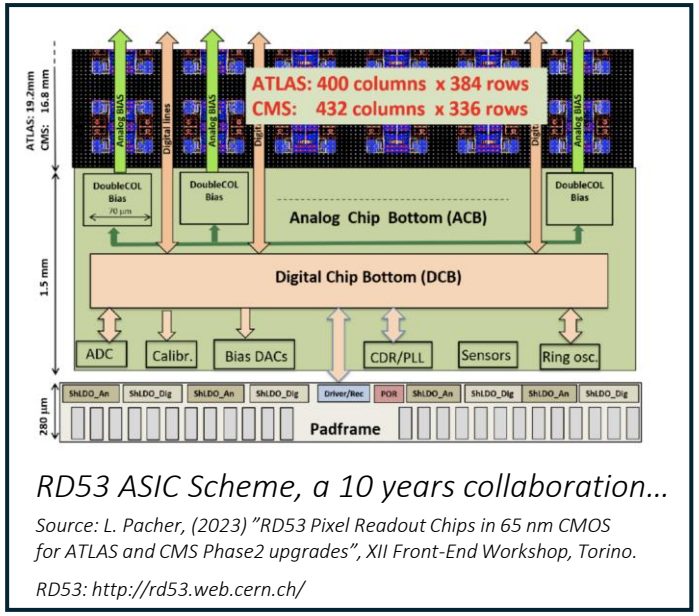


GRAIN ASIC

Timeline



- The new ASIC for GRAIN:
  - Leveraging expertise from previous and ongoing developments
  - Implementation of silicon-prooved IP blocks shorten the development time
- 2 Engineering runs:
  - A 1024 demonstrator tape-out scheduled for the end of December 2025
  - Last submission with bug fixes in October 2026
- Ongoing and future activities:
  - Architecture validation
  - New blocks and digital control design, floorplan and pin-out
  - Test board and packaging under study, production once the PADframe will be freezed (Dec 2025)



RD53 ASIC Scheme, a 10 years collaboration…

Source: L. Pacher, (2023) "RD53 Pixel Readout Chips in 65 nm CMOS for ATLAS and CMS Phase2 upgrades", XII Front-End Workshop, Torino.

RD53: http://rd53.web.cern.ch/


THANKS