Readout ASIC for SiPM Arrays in the GRAIN Liquid Argon Detector

Activity Report

DUNE Collaboration Meeting, Ferrara
29/10/2024

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ASIC Requirements: Signal Waveforms

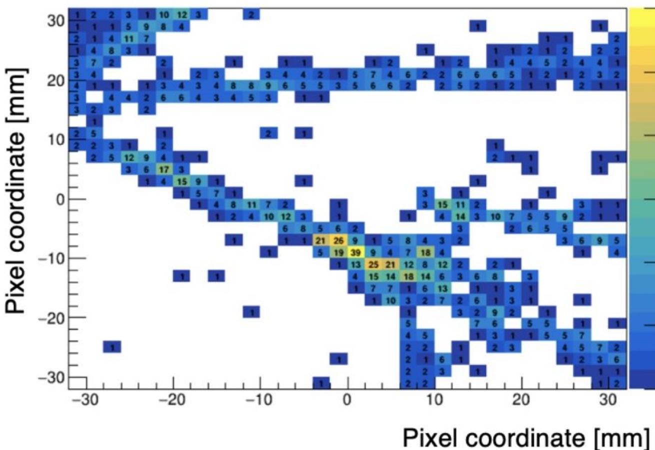
Simulation for a matrix of 2 x 2 mm^2 SiPM with the optical lenses approach

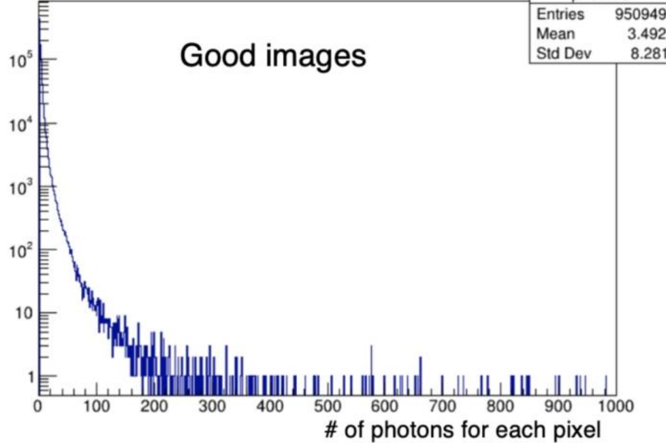
SiPM signals to be readout have a complex structure:

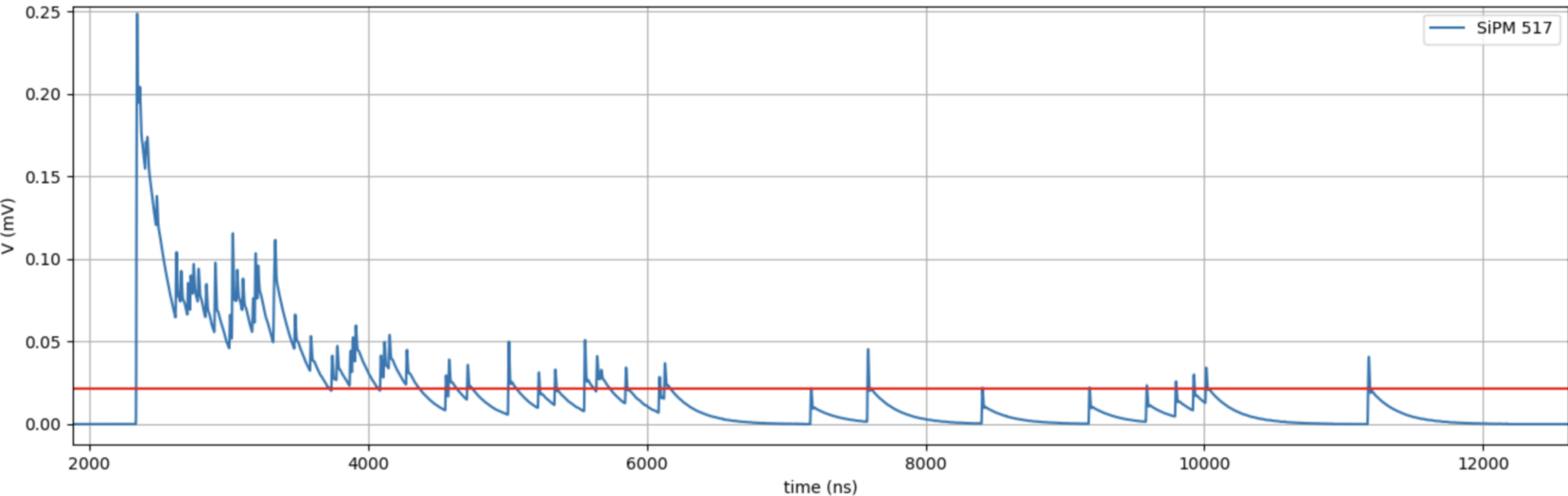
- Single photon and large number of piled-up photons.

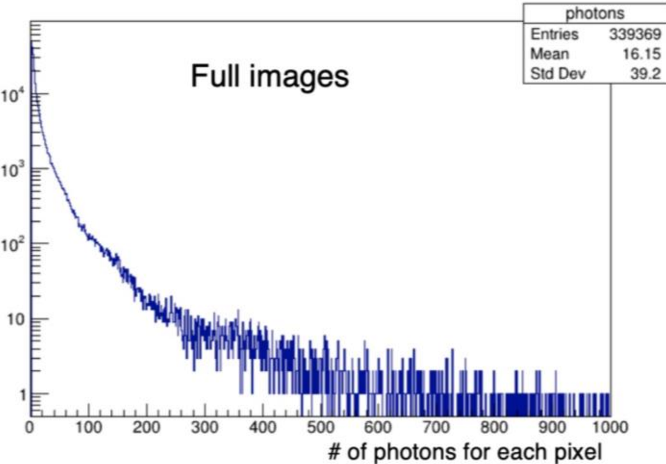
The ASIC must:

- **Detect single photons** (threshold = 0.5 p.e.)
- **Timestamp** the Maximum Number of Events
- **Count the photons** while minimizing the unintegrated and undigitized charge









Plots from "ASIC requirements for GRAIN optical detector readout" – A. Caminata et al

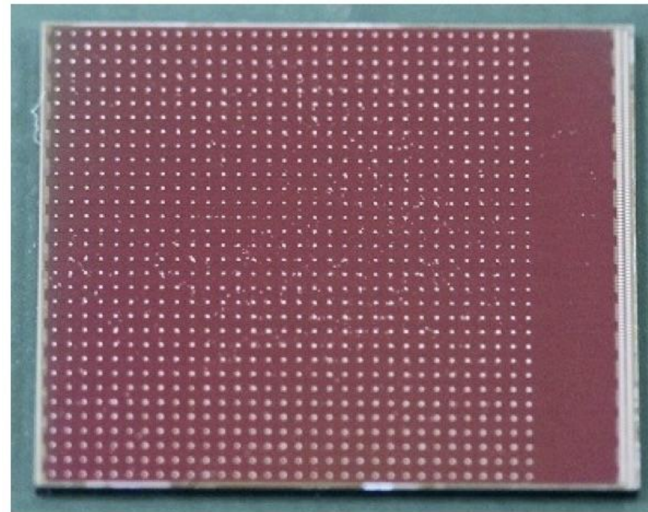
INFN

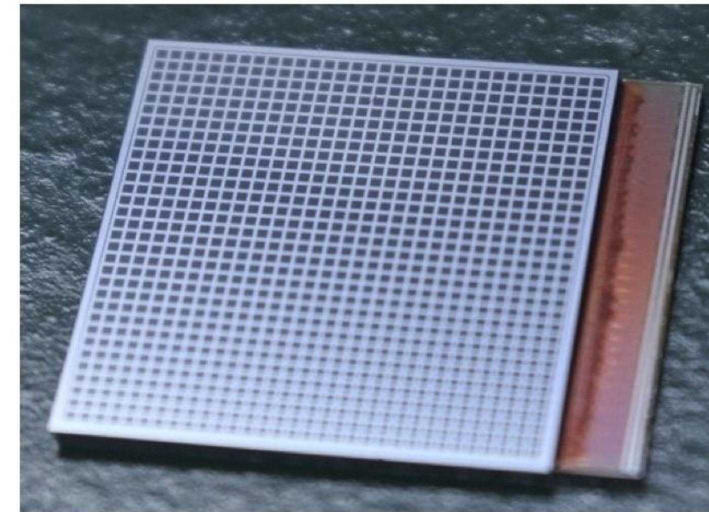
Features	ASIC for GRAIN
Channel Modularity	1024
SiPM Size	$2 \times 2\ mm^2$ / 100s pF
Measurements	ToA, ToT, Charge Integral
Single Photon Time of Arrival Resolution	100 ps
Time over Threshold Resolution	1 ns
Charge Integration Response	Bilinear
Charge Integral Resolution	9 bit: 10 codes/phe; 3 codes/phe
Charge Dynamic Range	[1 - 25 phe]; [25 - 150 phe]
AVG Power Density	10 mW/ channel
Silicon Die Size	$20 \times 20\ mm^2$ (Reticle Size)
Operating Temperature	77 K – 300 K
Number of LVDS tranceivers	32 = 1 x Column
LVDS Transceiver Speed	320 Mbps SDR
Clock Frequency	310 – 325 MHz
Power Gating Feature	DUNE-compatible

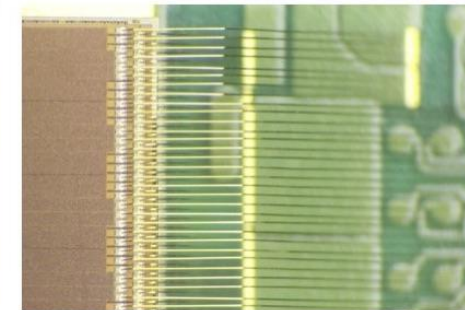
INFN Background in 1024 Channels ASICs

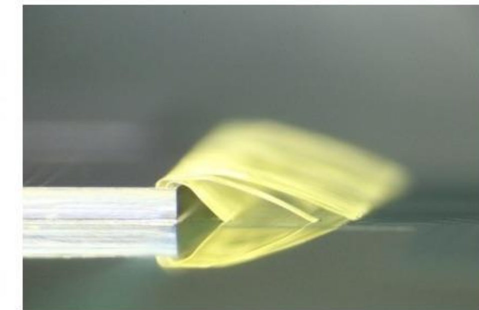
- **Parent ASIC:** R&D with an external company
  - UMC 110 nm
  - 1024 Channels, reading out silicon pixels
  - The ASIC is bump-bonded to the pixels
  - Key IP blocks like the TAC based TDC (30 ps)
  - Basis for the following prototypes

- **ALCOR v1**
  A **L**ow power **C**hip for **O**ptical sensors **R**eadout

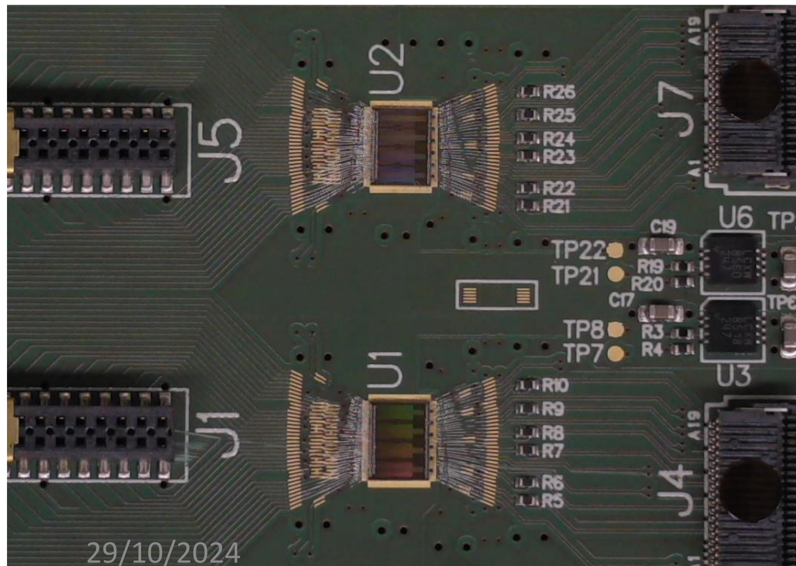








ALCOR's Parent: 1024 pixel channels were bump-bonded to the silicon pixels. The ASIC was wire-bonded on the board

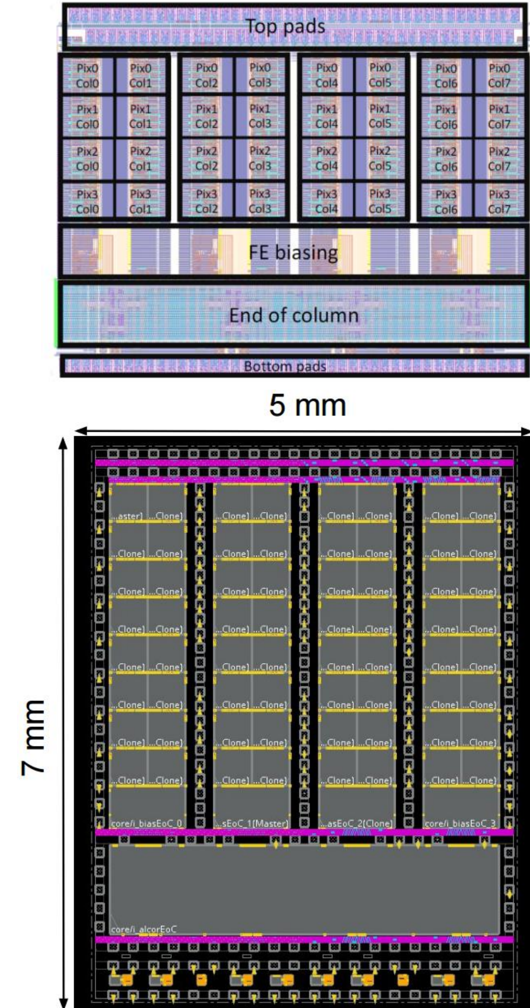


2 ALCOR chips wire bonded on the dedicated board
Courtesy of Fabio Cossio (INFN)

SiPM Readout ASICs at INFN

- **ALCOR v1:** Mixed-signal ASIC for **SiPM** readout, *Darkside* framework (2019)
  (**A** **L**ow power **C**hip for **O**ptical sensors **R**eadout)
  (PhD Thesis, W. Cheng, Polito: https://iris.polito.it/handle/11583/2842529)
  - UMC 110 nm
  - 32 channels, 4.95 x 3.78 mm^2
  - 440 x 440 μm^2 pixel channel
  - Single-photon time tagging and ToT , compatible with both signal polarities
  - LVDS digital output, 320 MHz DDR Tx links
  - ≈12 mW/channel
  - Tested at room temperature and in liquid Nitrogen
- **ALCOR v2.0/.1 and v3** ASICs for the dRICH EIC Detector at BNL (NY, USA)
  (XII Front-End Workshop, Torino, link : https://agenda.infn.it/event/37033/contributions/228026/)
  - Scaled to 64 channels
  - V2.0: 2023 MPW and engineering run, debugged and optimized for the EIC detector
  - V2.1: 2024 (Jan) Engineerig run, currently under test
  - V3 : Final version, Silicon available in 2025

ALCOR v1 Top Cell Layout (Courtesty of F.Cossio)



Features	ASIC for GRAIN	ALCOR v3
Channel Modularity	1024	64
Measurements	ToA, ToT, Charge Integral	ToA,ToT
Single Photon Time of Arrival Resolution	100 ps	150 ps
Time over Threshold Resolution	1 ns	1 ns
Charge Integration Response	Bilinear	N.A.
Charge Integral Resolution	9 bit: 10 codes/phe; 3 codes/phe	N.A.
Charge Dynamic Range	[1 - 25 phe]; [25 - 150 phe]	N.A.
AVG Power Density	10 mW/ channel	10 mW/ channel
Silicon Die Size	20 x 20 mm^2 (Reticle Size)	4.95 x 3.78 mm^2
Operating Temperature	77 K – 300 K	300 K
Number of LVDS tranceivers	32 = 1 x Column	8 = 1 x Column
LVDS Transceiver Speed	320 Mbps SDR	320 Mbps SDR; 640 Mbps DDR
Clock Frequency	310 – 325 MHz	310-325 MHz
Power Gating Feature	DUNE-compatible	No

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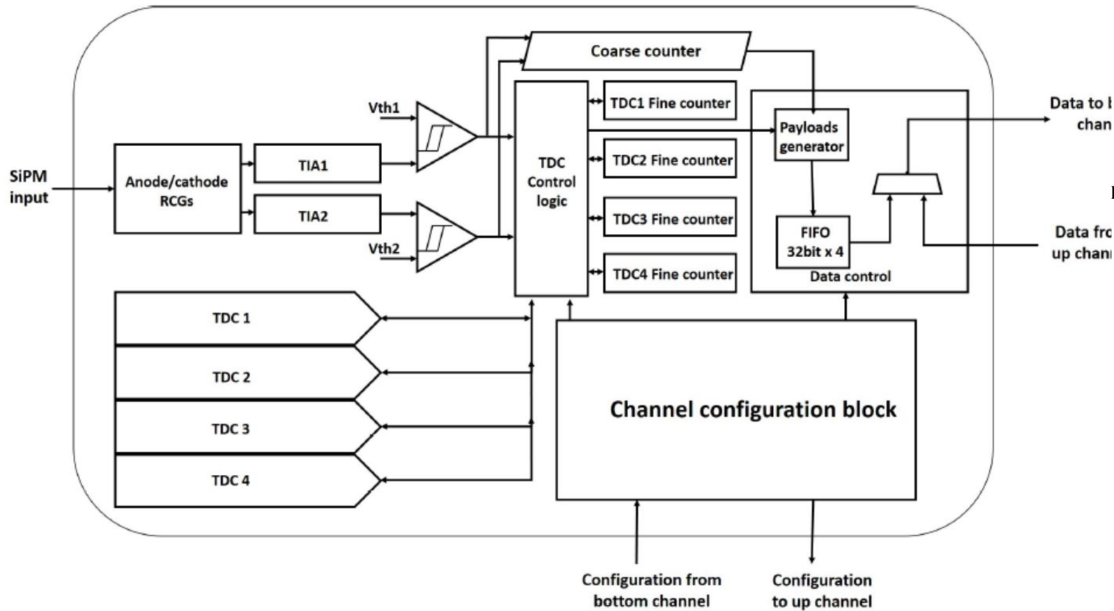
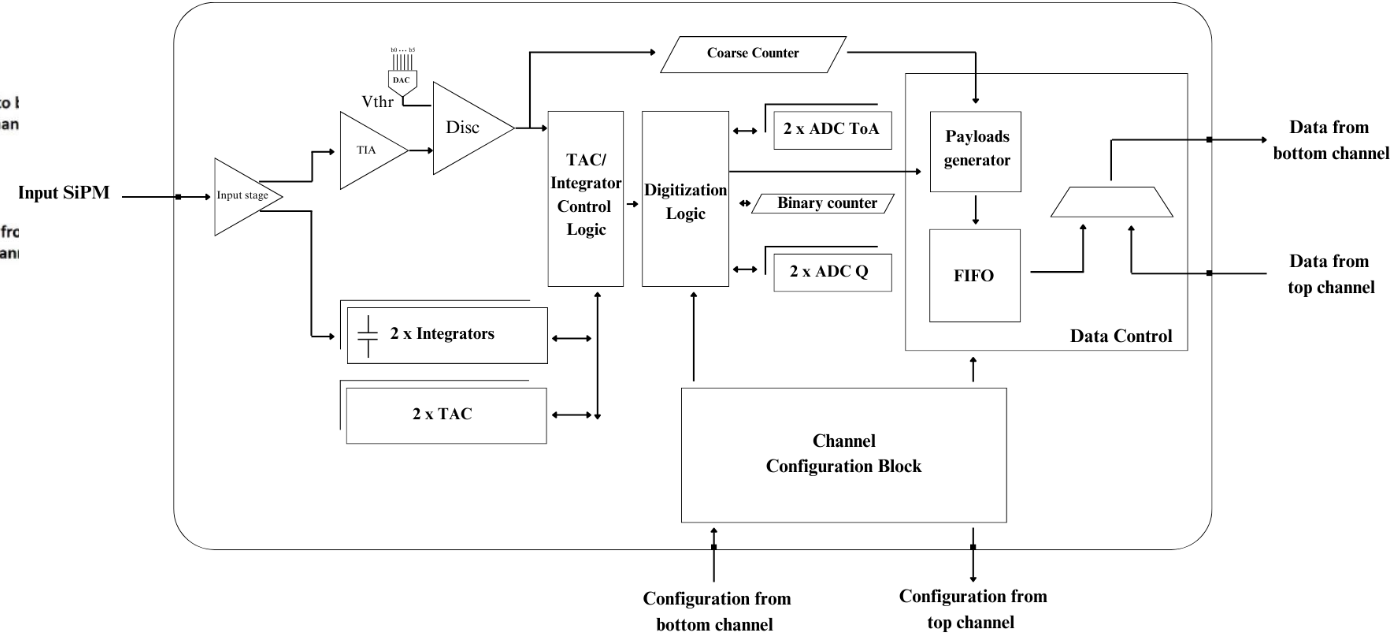
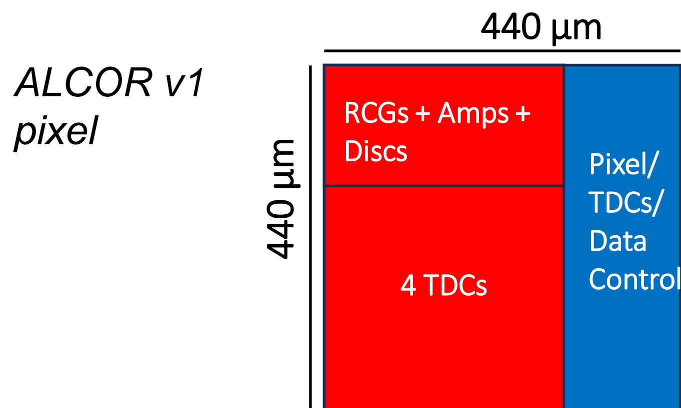
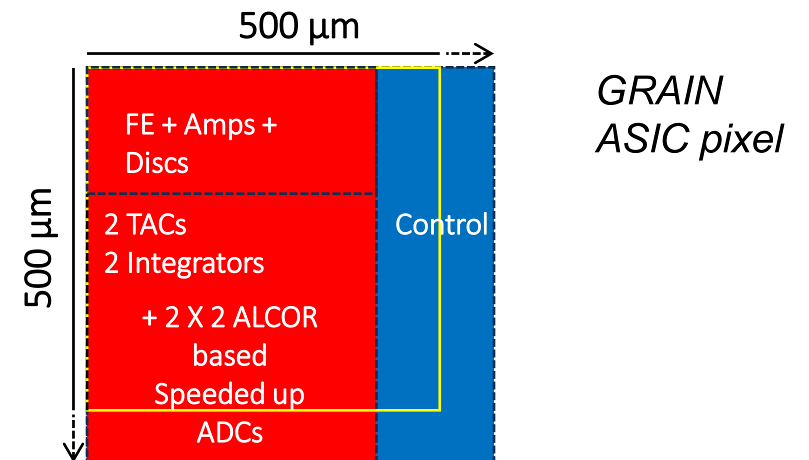
Upgrading the ALCOR Pixel





ALCOR v1 pixel





GRAIN ASIC pixel

A Reticle Size ASIC

1024 channels ASIC (32 x 32)

Wafer reticle size: 20.340 x 31.840 mm²

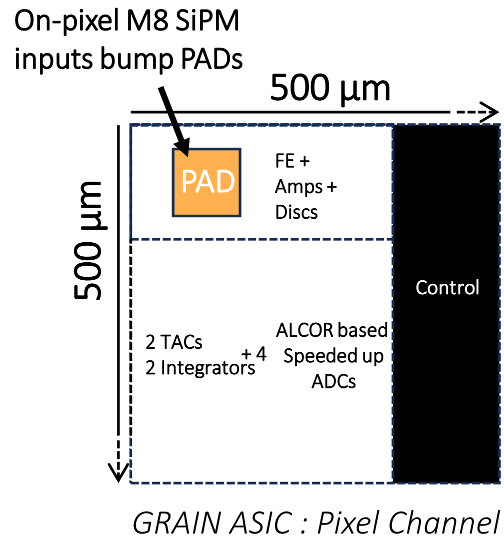
- Safe circuit size < 20 mm x 20 mm
- Hp: pixel channel pitch ≈ 500 µm

→ 32 x 500 µm = 16 mm + EoC, Biasing, Tx

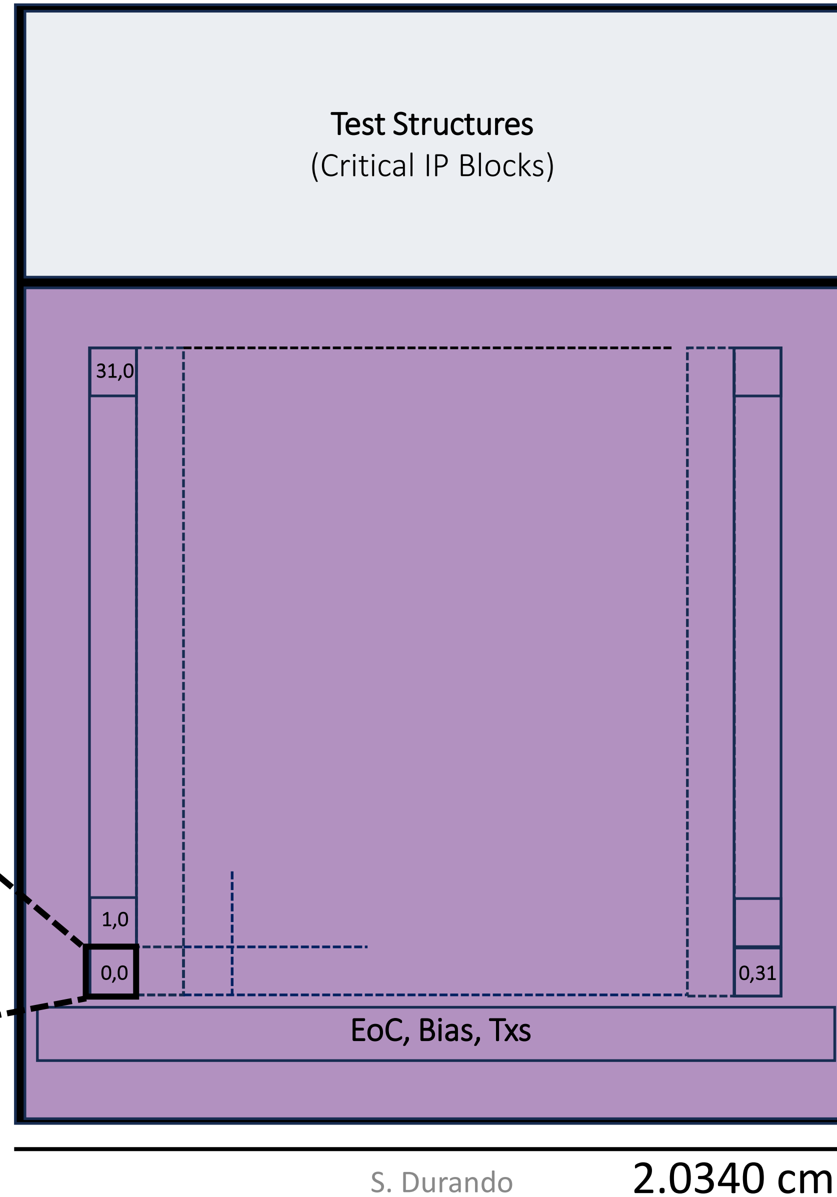
High density I/O:

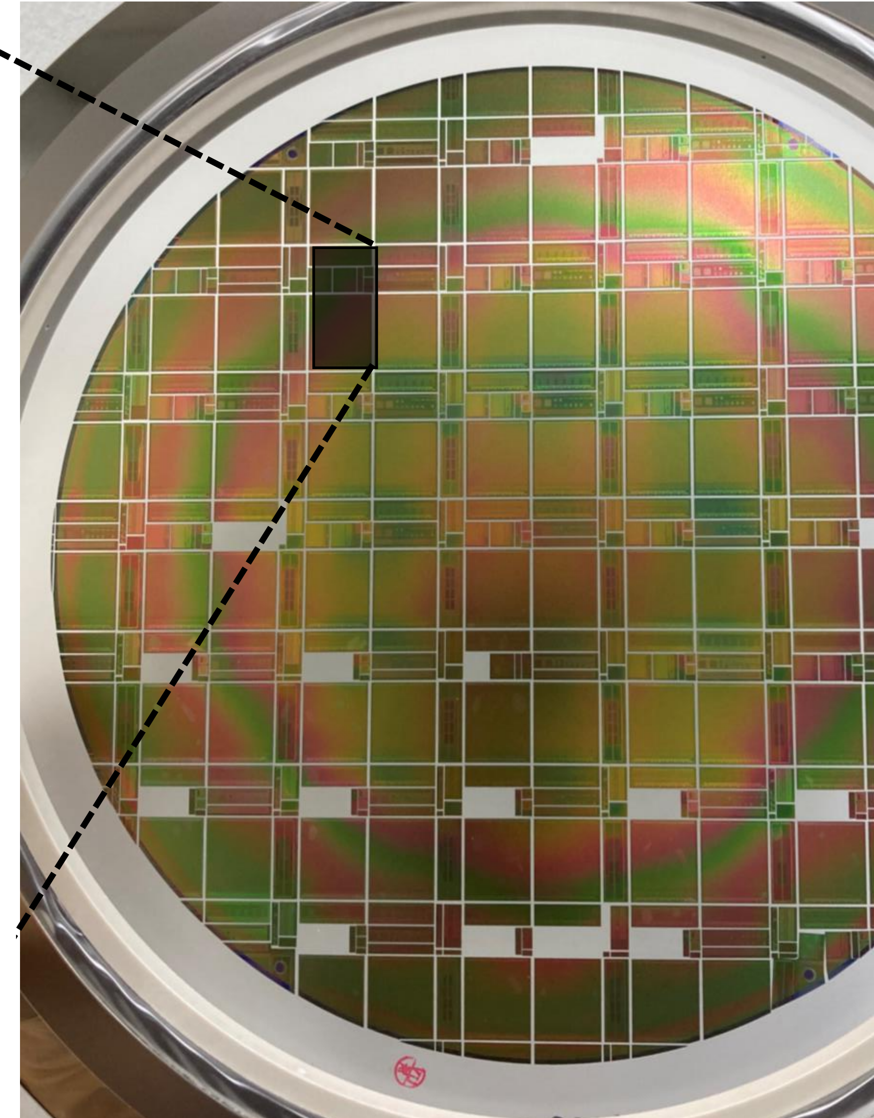
- Advanced packaging techniques

Pin out under discussion



GRAIN ASIC : Pixel Channel





Courtesy of the ARCADIA collaboration

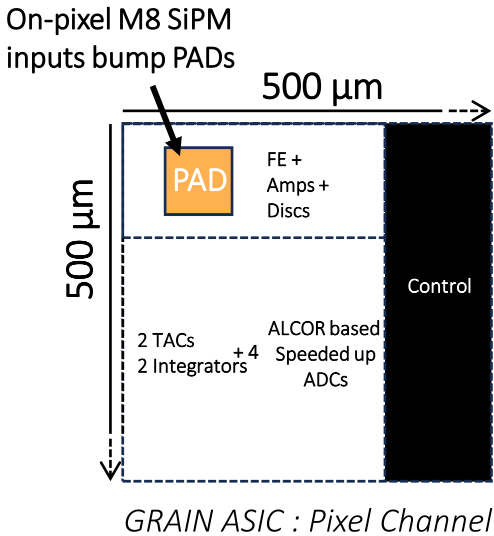
Note: The ASIC has not yet been submitted

A Reticle Size ASIC

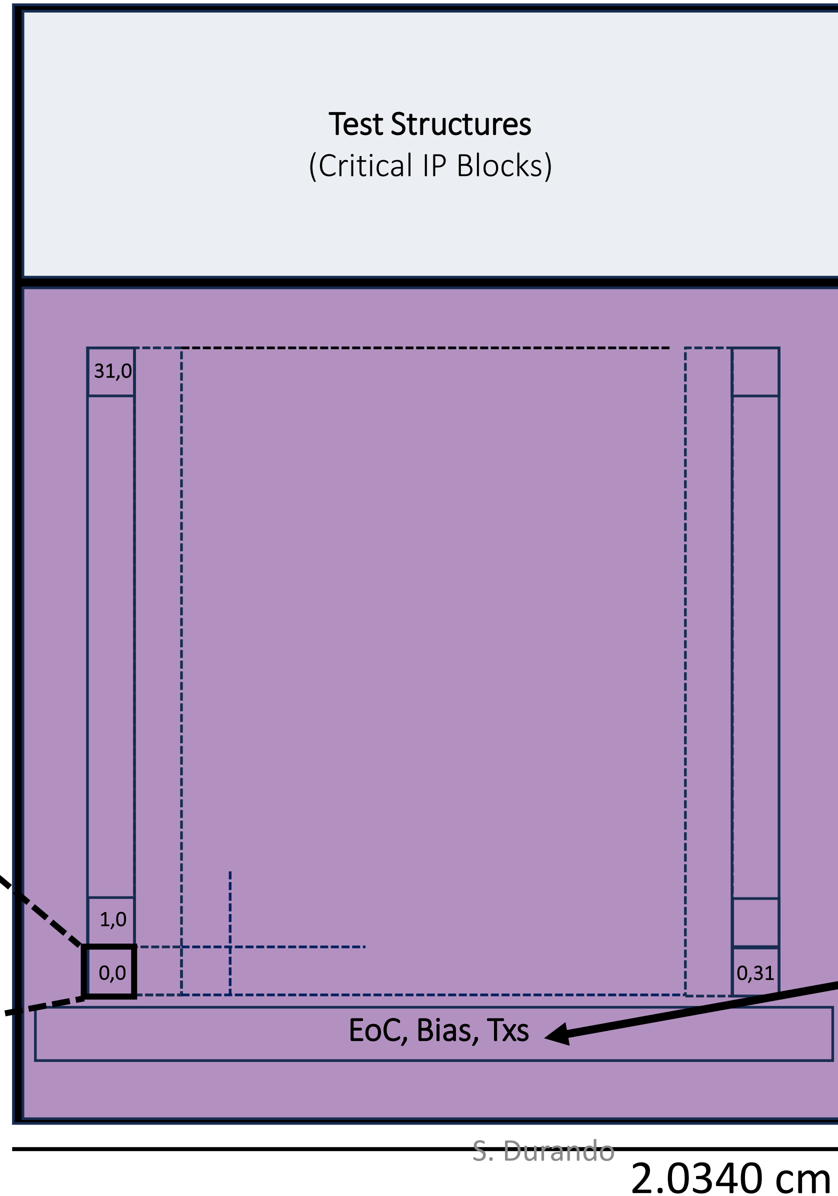
End-of-column LVDS with high-impedance mode, allowing multiple columns to share the same LVDS trace via Time-Division Multiplexing (TDM).

An access token passed among the columns authorizes transmission.

Various link aggregation configurations are supported, from 32 separate pairs to a single LVDS pair.



GRAIN ASIC : Pixel Channel

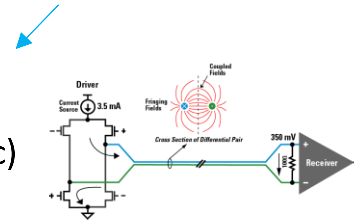


In the GRAIN detector the number of LVDS feedthrough in the cryostat must be limited!

- Very high cost of high-speed connectors
- Load for cryocoolers

Link aggregation

- **MAX BW:**
  32 LVDS channels:
  320 Mbps / column (32 c)
- **MIN BW**:
  1 LVDS channel:
  10 Mbps / column (32 c)



Timeline

2024				2025			
Jan-Feb-Mar	Apr-May-June	Jul-Aug-Sept	Oct-Nov-Dec	Jan-Feb-Mar	Apr-May-June	Jul-Aug-Sept	Oct-Nov-Dec
Specs/Param Definition							
		Design					
		Schematic Level to Layout				Final Verifications	
		Channel	Readout and Integration		Layout		

2026				2027			
Jan-Feb-Mar	Apr-May-June	Jul-Aug-Sept	Oct-Nov-Dec	Jan-Feb-Mar	Apr-May-June	Jul-Aug-Sept	Oct-Nov-Dec
Production							
Chip Prod	Packaging	**Tests and Validation**					
			Final Design				
						Production	
						Chip Prod	Packaging

Architecture Validation

- **Validation of the architecture** by the collaboration for GRAIN detector's physics with:
  - Coded aperture masks
  - Lenses
- **Python software** designed in Torino by Sofia Blua and Valerio Pagliarino
  - Inputs: time domain reconstruction of a single spill SiPM event
  - Behavioural model: Ideal description of the pixel electronics' response
  - Output: numpy array (ASIC-like output)

Interactive GUI

1 Load the default configuration, or change the filename for loading a custom configuration

2 Load the waveform of the single PHE current signal, then choose the Rq from the list box, finally press "Load w."

3 Load a timestamp file

4 Adjust the parameters

5 Press "Apply parameters" and then "Run Simulation"

DUNE - GRAIN Readout Chip Behavioral Simulation - INTERACTIVE MODE - (INFN-TO VLSI Group)

Courtesy of Sofia Blua and Valerio Pagliarino

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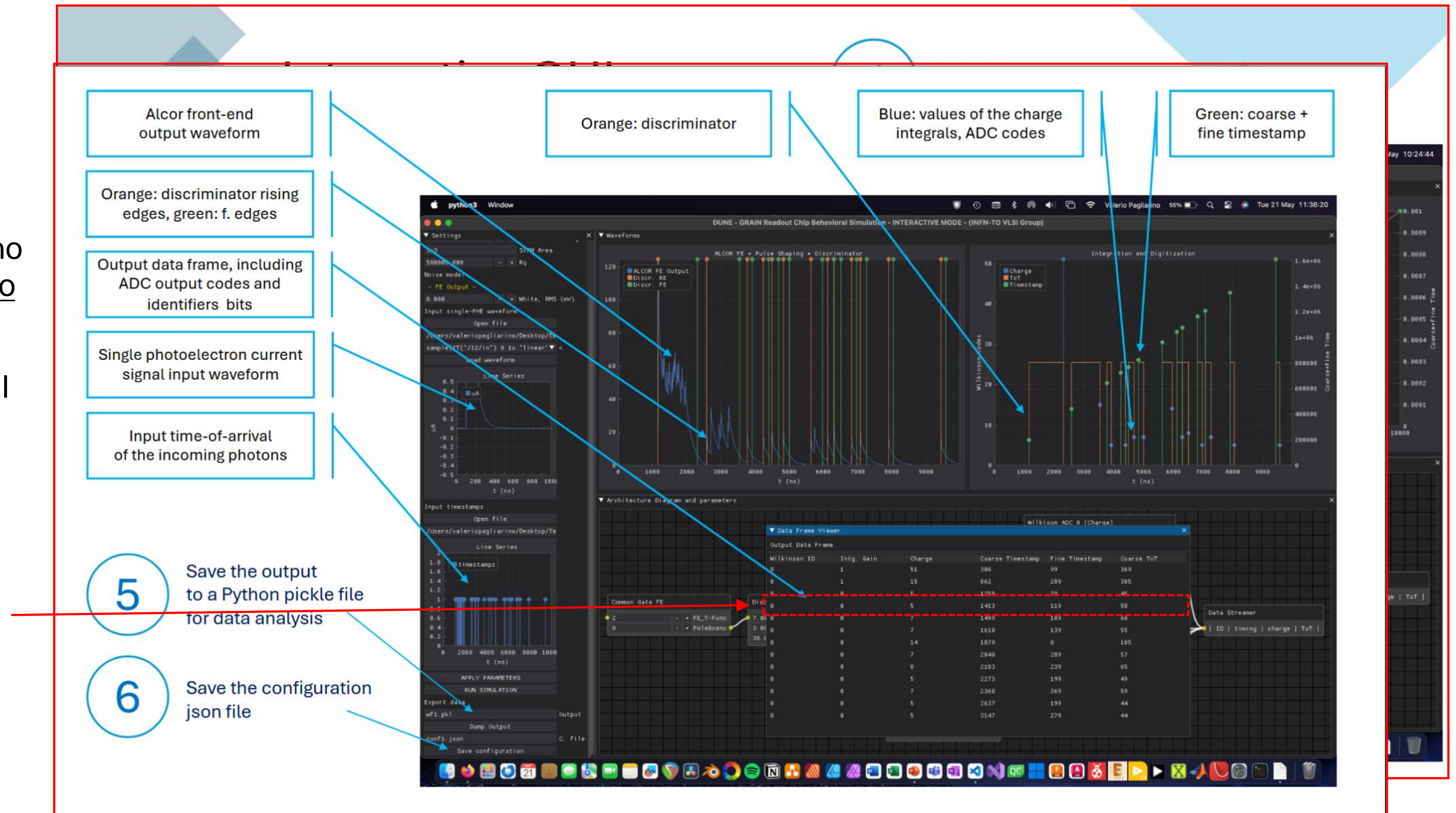


Courtesy of Sofia Blua and Valerio Pagliarino

Architecture Validation

Validation conducted by Bologna and Genova INFN

team:

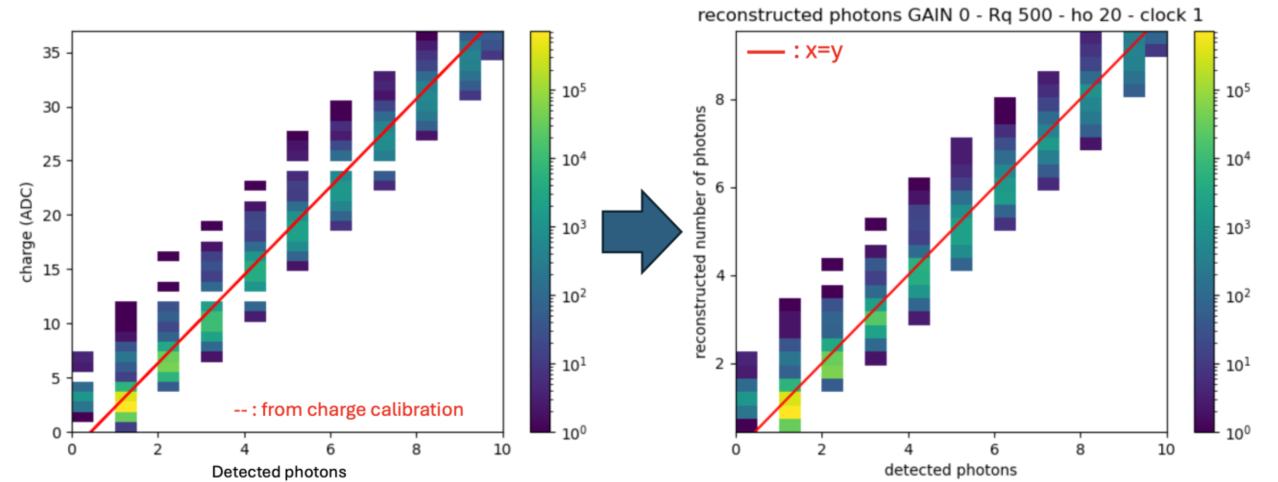
- Simulation of realistic, physics-driven events and attempts at reconstruction with the lenses and the coded mask approaches

Critical variables:

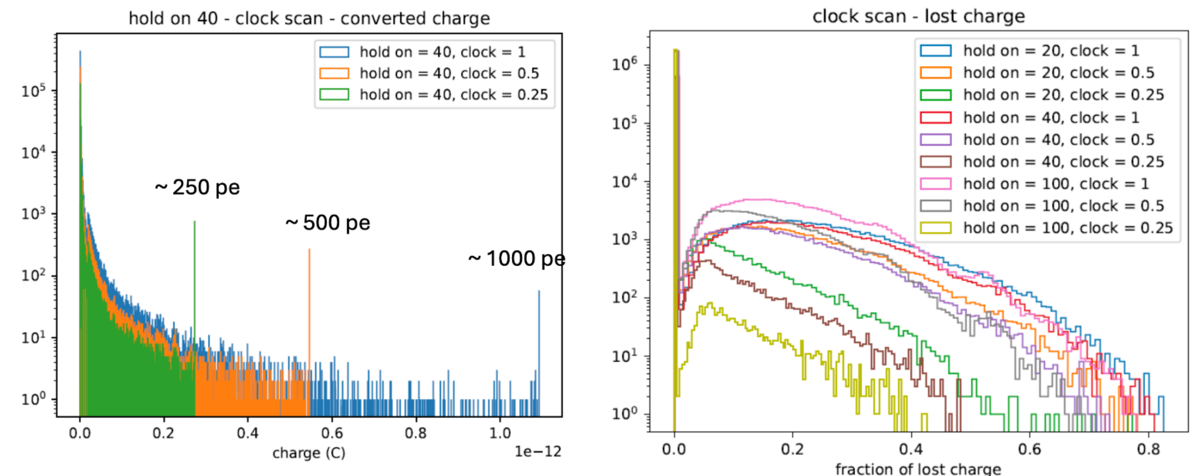
- ADC's conversion speed (4 x ALCOR Version)
- Hold-on (time extension of the integration window after the trailing edge of the discriminator)
- Integrator gains (2 gains at least are needed)

Results suggest that the proposed architecture meets reconstruction requirements with minimal event information loss.

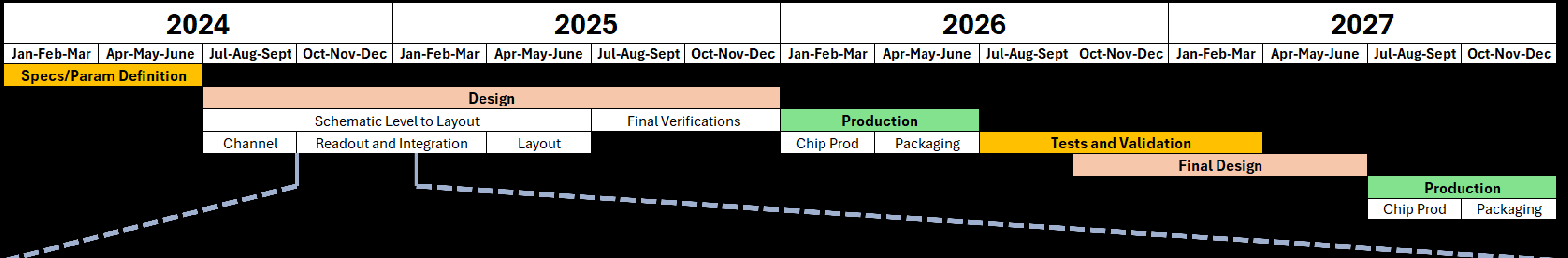
Calibration of the charge integrator

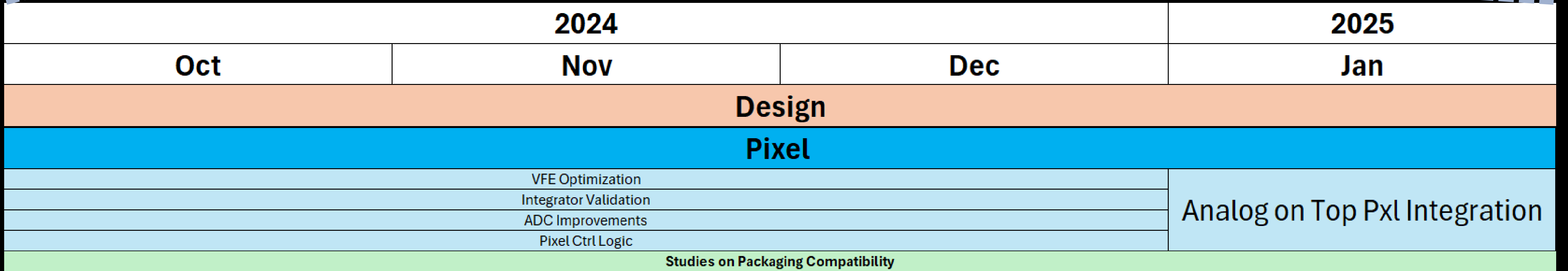


Dead time and fraction of lost charge



Timeline: Short-Term Goals





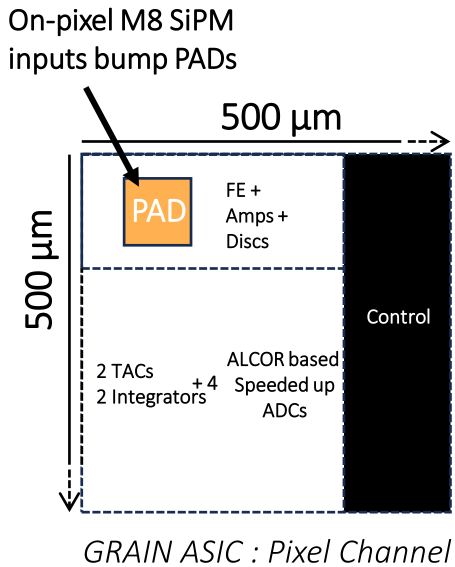
+ Cryogenic and room temperature ALCOR tests
… Then, a 2 x 2 matrix version by April/May (no submission), the 32 x 32 pixels version will follow

Flip-Chip BGA Package

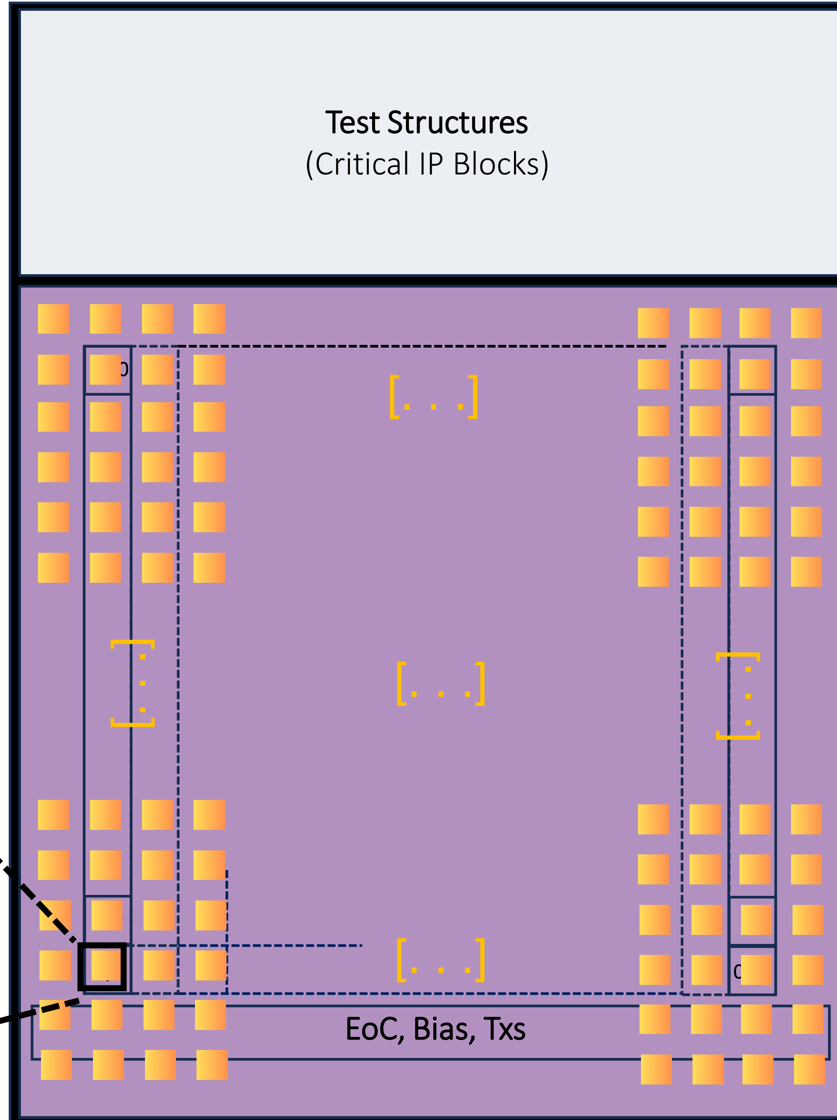
Example:

Grid of 40 x 40 PADs with 500 µ m pitch

- 1024 input PADs to the SiPM
- 576 PADs for 6 supply domains, output drivers, trigger, SPI, Reset, En, Low power



GRAIN ASIC : Pixel Channel

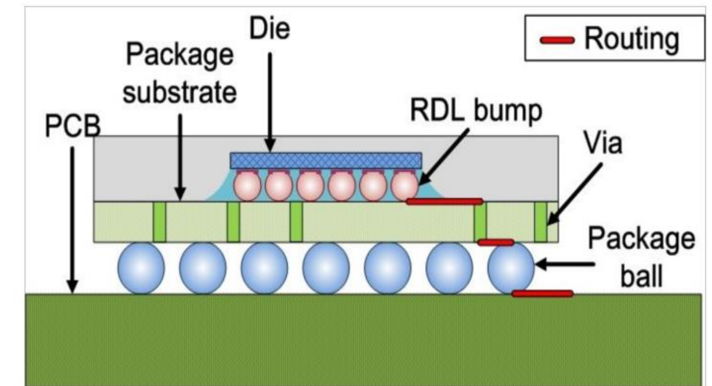


The ASIC is bump-bonded to an interposer connected to the board with package balls

- On-pixel PAD for SiPM
- Inter-column supply and ground PADs for reduced IR drops

Similar approach is followed for ALCOR v3 implementation for EIC

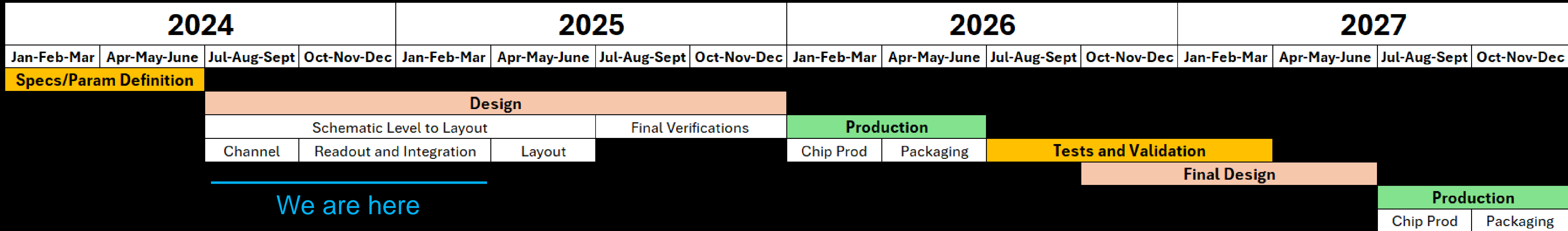
Ongoing investigation of possible companies



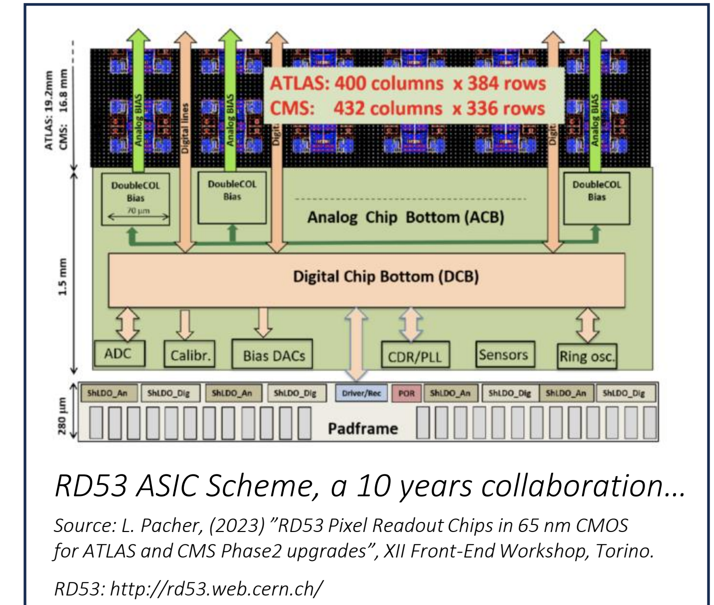
Flip-chip BGA working principle

Hsu, Hsin-Wu & Chen, Meng-Ling & Chen, Hung-Ming & Li, Hung-Chun & Chen, Shi-Hao. (2012). On effective flip-chip routing via pseudo single redistribution layer. 1597-1602. 10.1109/DATE.2012.6176727.

Timeline



- **The new ASIC for GRAIN:**
  - Leveraging expertise from previous and ongoing developments
  - Implementation of silicon-prooved IP blocks shorten the development time
- **2 Engineering runs:**
  - A 1024 demonstrator tape-out scheduled for the end of December 2025
  - Last submission with bug fixes in summer 2027
- **Ongoing and future activities:**
  - Pixel design targeting analog integration on top by the end of January
  - Test board and packaging are under study; production will commence once the PADframe is finalized (Dec 2025).



RD53 ASIC Scheme, a 10 years collaboration…

Source: L. Pacher, (2023) "RD53 Pixel Readout Chips in 65 nm CMOS for ATLAS and CMS Phase2 upgrades", XII Front-End Workshop, Torino.

RD53: http://rd53.web.cern.ch/

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BACK UP Slides

SiPM Signal Waveform

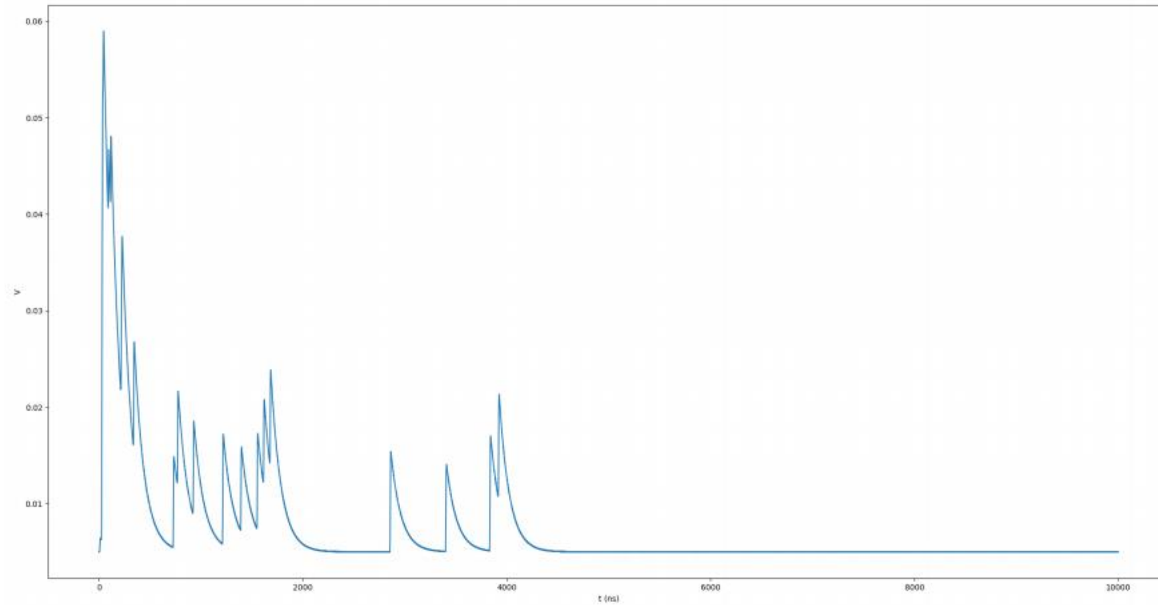
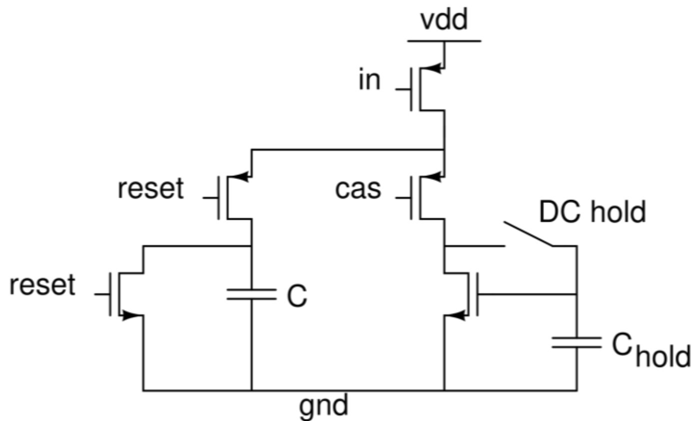


Figure 11: A typical SiPM waveform over the duration of the spill. All photons originate from one interaction.

Ongoing Activities: Pixel Design

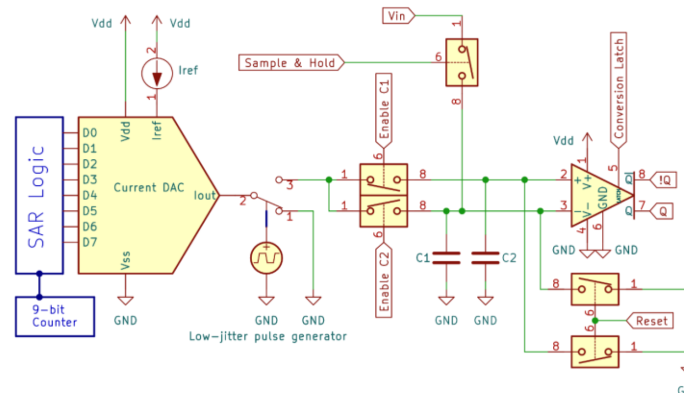
Integrator Design:

- Transistor level design in Virtuoso
  - Current mirror based
  - DC current compensation
  - Two gains
- Schematic level simulations



Current-steering ADC Design :

- ALCOR's ADC with improoved conversion speed
- Backward compatibile
- New SAR-based conversion algorithm
  - Faster conversion
  - Control logic and current injection improvements
- Block ready for integration expected by December



VFE Optimization :

- ALCOR Cryogenic tests and simulations showed:
  - Vth and R variations impact mostly the TIA and the DACs
- Optimization
  - TIA and DACs design optimization
  - Introcuction of configurable correction blocks
  - Noise optimization

Pixel

Pixel Design