ASIX
(Analog spectral Imager for X-rays)

Proposta di Esperimento

Area di ricerca: Detectors

Principal Investigator: Massimo Minuti (INFN Pisa)

Responsabile locale: Luigi Gaioni (INFN Pavia)

ASIX at a glance

🎯 Goal of the project: establish new X-ray detection systems with optimal imaging and spectral capabilities, combined with an event-driven readout logic to enhance system rate capability

- The position and energy resolutions are targeted to be better than 10 μm and 350 eV (@8 keV), respectively, with a maximum global readout rate of up to 10^8 hits/cm²/s
- INFN Units: Milano, Pisa, Pavia, Torino
- External Units: TIFPA, Unimi, Unipi, Unipv, Unibg, Polito
- Duration: 3 years

State of the art

- X-ray radiation is widely used in medical, industrial, scientific, artistic, and security applications
- Detection techniques typically leverage electronic devices that provide information about photon absorption point, energy, and arrival time
- Key point is the balancing of spatial and energy resolution, the latter being typically limited by charge-sharing issues in small-pixel detectors (<100µm)

	Medipix4/ Timepix4	Eiger	PIXIE-III	XPOL-III	This Proposal
Pixel pitch	55 µm	75 µm	60 µm	50 µm(hex)	50 µm(hex)
Pixel density [px/mm^2]	330	180	280	470	470
Pixel noise [rms]	65 e-	120 e-	50 e-	50 e-*	20-30 e-*
Minimum Threshold	450 e-	700 e- (@2.5 keV)*	1.5 keV	250 e-*	100-150 e-*
Energy Resolution (FWHM) Si-equivalent	1.5 keV (@2ke- Qin)*	1 keV (@8keV)*	2 keV (@20keV)*	450 eV*	250-350 eV*
Technology	65 nm		130 nm	180nm	65nm

Design goals

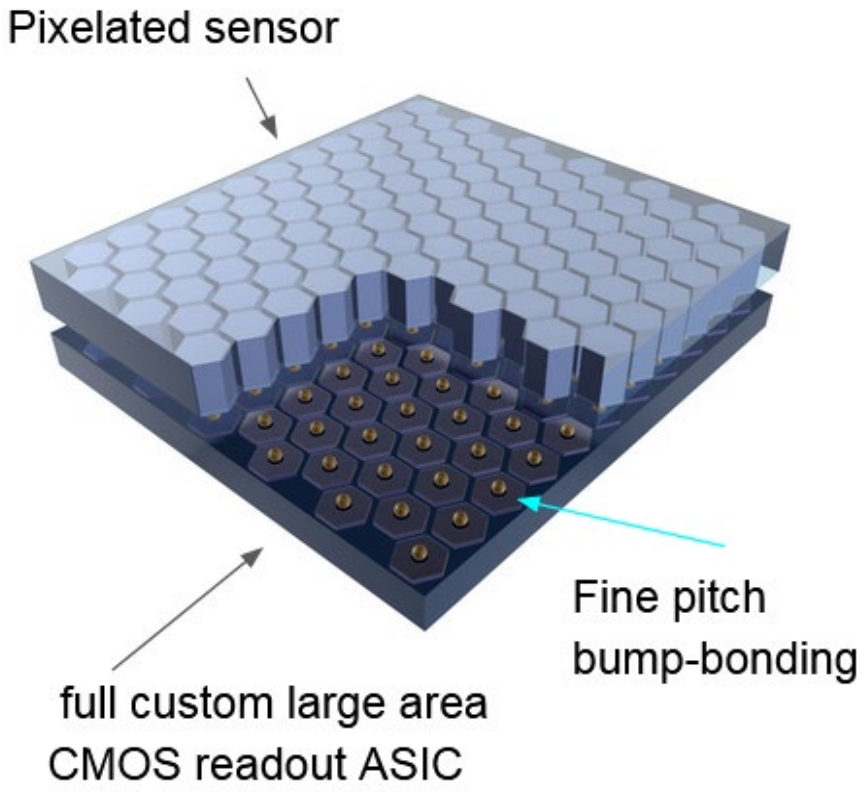
- The ultimate goal is to achieve energy resolutions at the Fe, Cu, Mo, and Ag K-lines comparable to the best-in-class X-ray detectors dedicated to spectroscopy. This will be matched with excellent imaging resolution provided by the ASIC granularity and high data throughput.
- As the final outcome, we propose to develop, in a 65 nm CMOS technology, a small-scale demonstrator (~5 x 5 mm²) of a pixel hybrid sensor

Characteristic	Design goals
Energy range	2–10 keV
Energy resolution	350 eV FWHM @ 8 keV
Pixel size	50 µm
Spatial resolution	10 µm
Front-end noise (ENC)	< 30 e^-
Dynamic Range	20000 e^-
Active area	≥ 5 x 5 mm^2
Trigger mode	Self-triggering
Readout mode	event driven, full readout
Maximum global readout rate	10^8 hits/cm^2/sec
Power Consumption	≤ 1 W/cm^2

The ASIX detector

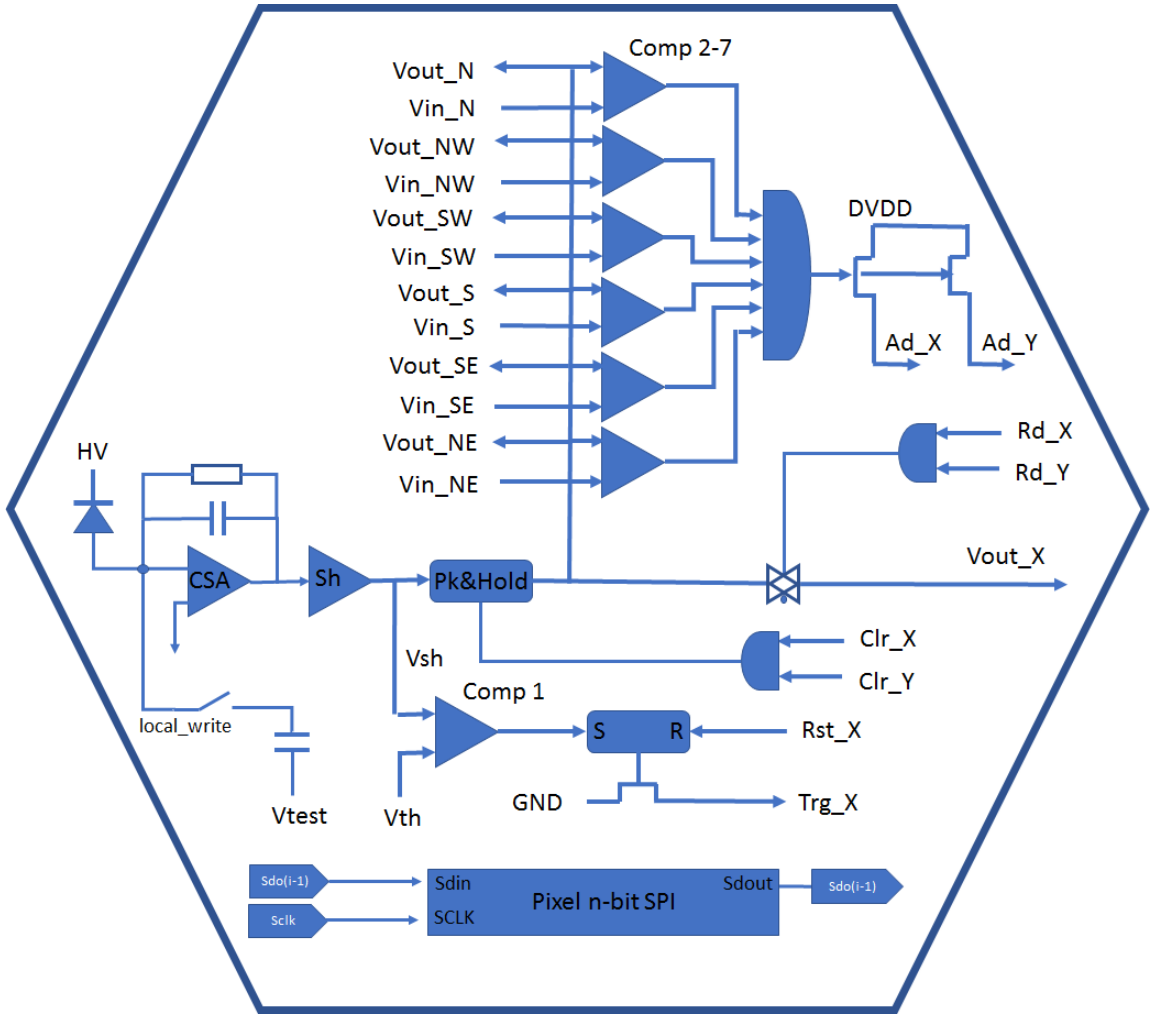
The ASIX detector units will implement a hybrid structure combining:

- a full-custom readout ASIC in 65 nm CMOS, equipped with low-noise front-end electronics, on chip A/D conversion, readout and configuration logic
- a customized edgeless Silicon sensor fabricated with advanced processing techniques aiming at minimizing the leakage current and the dead space at the device edges
- a simple and robust electro-mechanical integrated assembly on chip carrier boards aiming at providing a fully functional hybrid sensor module
- a compact and portable FPGA based DAQ system capable of supporting test and performance evaluation activities in the relevant test environment



ASIX Readout Chip

- A key point of the project is the development of pixel electronics with ultra-low noise, combined with fast readout and high-speed data output interfaces
- For the pixel electronics, we envision a full spectroscopy chain with an ultra-low-noise front-end (< 30 e rms), followed by a peak detector circuit, local discriminators, and readout and configuration logic
- On-chip A/D conversion will build upon a 10-bit SAR ADC capable of 5-10 MSPS, which was previously developed for earlier experiments. This ADC will serve as our baseline for customization in the ASIX context
- **Pavia group will be involved in the design of pixel electronics + ADC**



WP Structure

WP	Name	Responsible	Contributors
WP 1	Project management & dissemination	Massimo Minuti	MI, PI, PV, TO
WP 2	Readout ASIC design, verification and development		MI, PI, PV, TO
WP 3	Sensor design, verification and development	Maurizio Boscardin	TIFPA
WP 4	Detector Module Assembly, Test equipment and DAQ		PI
WP 5	Test and validation		MI, PI, PV, TO

Task timeline breakout

WP	Task	start	duration	end
1:Project management & dissemination	1: Coordination	0	36	36
2:Readout ASIC	2.1: proto-chip design	0	6	6
	2.2: proto-chip fabrication	6	3	9
	2.3: final-chip design	10	8	18
	2.4: final-chip fabrication	18	3	21
3:Sensor design, verification and development	3.1: sensor design and process review	12	2	14
	3.2: sensor fabrication	14	7	21
4:Detector Module Assembly, Test equipment and DAQ	4.1: hybrid assembly	21	8	29
	4.2: DAQ setup	7	3	10
5:Test And Validation	5.1: proto-chip test	9	3	12
	5.2: final-chip test	21	3	24
	5.3: ASIX sensor test	29	7	36

Two deliverables expected in WP2
D2.1 proto-chip ASIC
D2.2 final-chip readout ASIC

Budget

WP	Item	Sede	Capitolo	2025 (keu)*	2026 (keu)*	2027 (keu)*	Tot 3 anni(keu)*
1. "Project Office"	Missioni	PI	Miss	1,5	1,5	1,5	4,5
	Missioni	PV	Miss	1,5	1,5	1,5	4,5
	Missioni	MI	Miss	1,5	1,5	1,5	4,5
	Missioni	TIFPA	Miss	1,5	1,5	1,5	4,5
	MIssioni	TO	Miss	1,5	1,5	1,5	4,5
	Totale WP						18
2. "Readout ASIC design, verification and development"	prototipo 1 di piccola scala 2 X 2 mm^2 mi@asic	PV	Cons	18			18
	chip finale 5 X 5 mm^2 MPW	PV	Cons	90			90
	Totale WP						108

3. "Sensor design, verification and development"	Sensore finale		Cons		30		30
	Totale WP						30
4. "Sensor Module Assembly, test equipment and DAQ"	assemblaggio ASIC/sensore	PI	Cons		98		98
	PCB sensor carrier	PI	Cons	1,5	4		5,5
	Test station PC	PI	Inv	2			2
	DAQ Boards	PI	Cons	2,5			2,5
	Mechanics	PI	Cons		2	5	7
	Totale WP						115
5. "Test and validation"							
	Totale WP						0
Totale				121,5	141,5	12,5	275,5

Participant list for PV group

Name	Role	FTE
Luigi Gaioni	Local coordinator	0.4
Andrea Galliani	Participant	0.5
Massimo Manghisoni	Participant	0.3
Lodovico Ratti	Participant	0.1
Gianluca Traversi	WP2 leader	0.3

TOT FTE 1.6

INFN Pavia services requests

NONE