Istituto Nazionale di Fisica Nucleare

ASPIDES

A CMOS SPAD and Digital SiPM Platform for High Energy Physics (proposta di esperimento)

Responsabile nazionale: Lodovico Ratti (sez. di Pavia)

INFN Pavia, Consiglio di Sezione, 3 luglio 2024, Pavia

ASPIDES project

Goal:

develop SiPMs in CMOS technology (digital SiPMs or dSiPMs) for fast (high time density), high dynamic range counting and high accuracy timing – application to dual readout calorimetry, RICH, dark matter and neutrino experiments

Participating units:

Bari (N. Mazziotta), Bologna (L. Rignanese), Milano (R. Santoro), Pavia (L. Ratti), Trento (L. Pancheri), Napoli (G. Fiorillo), Padova (G. Collazuol), Torino (M. Da Rocha Rolo)

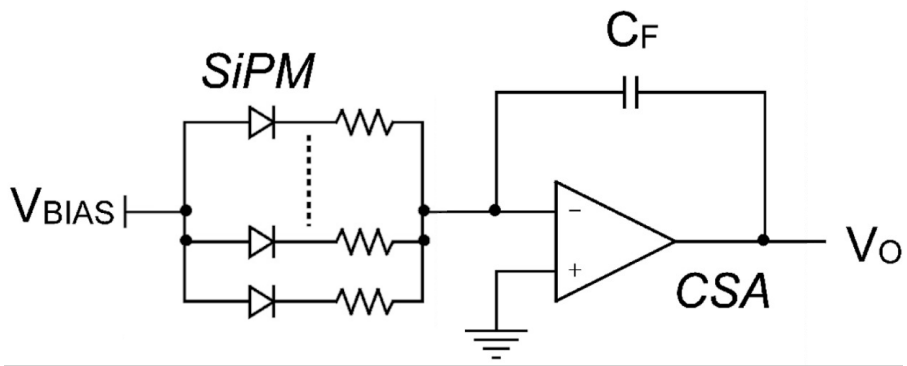
Research area:

Detectors and electronics

Duration: 3 years

SiPMs: analog vs digital

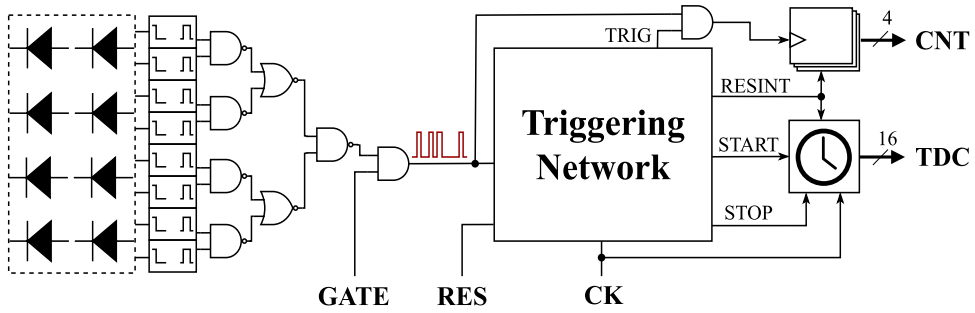
- Analog SiPMs: signal proportional to number of fired cells – real time detection



✓ Inherently fast circuits, allowing the detection of photons with **high temporal density**

x High power consumption, need for a converter to digital domain

- Digital (CMOS) SiPMs: NAND/NOR compression trees, binary counters, serialized pulses from fired cells



M. Perenzoni et al. 2017 – IEEE JSSC

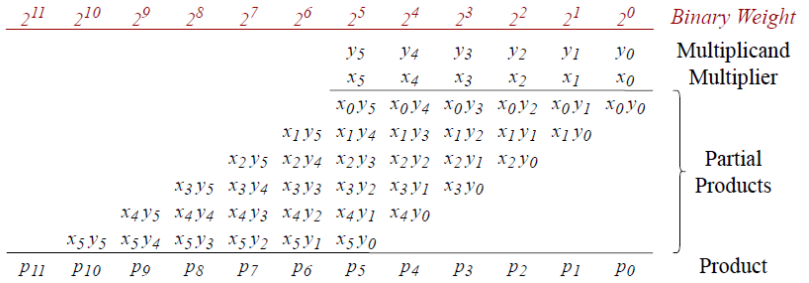
✓ No static power consumption, standardized design, standard cells, no A/D converters, open to new features

x Problems with detection of photons with **high temporal density**

Parallel counters

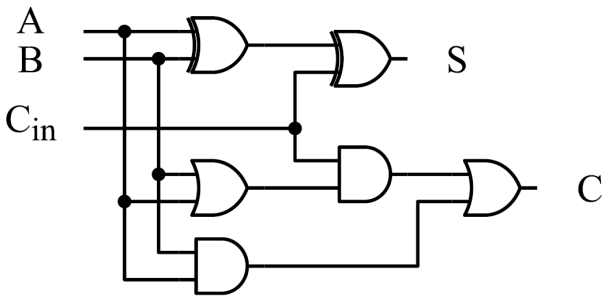
*"A **Parallel Counter** is a combinational network which provides q outputs, processing the signals coming from its **$p \leq 2^q - 1$** inputs. The binary number represented by the q outputs is the number of bit at 1 fed as inputs"*

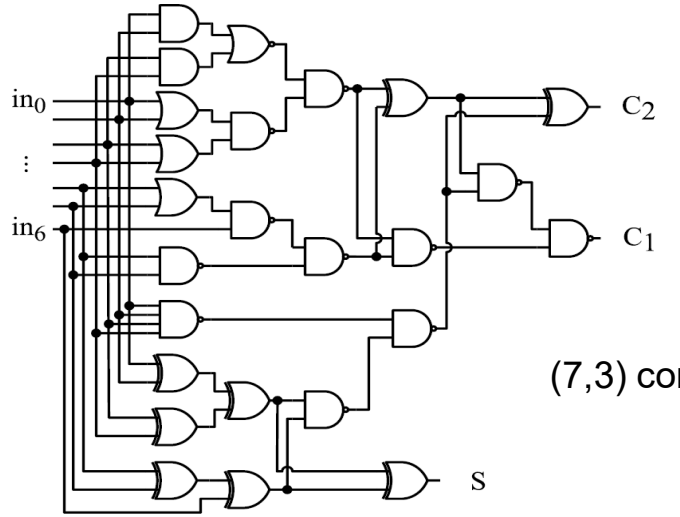
L. Dadda, "On Parallel Digital Multipliers", Alta Frequenza, 1976



(n,m) compressors are devices capable of collapsing n input lines into m output lines interpreted as the binary representation of the number of ones at the input ($m \geq \lceil \log_2 n \rceil$)

(3,2) compressor





(7,3) compressor

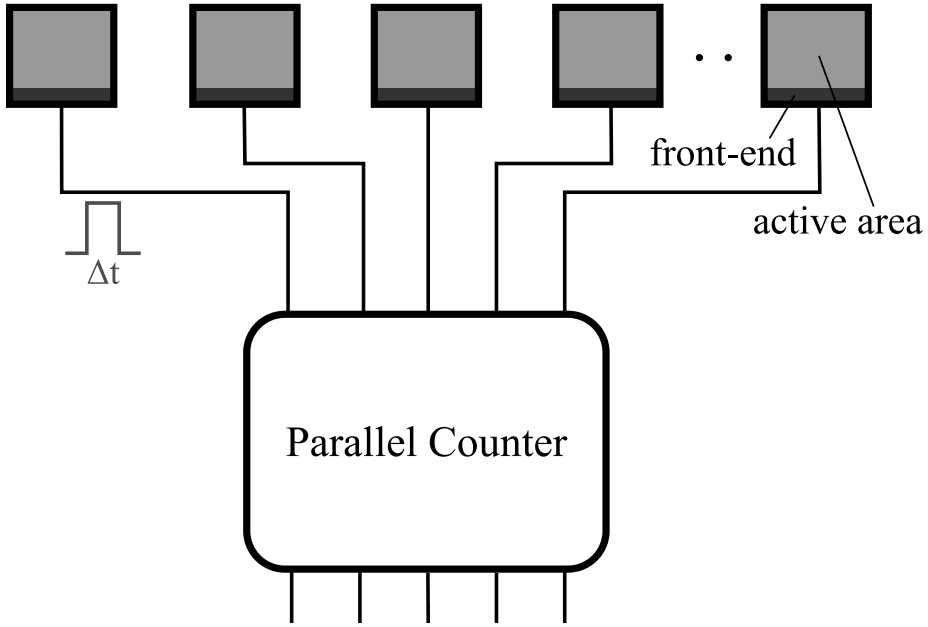
Mehta et al. 1991

Parallel counter based dSiPM (flash-dSiPM)

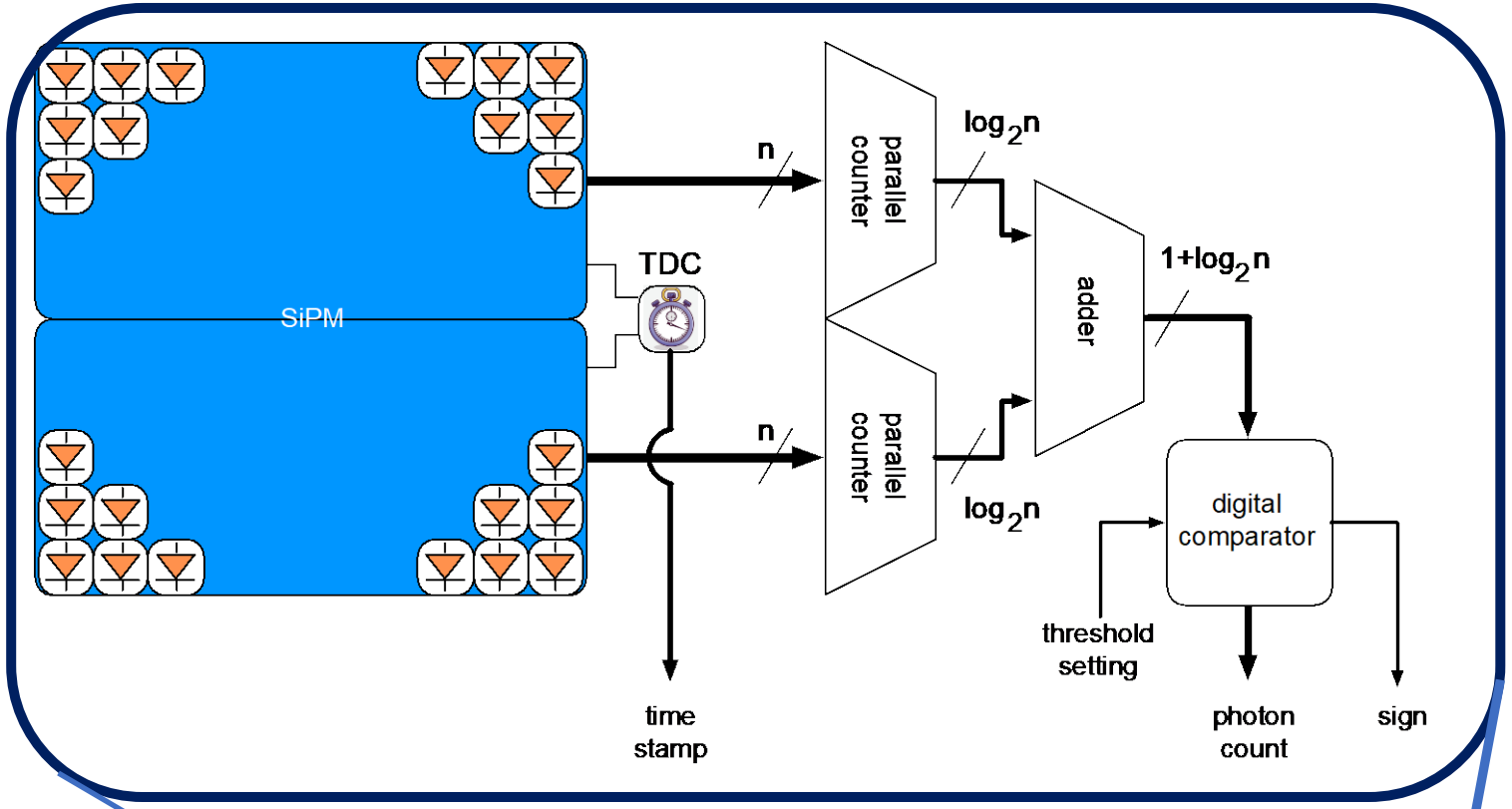
SiPMs based on high-speed combinational networks, low latency, real time photon counting from simultaneously fired SPADs

The integration of parallel counters in dSiPM structures brings several **challenges**:

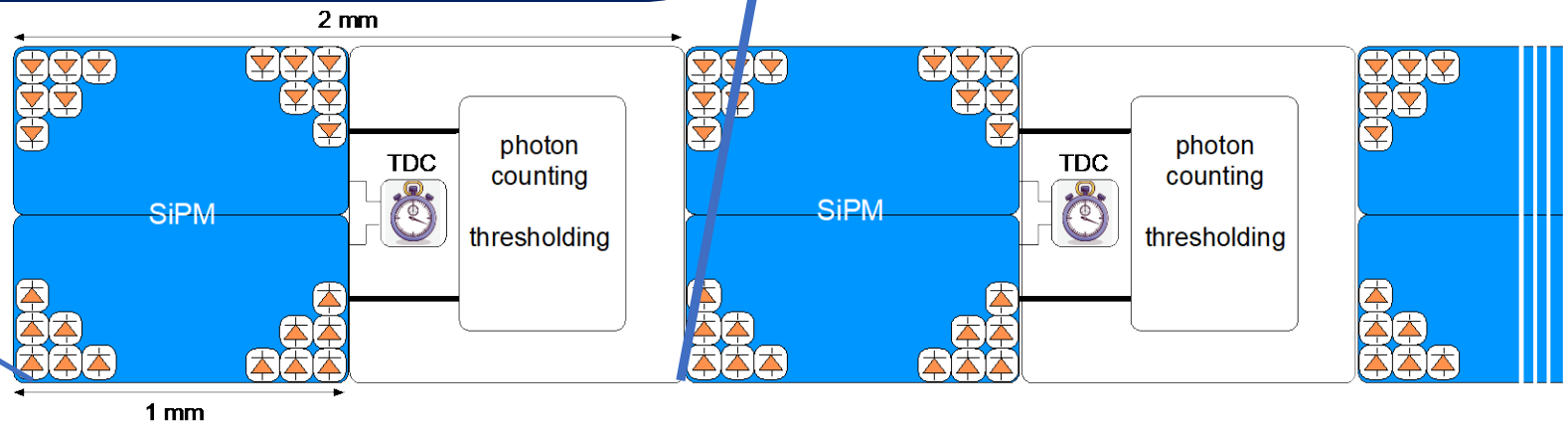
- large number of parallel **connections** from SPAD cells
- **poor modularity**
- **balanced** signal paths
  - reduction of **glitches** (spurious pulses)
  - **power** consumption optimization
- **area** optimization
- **delay** optimization



Parallel counter based dSiPM (flash-dSiPM)



Demonstrator for dual readout calorimetry applications



Fully digital approach – Pros and Cons

Pros

- Measurement result immediately available in digital form
- No need for additional readout chips to be coupled to the sensor
- Easier linearization and calibration – direct digital output vs digital/analog (including noise + non uniformity)/digital conversion
- Integrated TDC – local timing signal generation and measurement
- Smaller costs for large areas

Cons

- Readout architecture has poor modularity
- Fill factor may suffer from small pitch and readout circuit complexity

Specifications

Requirements	**Dual readout calorimetry**	**Cherenkov (eg RICH, IACT)**	**DM**	**neutrino**
SiPM Unit area (mm^2)	1x1	mm scale	10x10	6x6
Micro-cell pitch (um)	10-15	40-50	25-30	50-150
Macro-pixel area (um^2)	500x500			
PDE (%)	>20	> 40	>45	>35
DCR (kHz)	<100 kHz/mm^2	very low for single pe detection	<0.1 Hz/mm^2 (at LN)	<0.2 Hz/mm^2 (at LN)
AP (%)	<1	few		<5%
Xtalk (%)	few	few	Total Correlated Noise Probability (Xtalk + AP) < 60 %	<35%
Trigger	external, self	self, external	self	
Output data: light intensity	no. of fired cells in 1 or 2 time windows (10's of ns long)			
Output data: time	time of arrival of the first photon in the window, possibly of the last photon (TOT)	ToA and ToT	ToA and TOT	
Time resolution (ps)	<100	< 100 single pe		
Module size and form factor	strip with 8 units (1mm x 16 mm), pitch of 2 mm			
Connection	BGA			

Activity program

2025

- Characterization of the ASAP110LF test chip developed in a 110 nm CMOS technology, including different SPAD arrays with different features (passive and active quenching, different active area, structures for investigating timing properties and ionizing radiation tolerance) and mini-SiPMs
  - DCR, breakdown voltage, afterpulsing, electrical and optical cross-talk, also as a function of the temperature
  - QE and PDP/PDE
  - Time resolution

- Investigation of the cumulative damage from ionizing radiation (X-ray) and from atomic dislocation in the substrate (neutrons, protons)

- Study of SPAD operation in cryogenic conditions

Activity program

2025-26

- Development of small scale prototypes of CMOS SiPMs consisting of about 1000 SPADs with 15-20 um pitch
- for the readout, both a fully digital and a mixed analog and digital approach will be explored – best compromise between detection efficiency (fill factor) and functional density
- on sensor electronics to be provided with event detection, counting, thresholding and time stamping capabilities, possibly together with the ability to follow the time evolution of the light pulses – reconstruction of the longitudinal shower and discrimination between Cherenkov and scintillation signals
- specific structures included to test the chip functionalities

- submission 3Q 2025, characterization 1Q 2026

2026-27

- Development of a demonstrator chip including 8 SiPMs, each with a 1 mm^2 area and a 2 mm pitch (64x64 cells, 15 um pitch) – dual readout calorimetry
- inter-SiPM region used for integrating most of the electronics, to minimize the impact on the fill-factor
- smaller versions of dSiPMs for application to RICH, DM and neutrino experiments (larger SiPMs)
- characterization to be performed in the lab and in a beam test

- submission 4Q 2026, characterization 2Q-4Q 2027

Personnel involved in the experiment

PAVIA

Roberto Ferrari: 5%

Lodovico Ratti: 40%

Fatemeh Shojaei: 100%

Carla Vacchi: 20%

Sezione	FTE
Bari	>1
Bologna	0.3
Milano	1.0
Napoli	1.3
Padova	0.4
Pavia	1.65
Torino	0.35
Trento	1.2
TOTALE	>7.2

Financial request (PV, 2025)

		k€
Missioni	missioni a Bologna per meeting su interfacciamento con DAQ; missioni a Torino per meeting su circuiti di front-end per SiPM digitale	2
Consumi	Run MPW con LFoundry, 12 mm^2 (2.52 kEuro/mm^2)	41
	Produzione di schede di test per collaudo di circuiti integrati	5
	packaging di 10 chip	3
Totale		51

Financial request (PV, 2026-2027)

		k€
Missioni	missioni a Bologna per meeting su interfacciamento con DAQ; missioni a Torino per meeting su circuiti di front-end per SiPM digitale	3
	Partecipazione a test beam (2 persone per 1 settimana)	3
Consumi	Run MPW con LFoundry, 25 mm^2 (2.52 kEuro/mm^2)	77
	Produzione di schede di test per collaudo di circuiti integrati	8
	packaging di 10 chip	3
Totale		94

Non sono richiesti servizi di sezione

Financial request (overall)

	2025	2026-2027
Missioni	~15 kEuro	~40 kEuro
Consumi	~75 kEuro	~140 kEuro
Totale	~90 kEuro	~180 kEuro