White Rabbit

Status and plans of the technology and the community around it

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European Laboratory for Particle Physics
(CERN)

LLRF Topical Workshop on Synchronization, Measurements and Calibration

INFN-LNF, Frascati, Italy
28 October 2024

Outline

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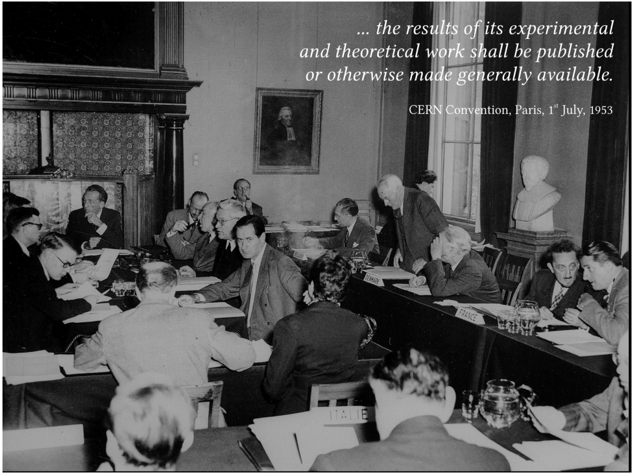
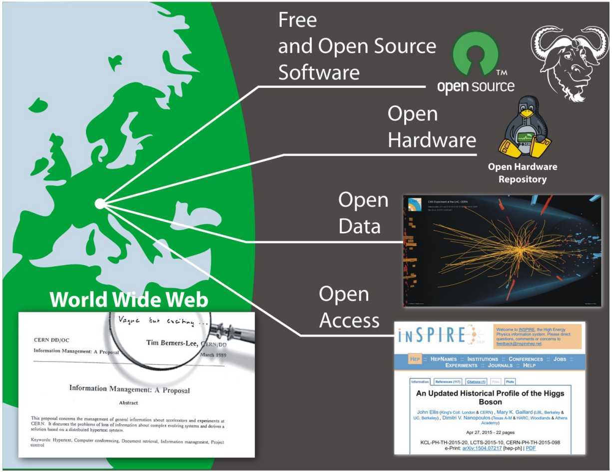
Dissemination



How to interpret one's dissemination mandate in the 21st century

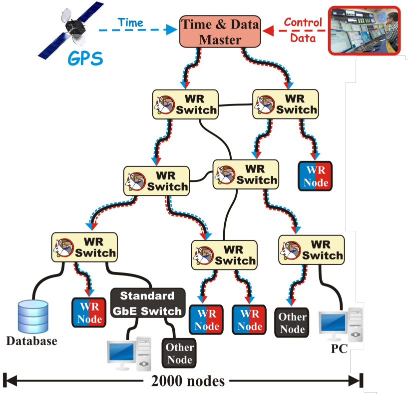


Outline

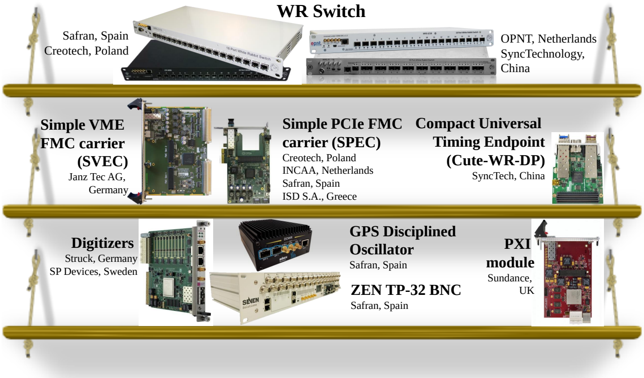
1. CERN's knowledge dissemination mandate
2. White Rabbit
3. White Rabbit and RF
4. Community
5. The White Rabbit Collaboration
6. Plans

What is White Rabbit?

- Initially meant for Big Physics facilities/projects: CERN, GSI, Nikhef. . .
- **Based on well-established standards**
  - Ethernet (IEEE 802.3)
  - Bridged Local Area Network (IEEE 802.1Q)
  - Precision Time Protocol (IEEE 1588)
- **Extends standards** to meet new requirements and provides
  - Sub-ns synchronisation
  - Deterministic data transfer
- Initial specs: links $\leq$10 km & $\leq$2000 nodes
- **Open source and commercially available**



Open **and** commercially available off-the-shelf



Companies selling White Rabbit:

`www.ohwr.org/projects/white-rabbit/wiki/wrcompanies`

White Rabbit technology - sub-ns synchronisation

Based on

- IEEE 1588 Precision Time Protocol on Gigabit Ethernet over fibre

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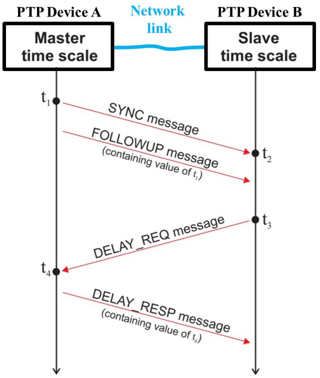
Enhanced with

- Layer 1 syntonisation
- Digital Dual Mixer Time Difference (DDMTD)
- Link delay model

Precision Time Protocol (IEEE 1588)



- Frame-based synchronisation protocol
- Simple calculations:
  - link delay: $\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$
  - offset from master: $OFM = t_2 - (t_1 + \delta_{ms})$

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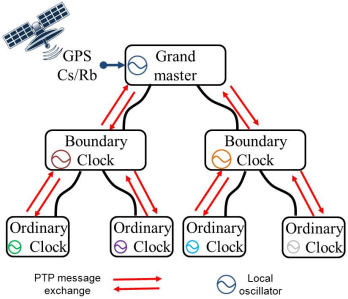

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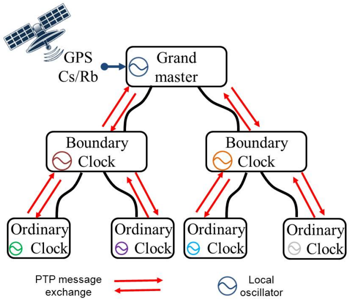

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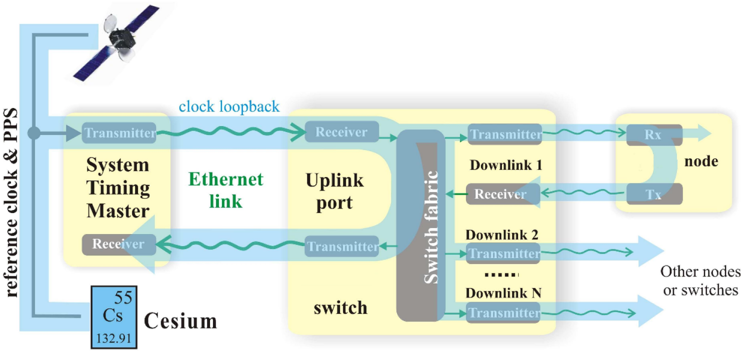
- Hierarchical network
- Shortcomings of traditional PTP:
  - devices have free-running oscillators
  - frequency drift compensation traffic can compromise determinism of other messages
  - assumes symmetry of medium
  - resolution of timestamps

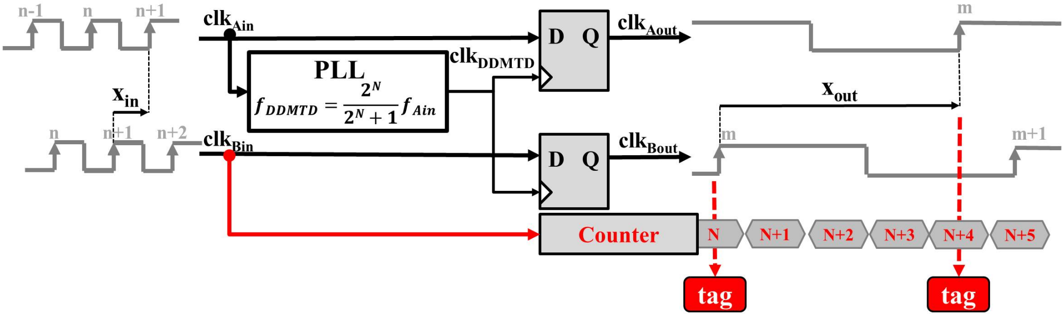
Layer 1 Syntonisation

- Clock is encoded in the Ethernet carrier and recovered by the receiver chip
- All network devices use the same physical layer clock
- Clock loopback allows phase detection to enhance precision of timestamps



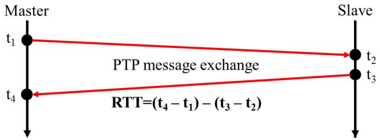
Digital Dual Mixer Time Difference (DDMTD)

- Precise phase measurements in FPGA
- WR parameters:
  - clk_{in} = 62.5 MHz
  - clk_{DDMTD} = 62.496185 MHz (N=14)
  - clk_{out} = 3.814 kHz
- Theoretical resolution of 0.977 ps



Link delay model

- Correction of Round Trip Time (RTT) for asymmetries



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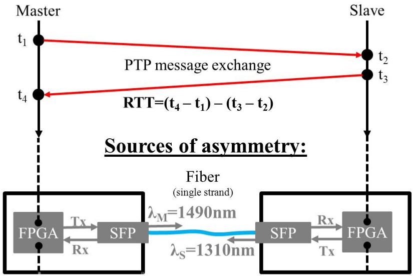

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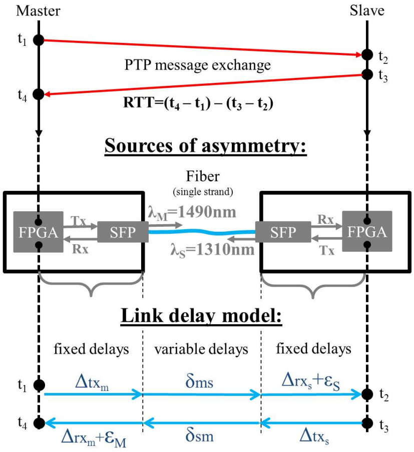
$$\alpha = \frac{\nu_g(\lambda_s)}{\nu_g(\lambda_m)} - 1 = \frac{\delta_{ms} - \delta_{sm}}{\delta_{sm}}$$



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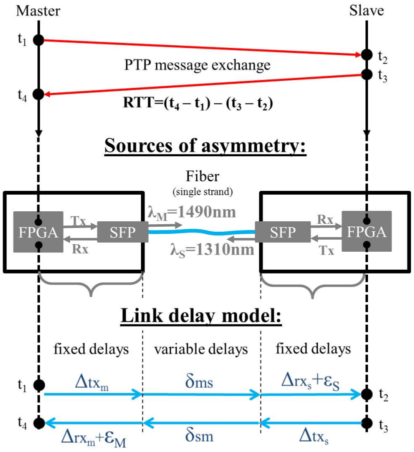
- Accurate offset from master (OFM):

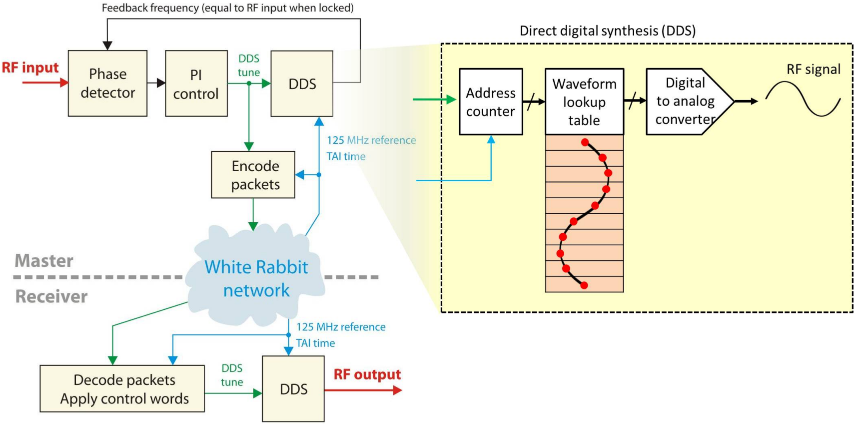
$$\delta_{ms} = \frac{1+\alpha}{2+\alpha}\left(RTT - \sum \Delta - \sum \epsilon\right)$$

$$OFM = t_2 - (t_1 + \delta_{ms} + \Delta_{txm} + \Delta_{rxs} + \epsilon_S)$$

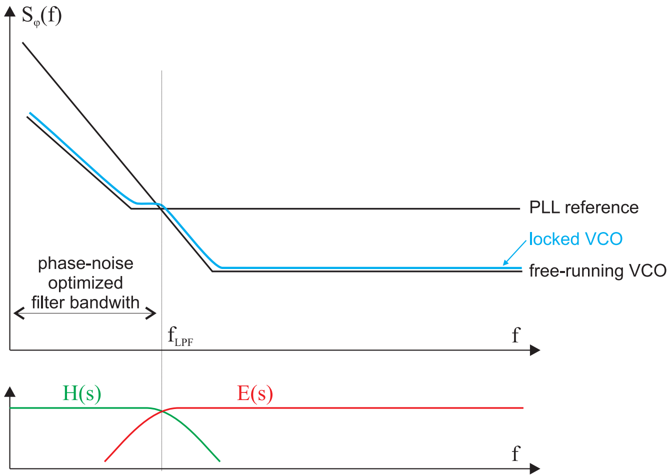


Outline

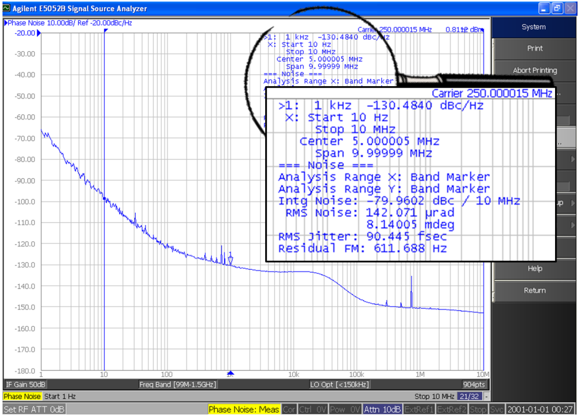
WR-derived reference clock signal for RF synthesis and sampling



Minimising jitter by using a good OCXO

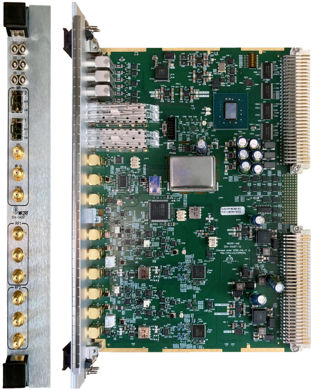


The eRTM14/15 MTCA.4 module for SPS LLRF



See https://ohwr.org/project/ertm15-llrf-wr/wikis for details

RF over Ethernet (RFoE) using WR: the WR2RF board



See also https://roe-mapping.web.cern.ch/

Fundamental limits

- WR is about getting the best possible time and frequency using off-the-shelf components and following standards.

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- “The [DDMTD] phase detector introduces a limitation in short-term stability equal to MDEV 4E-13 at τ = 1 s (ENBW 50 Hz), with a flicker PM behavior from τ = 1 s to τ = 100 s and more. The origin of flicker PM is due to the LVDS input clock buffer of the currently used FPGA and its related internal clock distribution. Similar results are observed for newer FPGAs, where a (slightly reduced) flicker PM is still present.”

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- See https://ohwr.org/project/wr-low-jitter/wikis for more details, in particular *M. Rizzi et al. "White Rabbit Clock Synchronization: Ultimate Limits on Close-In Phase Noise and Short-Term Stability Due to FPGA Implementation"*

Outline

Short history of WR

- 2008: first meeting at CERN
- 2009: first switch prototype
- 2012: first COTS switch available (open-source hardware, gateware, firmware, software)
- 2012: first operational deployment of WR (Gran Sasso National Lab)
- 2013-2018: WR concepts standardised within IEEE 1588
- 2024: creation of the WR Collaboration (see launch event)

WR post-standardisation

A technology supported by a friendly community working on a fully open-source implementation of IEEE 1588-2019 High-Accuracy (HA) profile, with a guaranteed sub-nanosecond accuracy

Outline

Entering a new phase

Post-standardisation issues

- How to maintain good support after the increase in uptake of the technology, both in industry and academia?
- How to ensure a high level of quality in the foundations of WR (switch and WR PTP core)?

The White Rabbit Collaboration in a nutshell

Ensuring sustainability

- Members pay a yearly fee and shape the future of the technology
- Fees are used to pay the WR Collaboration Bureau, which offers support (including training) and ensures WRS and WRPC are always in good health

The White Rabbit Collaboration in a nutshell

Letting information flow

- Collaboration with vendors ensures coherent growth of the WR ecosystem
- Keeping members well informed: online presentations, forum, regular meetings...
- Connecting people, institutes, companies (e.g. connecting NRENs with industry)

The White Rabbit Collaboration in a nutshell

Ensuring high-quality

- Making the evolution of WRS and WRPC the main task of the Bureau
- Teaming up with laboratories to establish a set of tests and qualification criteria
- Connecting the use of the WRC logo to the successful passing of those tests

The White Rabbit Collaboration in a nutshell

Projects! Some examples:

- Ongoing: collaboration with GMV and IQD on hold-over.
- Quantum: see e.g. CERN's Quantum Tech Initiative at https://quantum.cern
- Under discussion: robust, long-distance WR for smart grids

An experiment in public-private partnerships

Getting the best of both worlds

- Dissemination according to our Open Science mandate
- Impact and sustainability

Economics

- Companies can add value of top of WR and monetise products based on those developments
- They decide what they contribute as open source and what they keep proprietary

WRC members in 2024

SAFRAN
gmv INNOVATING SOLUTIONS
IQD
Sync Tech
Quincy Data
DEUTSCHE BÖRSE GROUP
LMS LIQUID-MARKETS SOLUTIONS The Power of the Possible™
jumptrading
University of New Hampshire InterOperability Laboratory
nu QUANTUM
SURF
GSI
MYRRHA
Nikhef
CERN
UNIVERSITÉ DE FRANCHE-COMTÉ

White Rabbit Collaboration

White Rabbit
COLLABORATION

Join us! For more details, see
https://www.white-rabbit.tech

Outline

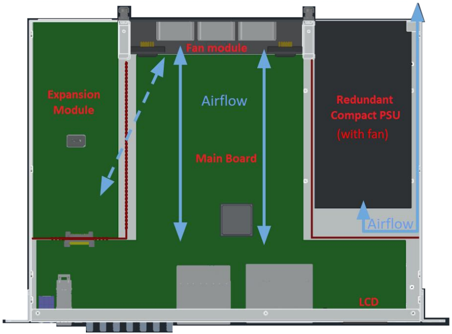
Plans

WR Switch v4

- GbE and 10GbE support
- Redundant and serviceable fans and power supplies
- Based on Xilinx/AMD Zynq UltraScale+ System-on-Chip (SoC)
- Expansion board slot for enhancements (low phase noise, hold-over. . .)

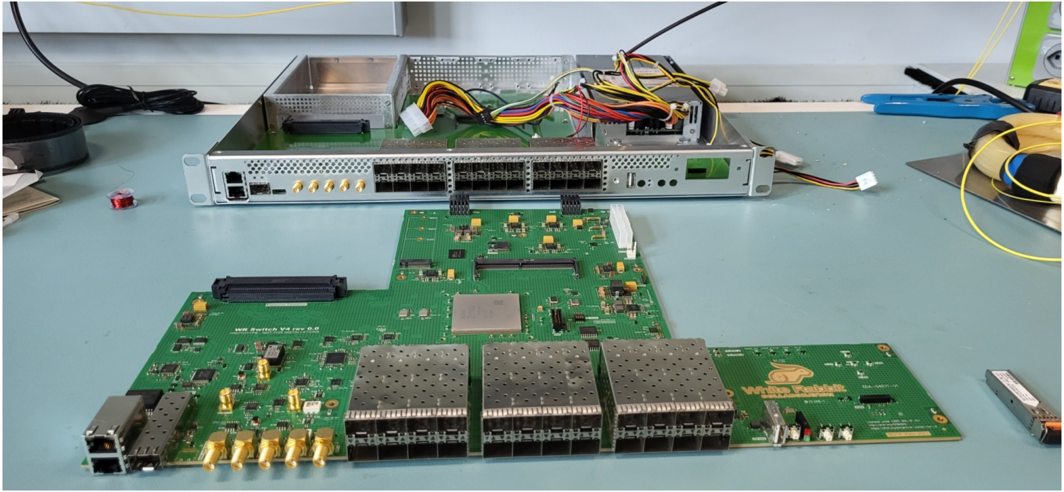
See https://ohwr.org/project/wr-switch-hw-v4/wikis for more details.

WR Switch v4

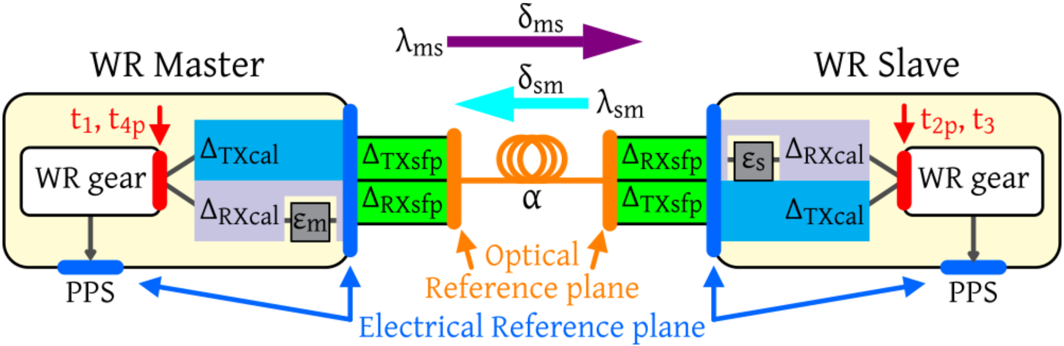


Prototyping stage, v3 functionality before the end of the year.

WR Switch v4



Standardisation++



Courtesy Henk Peek and Peter Jansweijer

Standardisation++ (P. Jansweijer, M. Lipiński)

Amendments to IEEE 1588-2019

- Absolute calibration
- In-situ calibration of asymmetry

Within the SNIA SFF working group

Storage of calibration parameters in SFP EEPROM

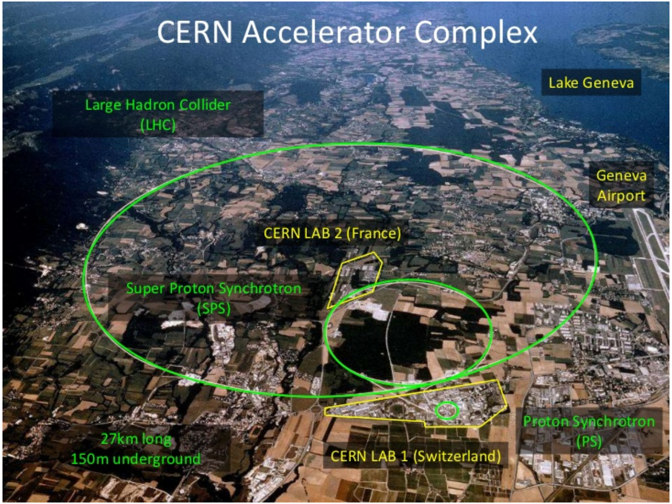
Possibilities for collaboration: non-exhaustive list

- Improving WR performance
  - In-depth studies of transceiver behaviour inside SoCs
  - Sensitivity to external factors such as temperature variations
- Improving WR usability
  - Monitoring and logging of important parameters and events with time stamps
  - Automation of calibration of port delays and fibre asymmetry
- Quantum: both QKD and entangled qubits
- Robustness: hardware and system-wide (clock ensemble). Redundancy and seamless switch-over ($<$1ns jump)
- Other?

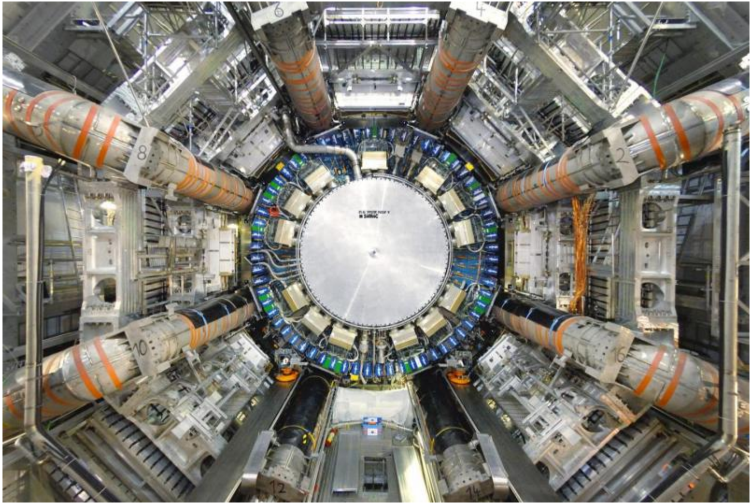
Backup slides

Backup slides

Accelerators



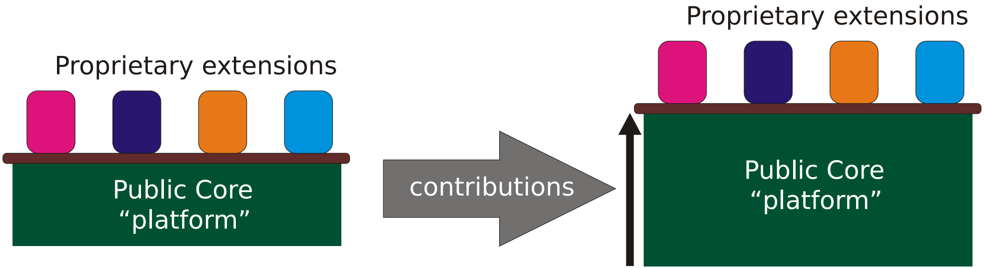
Detectors



WR and open source

	Commercial	Non-commercial
Open	**Winning combination. Best of both worlds.**	Whole support burden falls on developers. Not scalable.
Proprietary	Vendor lock-in.	Dedicated non-reusable projects.

Public-private partnerships



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