PIP-II

Fermilab

U.S. DEPARTMENT OF ENERGY | Office of Science

Timing and Synchronization in the LLRF systems of the Fermilab PIP-II Linac

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LLRF Timing Workshop

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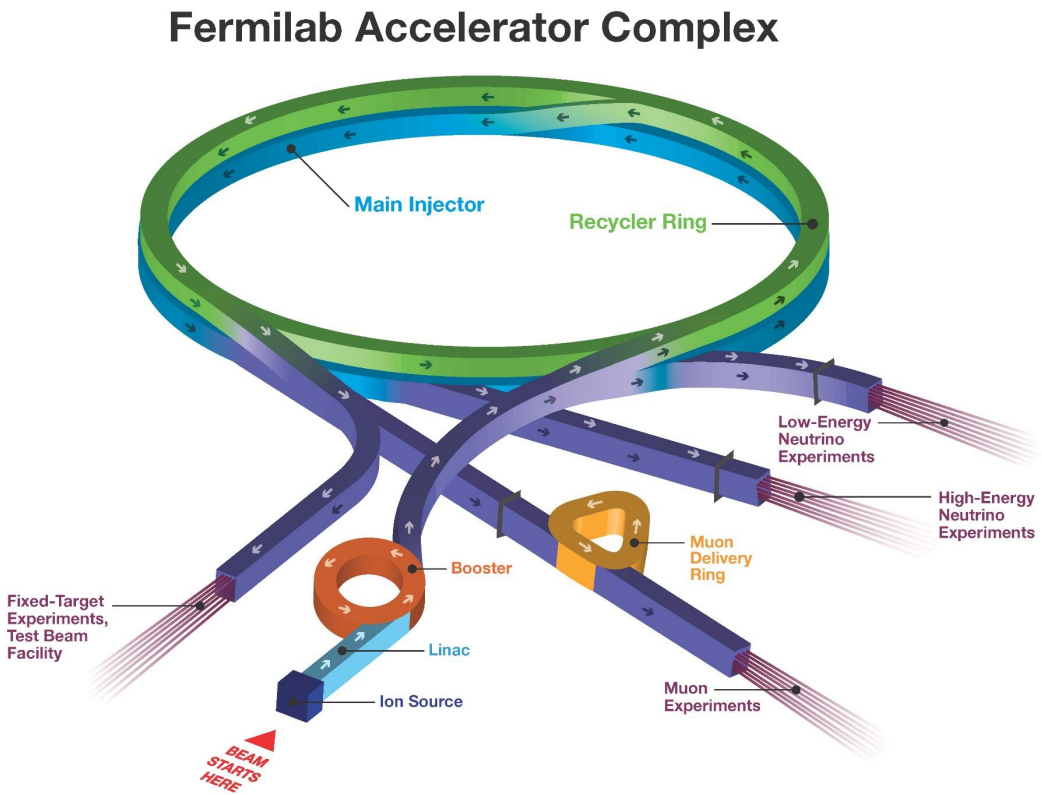
PIP-II is a partnership of:

- US-DOE
- India-DAE
- Italy-INFN
- UK-STFC-UKRI
- France-CEA, CNRS/IN2P3
- Poland-WUST, WUT, TUL

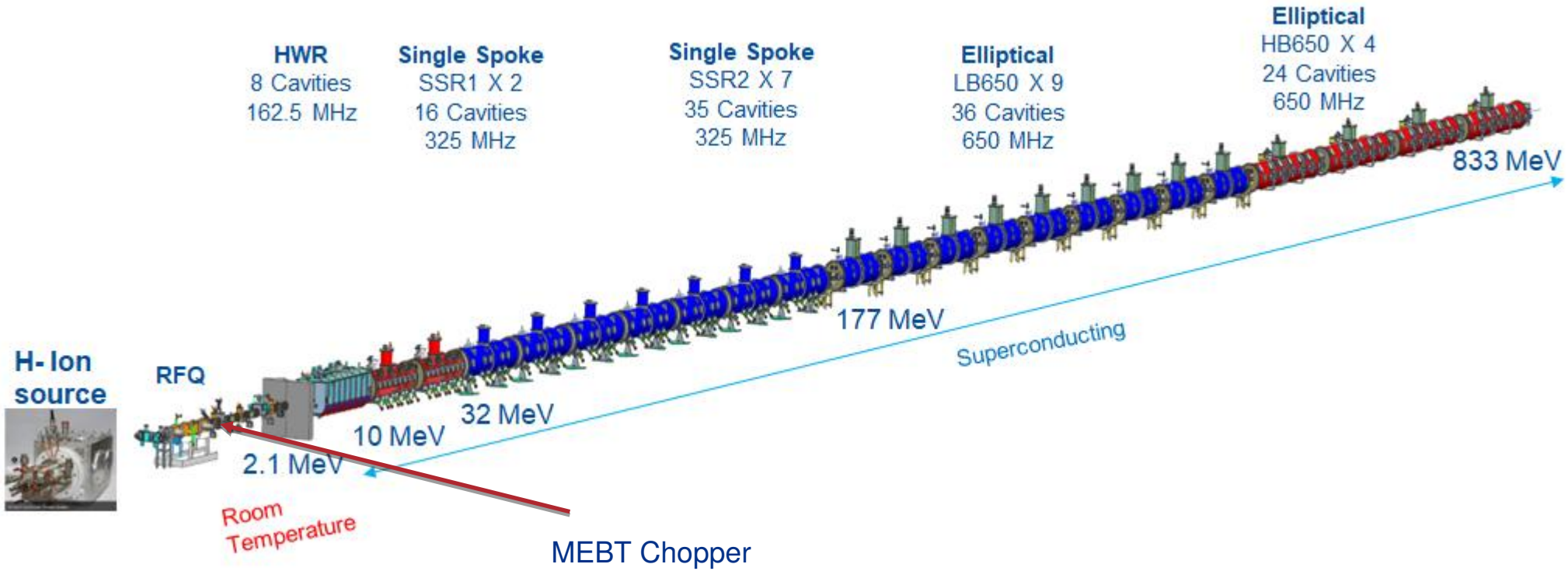
Outline

- PIP-II Linac and Fermilab Accelerator Complex
- LLRF Phase Reference Line
- Timing System for PIP-II Era
- Linac to Booster Transfer
- Beam chopper for non-harmonic transfers
- Synchronization for Beam Loading Compensation

Fermilab Accelerator Complex

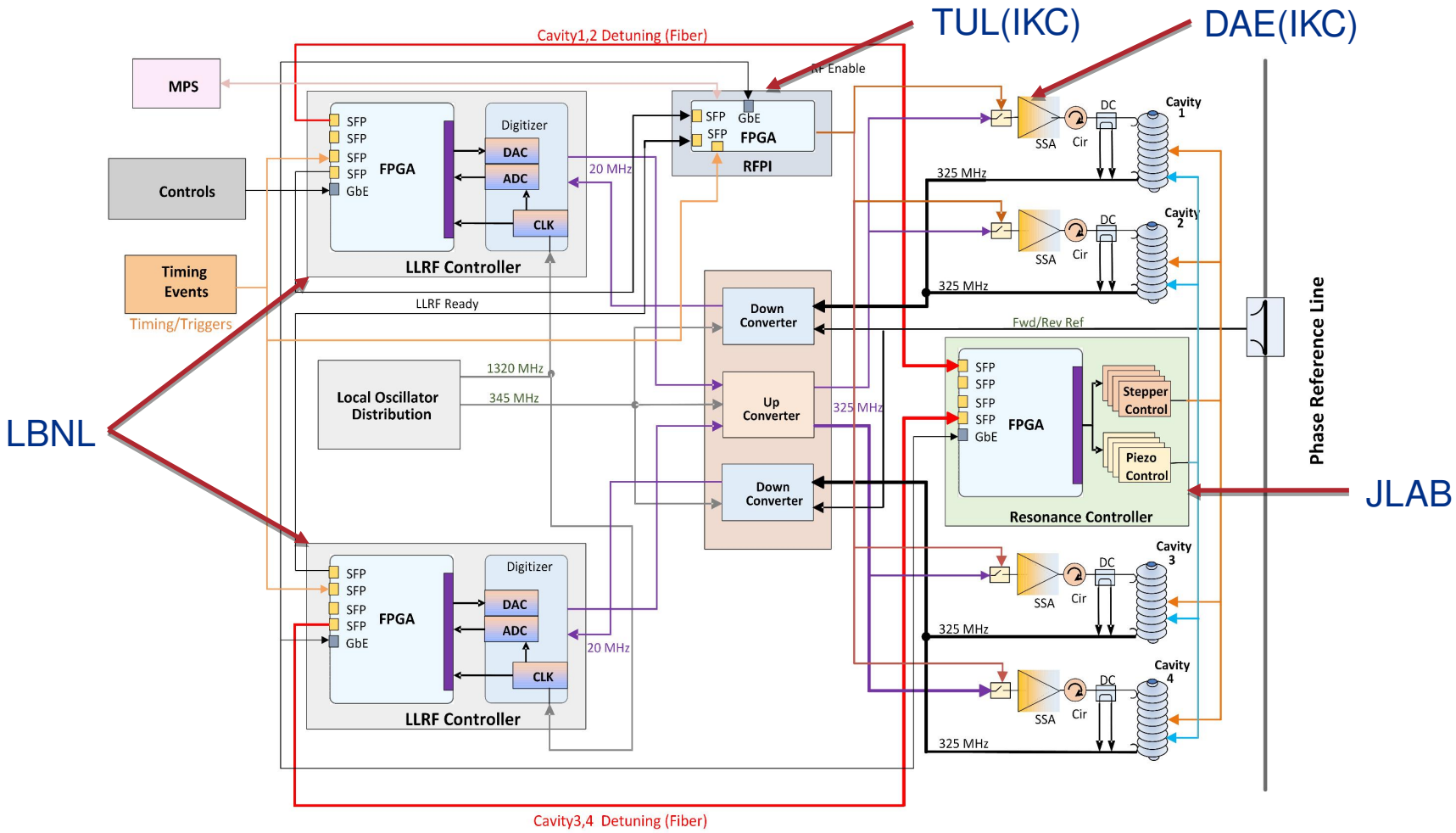


PIP-II Superconducting RF CW Linac

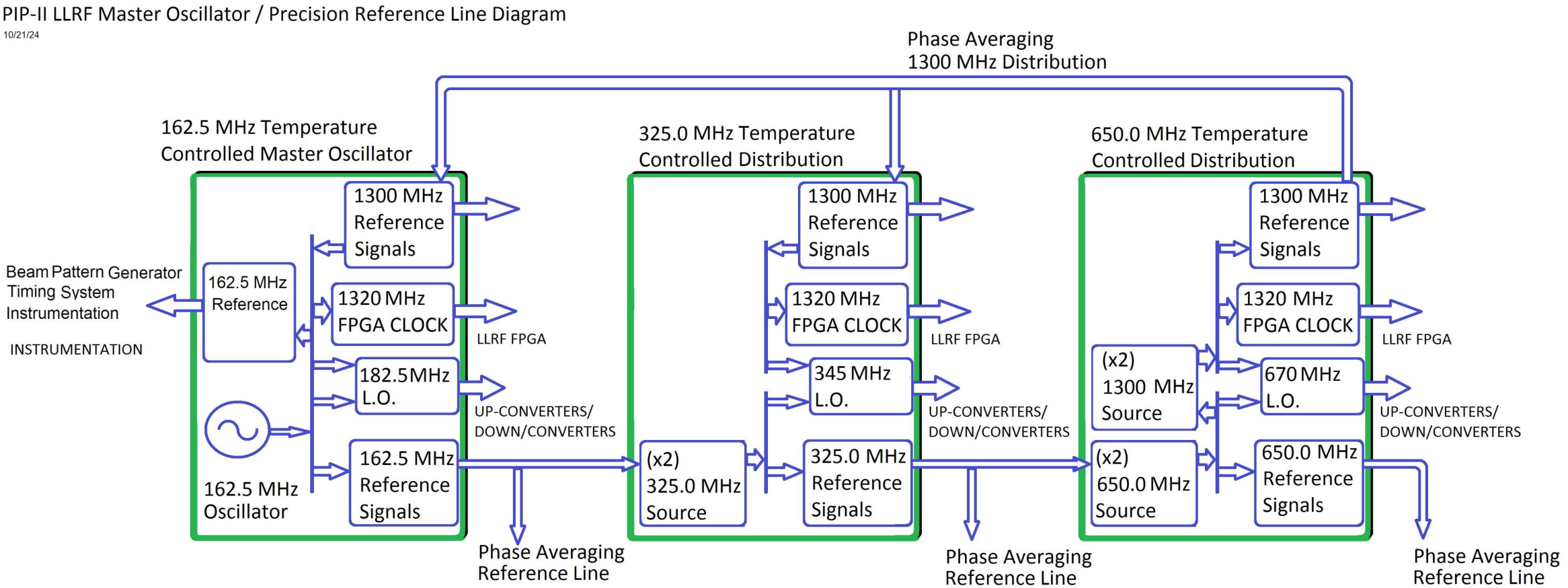


Linac beam injection limited by RF power - 2mA for 0.55ms
For 5 mA from RFQ 60% of beam is chopped out in the MEBT

PIP-II 4-Cavity RF Station



PIP-II Phase Reference and RF Distribution

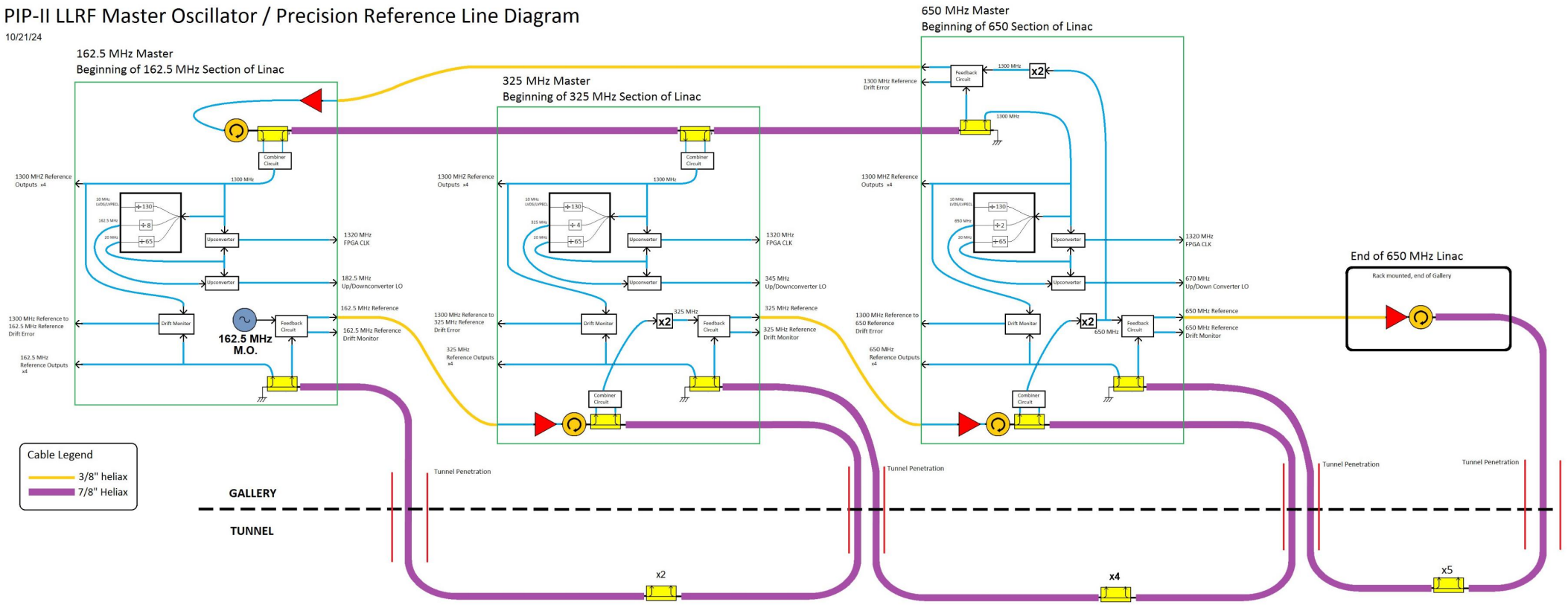


Master Oscillator/Phase Reference Line Requirements

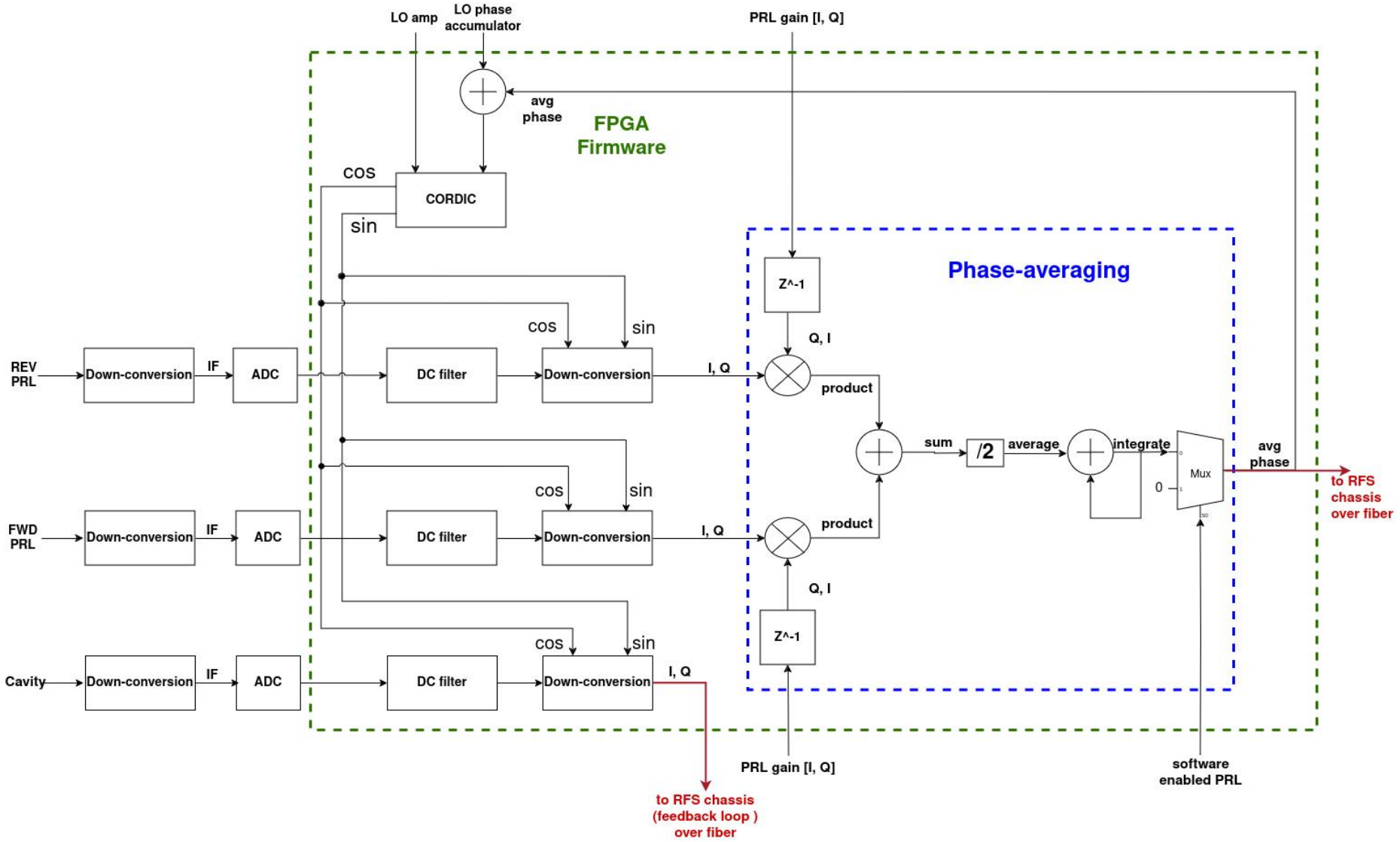
- Operate from single 162.5 MHz low noise oscillator (Wenzel Citrine) >-175dBc/Hz @ 100 kHz and provide signals to interfacing systems and within MO/PRL system as explained in block diagram
- The temperature controller unit shall hold the RF components in the temperature-controlled module at 42 degrees C, +/- 0.5 degree C, for a temperature range from 19 degrees C to 34 degrees C.
- Each M.O. station 36U rack requires a minimum of 2.4 kW/120V, 20A, uninterruptable power (M.O system has 3 stations in total- 162.5MHz, 325MHz, 650MHz) . Power to the M.O. wall mounted enclosure will be provided from the rack. Un-interruptible power is required for component stability, ensuring that that accelerator can recover in a minimum time from a power outage.
- The 162.5 MHz, 325 MHz, 650 MHz , and 1300 MHz reference lines shall be held to 1ps long term phase stability(i.e., 0.233 degrees at 650MHz) for an environment temperature range from 19 degrees C to 34 degrees C.

Master Oscillator/Phase Reference Line

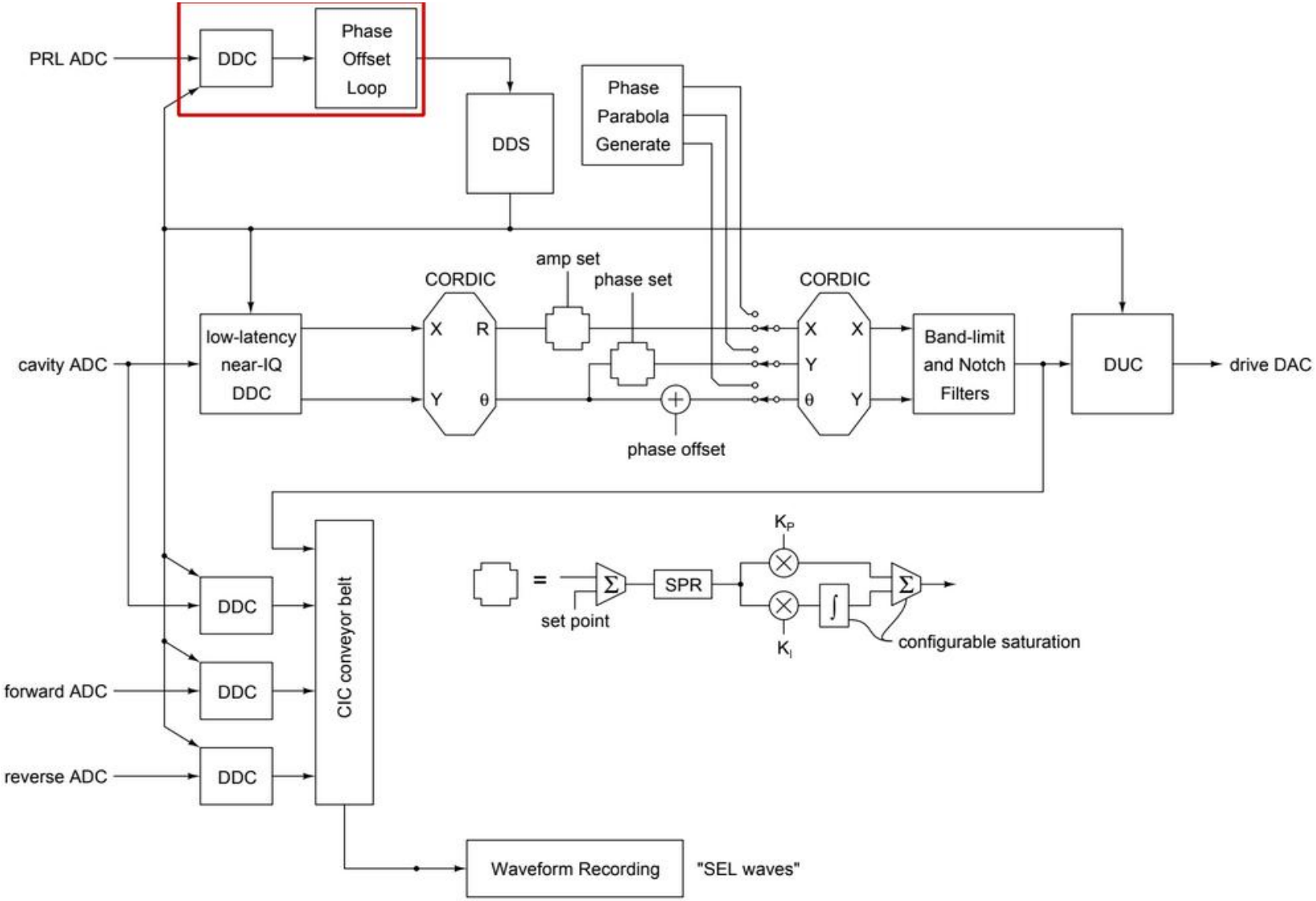
- The MO/PRL system will generate and distribute phase reference RF signals needed for the PIP-II accelerator at 162.5 MHz, 325 MHz, and 650 MHz; LO signals at 182.5 MHz, 345 MHz, and 670 MHz. Additional reference signals of 1300 MHz and 1320 MHz are also distributed.



Digital Phase Averaging in LLRF Controller



Stabilized Phase Reference in LLRF Controller



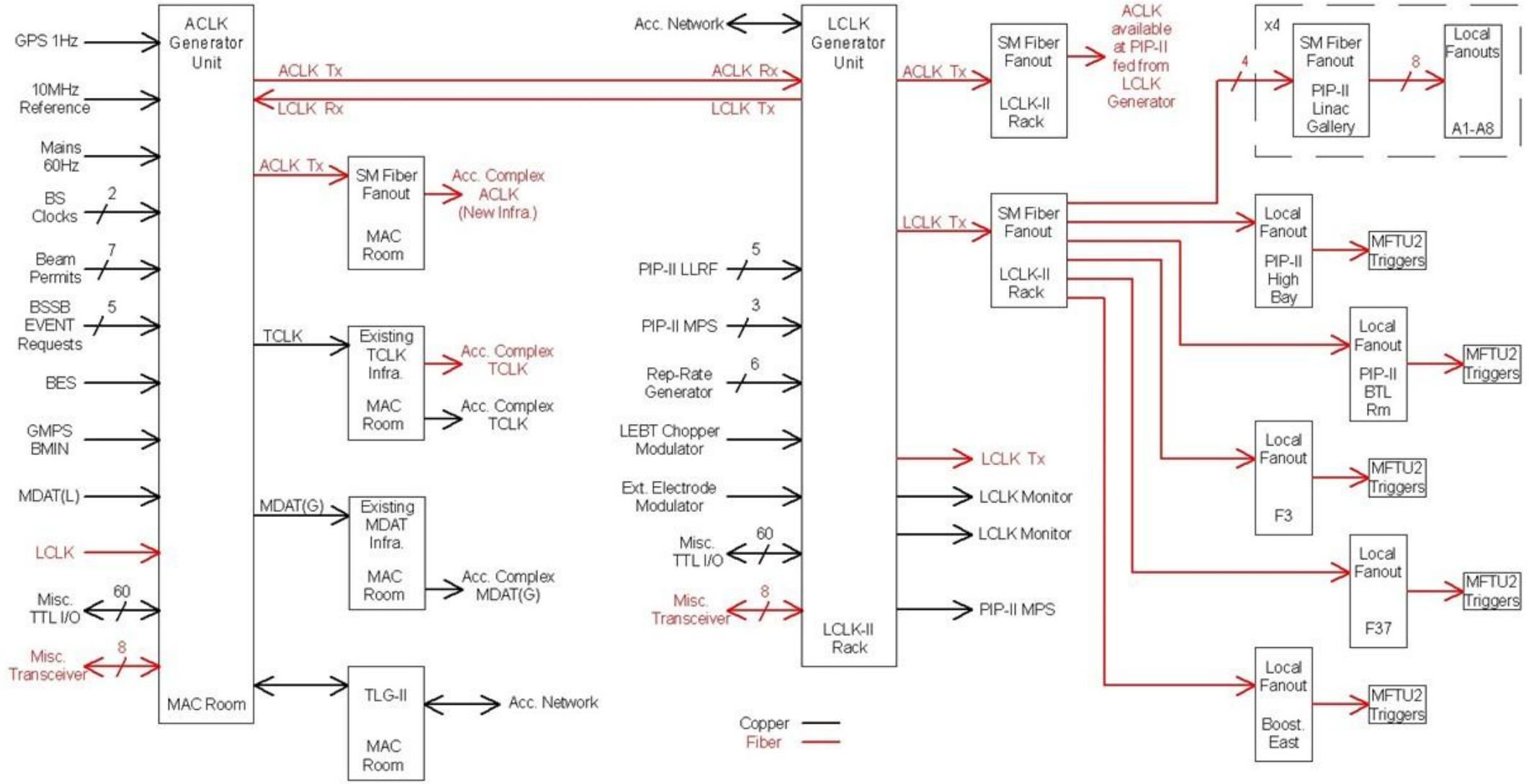
PIP-II Timing System

- The Linac timing system is a two part system. The first part is a global timing system (ACLK) that provides high level, event based timing for the whole Fermilab accelerator complex while the second part is a RF synchronized clock system unique to the PIP-II linac itself (LCLK-II).

- This two level clock system concept has been used at Fermilab (TCLK & individual machine Beam Sync Clocks) to support complex operations through both the Tevatron and Neutrino operational eras.

- PIP-II Source, Linac, BTL and Booster Injection systems are expected to use LCLK-II as their clock system due to its beam synchronous nature.

PIP-II Timing System



See Mark Austin' Poster ID 54 for more details

Clock Frame Definitions

- ACLK uses a GPS based 10 MHz source to create a 650 MHz PLL. This allows for encoding the data within consecutive 65-bit wide frames played out every 100 nS. TCLK compatible EVENTs on ACLK are defined by the lower 8 bits of the EVENT. TCLK would also be played out on a functionally equivalent TCLK output to be distributed to the rest of the Fermilab complex to maintain backwards compatibility with existing hardware.

ACLK Frame	00	MSB LSB	MSB LSB	XXXXXXXX	X	111111
65-bit	2 start bits	16-bit EVENT	32-bit Data	8-bit CRC	Parity bit	pad bits #60-65

Frame Clock = 10 Mhz

- LCLK uses the PIP-II 162.5 MHz RF to create a 650 MHz PLL. This allows for encoding the data within consecutive 72-bit wide frames with 1 frame corresponding to 18 ticks of the 162.5 MHz RF.

LCLK Frame	00	MSB LSB	MSB LSB	XXXXXXXX	X	1111111111111
72-bit	2 start bits	16-bit EVENT	32-bit Data	8-bit CRC	Parity bit	pad bits #60-72

Frame Clock = 9.028 Mhz

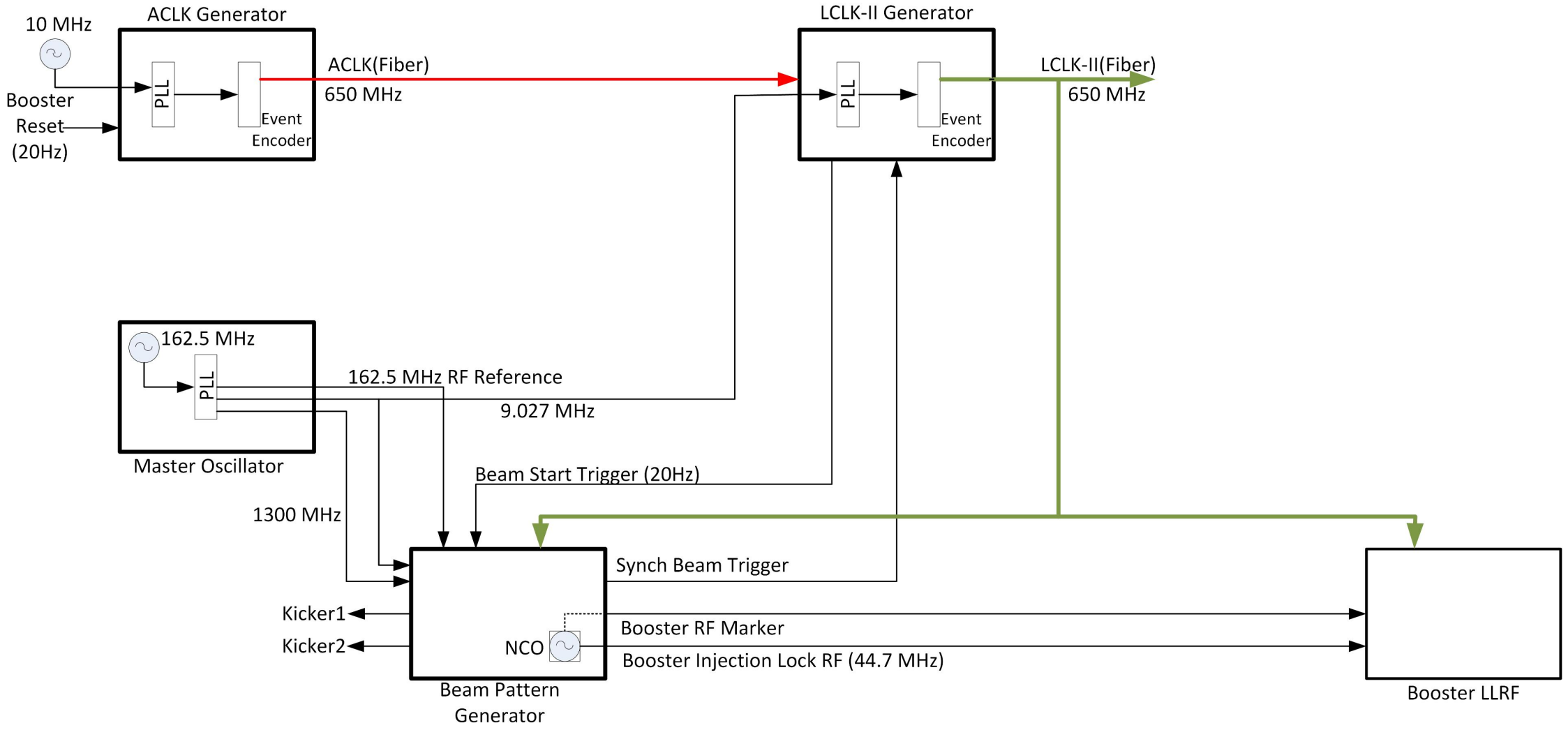
LCLK Events

Event	Description	Priority
$0000	Super Cycle and Master Clock Reset"; marks start of supercycle, ACLK sourced	5
$0002	Time Plot Timestamp Reset: generated once every 50,000,000 TCLK cycles (every 5 seconds); not synchronized to any other event, ACLK Sourced	19
$0007	720 Hz; synchronized to AC line, ACLK sourced	17
$000C	20 Hz; synchronized to GMPS BMIN, ACLK sourced	16
$000F	20 Hz; synchronized to A phase of AC line in MAC room, ACLK sourced	18
$0011	Booster Reset for Null Cycle, ACLK sourced	6
$0012	Booster Reset for Pre-Pulse Cycle, ACLK sourced	7
$0013	Booster Reset for MI/Fixed Target Beam Cycle, ACLK sourced	8
$0014	Booster Reset for MI/Muon Beam Cycle, ACLK sourced	9
$0015	Booster Reset for MI/NuMI Beam Cycle, ACLK sourced	10
$0016	Booster Reset for MI/Fixed Target Beam Cycle, ACLK sourced	11
$0017	Booster Reset for Booster Study Beam Cycle, ACLK sourced	12
$0019	Booster Reset for MI/NuMI Beam Cycle, ACLK sourced	13
$001C	Booster Reset for MI/Muon Beam Cycle, ACLK sourced	14
$001D	Booster Reset for BNB Beam Cycle, ACLK sourced	15
$008F	1 Hz; Generated by GPS RCVR in computer room, ACLK sourced	20
$0201	LINAC Start of Beam Event; triggered by Linac LLRF	1
$0202	LINAC HEP Beam Request Event; triggered by BSSB	2
$0203	LINAC Studies Beam Request Event; triggered by BSSB	3
$0204	LINAC Start of CW Studies Beam Event; triggered by Linac LLRF?	4
$0208	"Beam Event"; Beam cycle event triggered by LEBT Chopper Modulator	27
$0209	"Beam Event"; Beam cycle event triggered by Extraction Electrode Modulator	28

Beam Transfer Sequence to Booster

- PIP-II and Booster RF frequencies are non-harmonic, requiring the pulsed beam to be chopped so that the passed pulses are injected into a phase acceptance window
- The ACLK Generator will generate a Start of Beam event at a 20Hz repetition rate
- The LCLK-II Generator will reflect the Start of Beam event on LCLK-II ($201)
- The Beam Pattern Generator synchronizes this event to the 162.5 MHz beam pulse, starts playing the appropriate (stored) beam pattern and issues a synchronized beam start trigger to the LCLK-II generator
- The BPG provides the injection RF and a marker for the Booster to lock to.

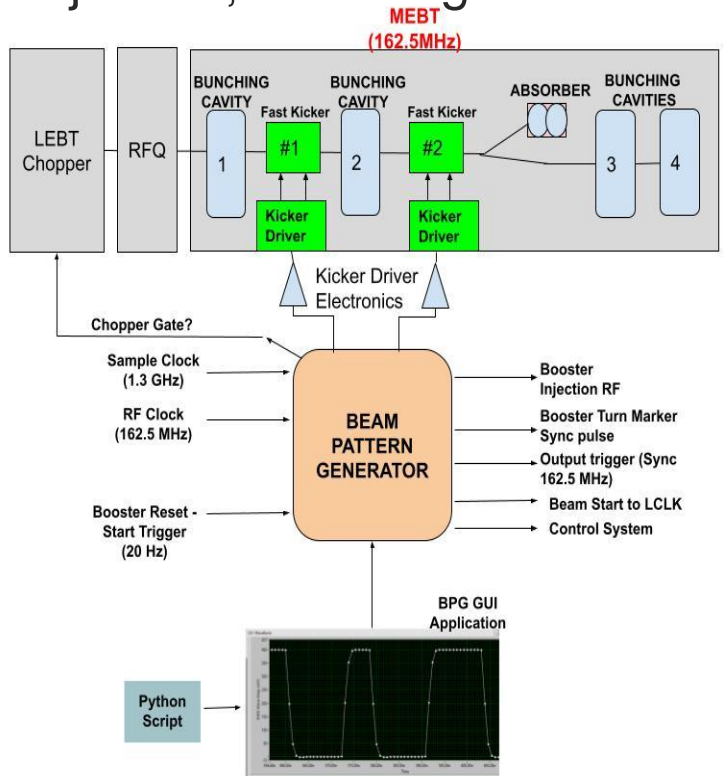
PIP-II Timing System Components



Beam Pattern Generator – System Design

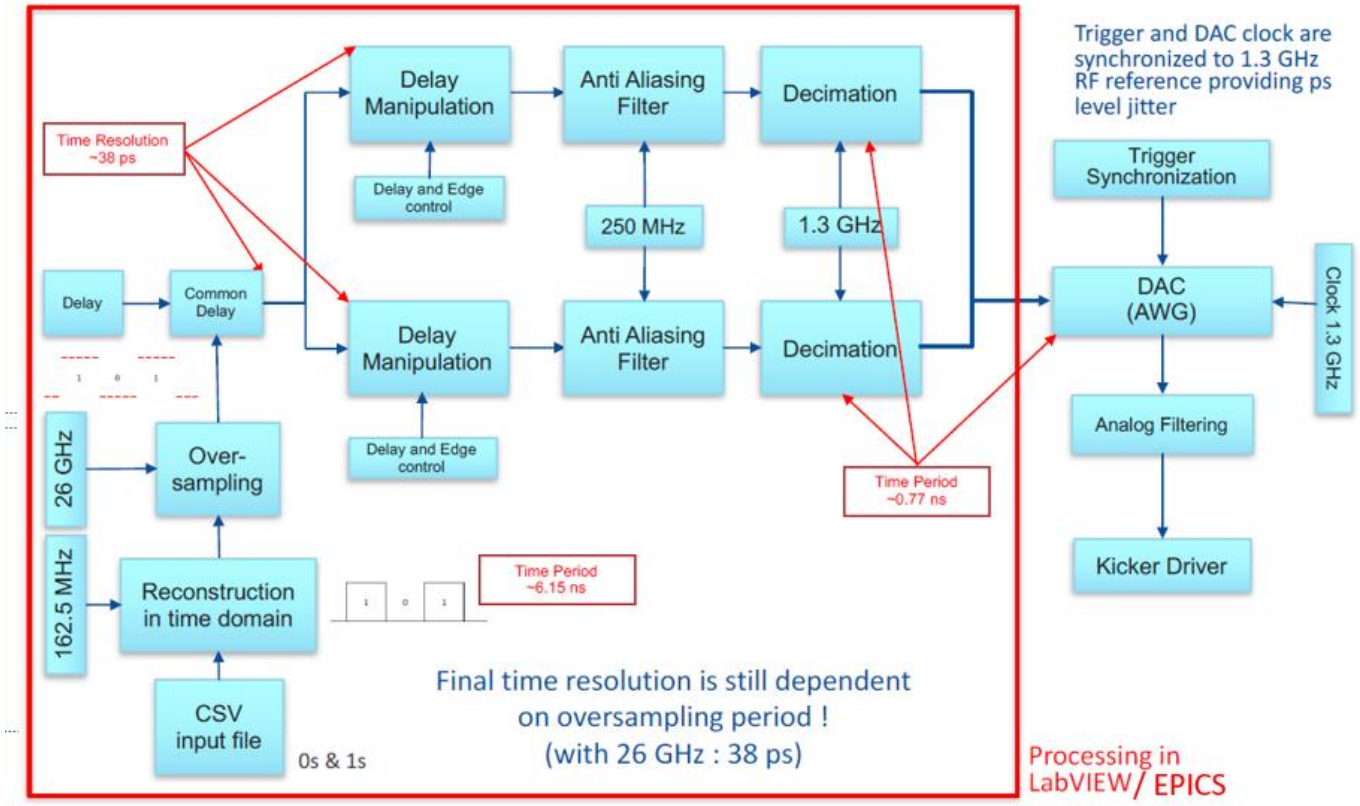
- Synchronize beam injection and the RF systems between PIP-II Linac and the Booster
- Synchronization is accomplished by controlling two MEBT beam choppers, which select 162.5MHz beam bunches from the LEBT and RFQ to produce an appropriate reduced beam bunch pattern that enables bucket-to-bucket transfer to the Booster RF at 46.46MHz (84th Revolution Harmonic)
- Reduces the beam current to an average of 2mA over the Booster injection, matching the Linac nominal beam current

- The Beam Pattern Generator (BPG) is the system that determines the bunch pattern as requested by experiment or by the Booster injection, and provides
  - drive to the MEBT Fast Kickers
  - the capability to drive the LEBT Chopper
  - the injection RF frequency/ phase reference which the Booster will phase lock to during injection signal which the Booster will lock to
  - a sync pulse for the Booster to generate the Booster revolution marker.



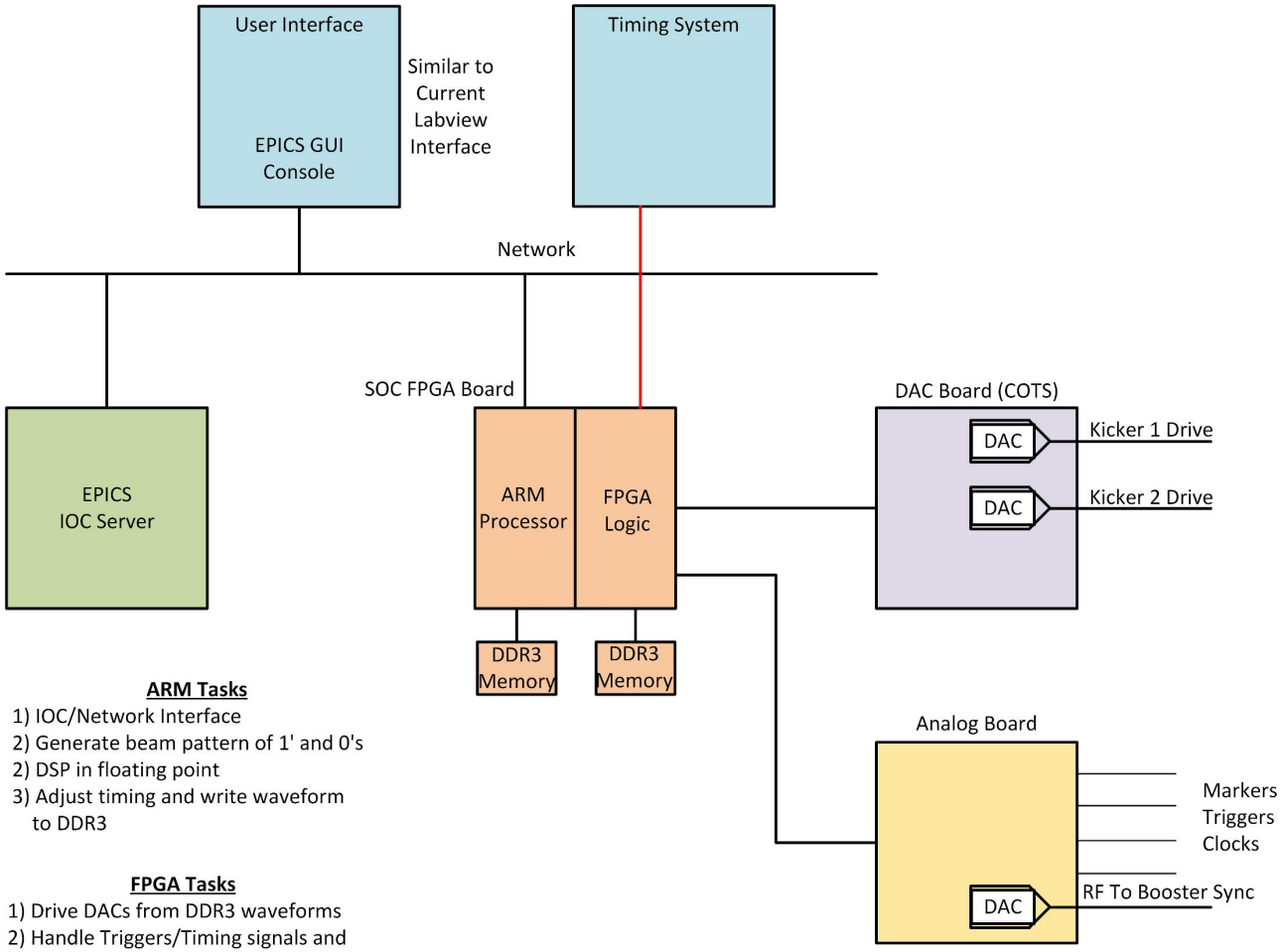
Beam Pattern Generator – Signal Processing

- External trigger as input in synchronizing circuit, will create an output trigger precisely aligned with the 162.5 MHz and the 1300 MHz RF
- Sub 1300 MHz period alignment is done so that the trigger maintains the setup and hold time requirements of the AWG input circuit
- Stable AWG output to the order of picoseconds
- Fine tunning resolution and precision requirements can be met with the 1.3 GSPS clock rate
- This sample rate allows the generation of a 650 MHz bandwidth signal with exact timing and amplitude
- Timing resolution ~38 ps, Virtual sampling rate 26 GSPS
- Final signals are digitally filtered to below the 650 MHz Nyquist frequency, then downsampled to 1.3 GSPS
- Analog reconstruction filter for DAC outputs



Beam Pattern Generator – Upgrade

System Architecture



ARM Tasks

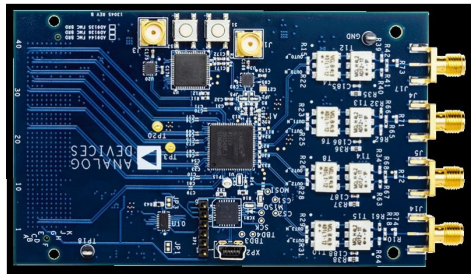
1) IOC/Network Interface
2) Generate beam pattern of 1' and 0's
2) DSP in floating point
3) Adjust timing and write waveform to DDR3

FPGA Tasks

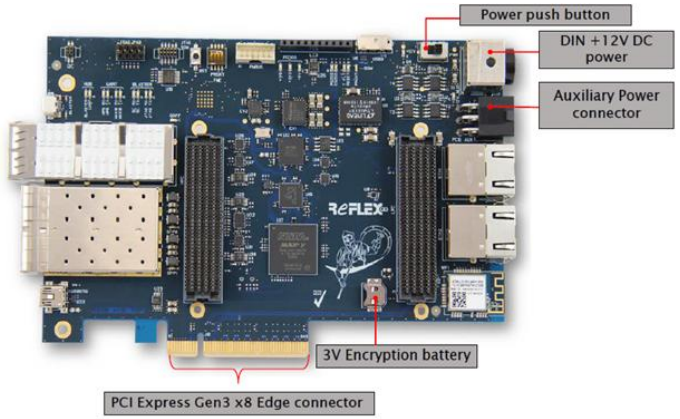
1) Drive DACs from DDR3 waveforms
2) Handle Triggers/Timing signals and markers

COTS Hardware Components

Arria10 SOM



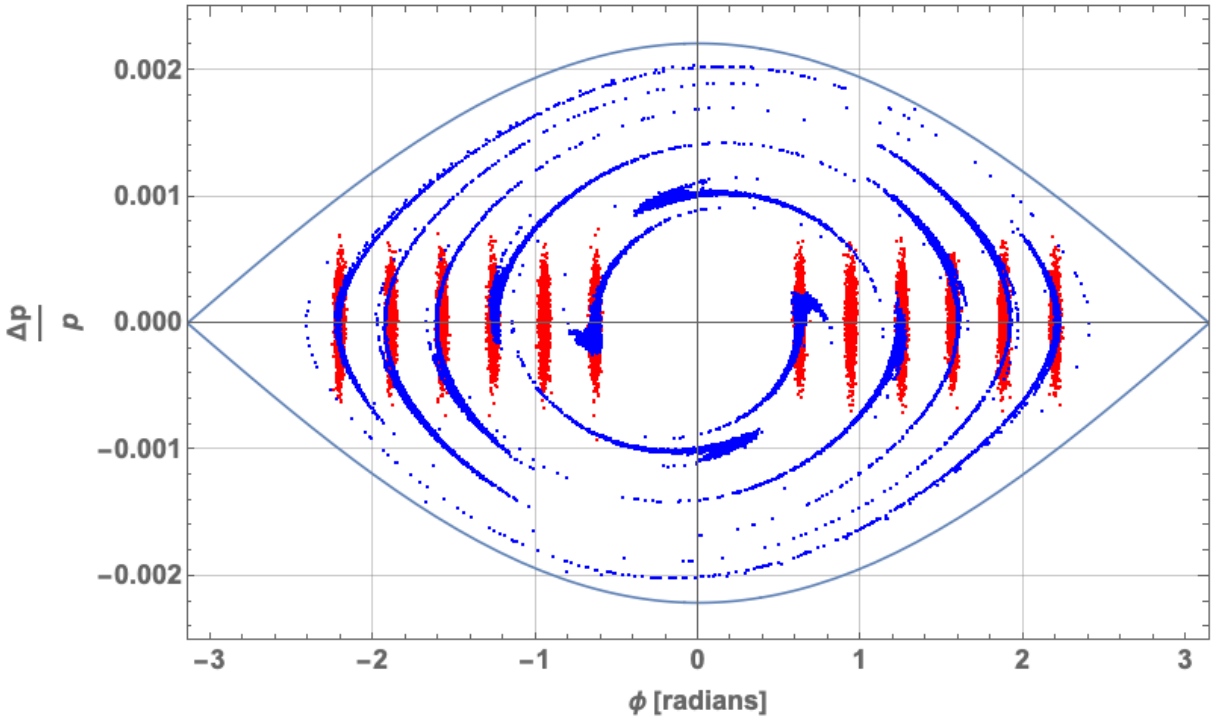
2 ch HS DAC Board
AD9136-FMCEBZ
16-bit, 2.8 GSPS, Ext Clk Input

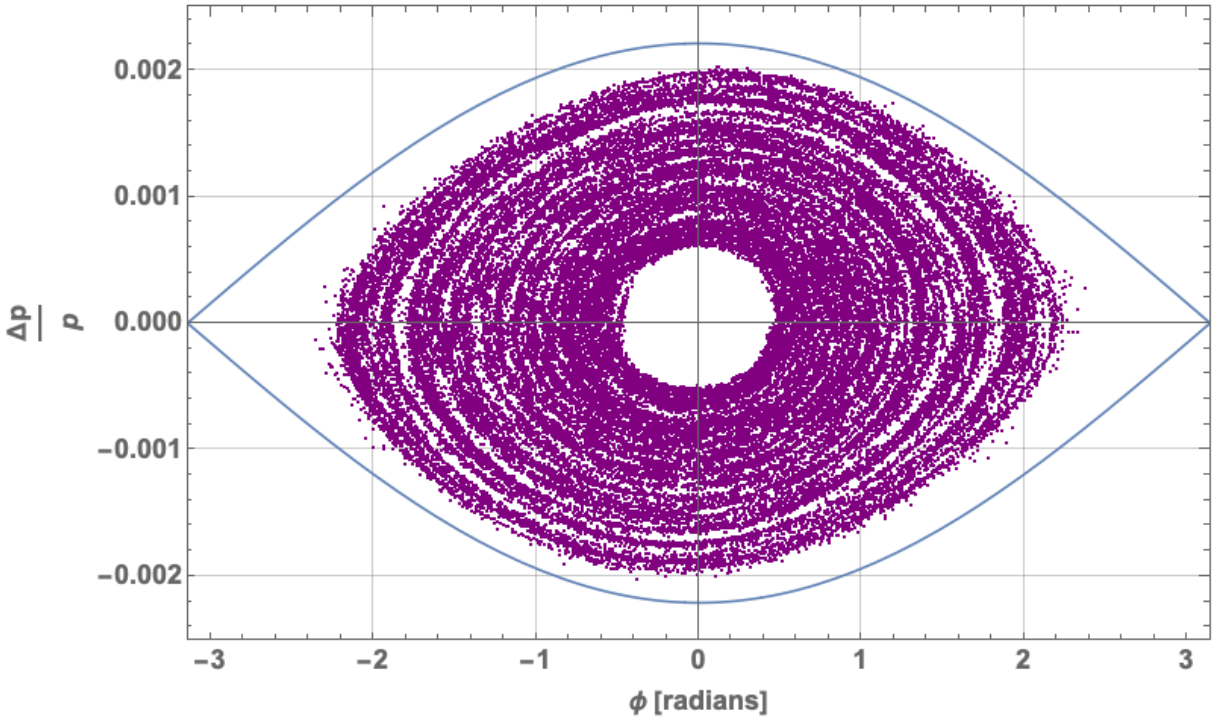


Carrier Board

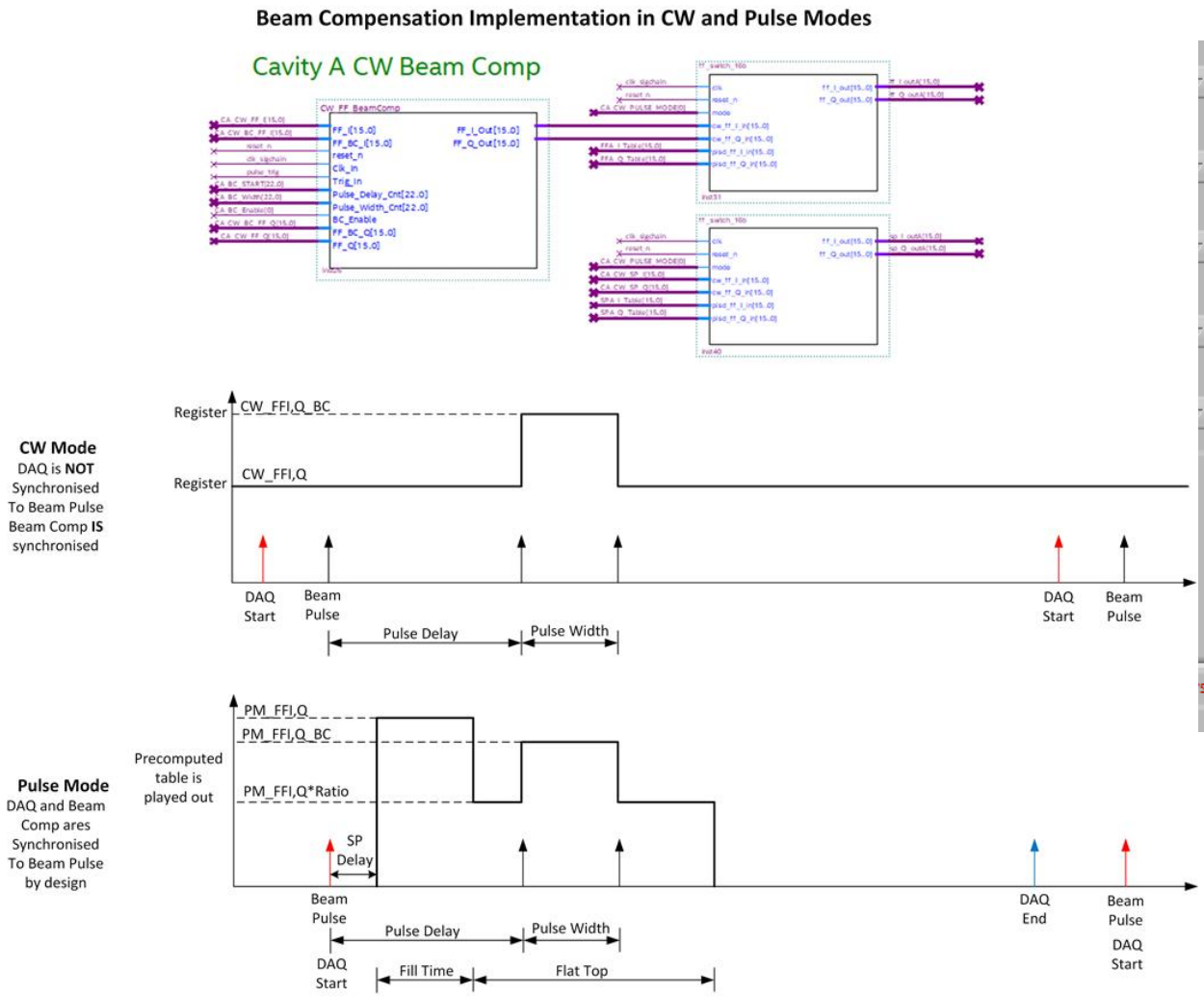
On Momentum Booster Injection Scheme for PIP-II

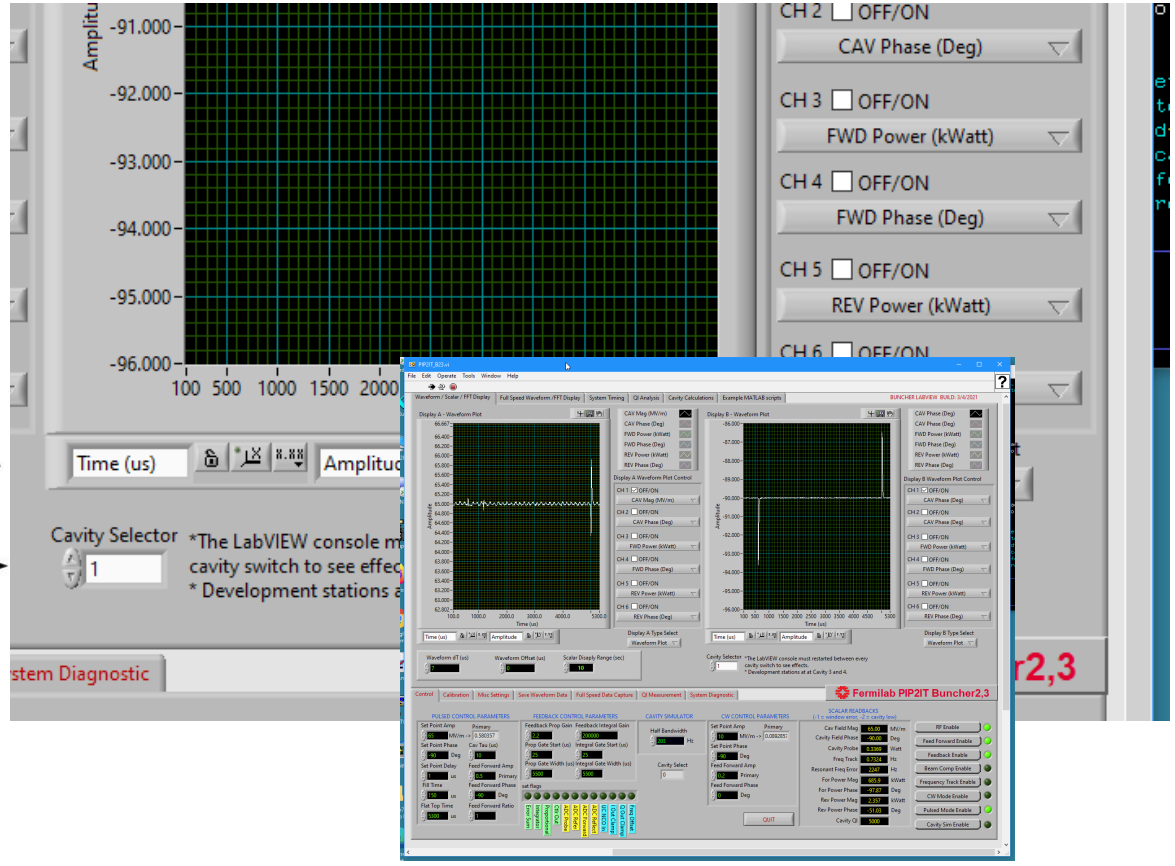
- Proposed overlap area for beam injection. The red dots are representative of beam in the incoming Linac buckets, the green dots are after 292 turns. Linac bucket centroids are chosen to be in the range {−0.7π, −0.15π} or {0.15π, 0.7π}





Beam Loading Compensation – Buncher 2





Summary

- PIP-II Timing System Design is being finalized
- LLRF Phase Reference Line design work is progressing
- Beam pattern generator operation was tested with a prototype at PIP-2IT. A final design with hardware upgrade is in progress
- All above subsystems have Final Design Reviews in 2025
- The Cryomodule Test Stand (CMTS) will provide an additional test bed for validating these systems

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