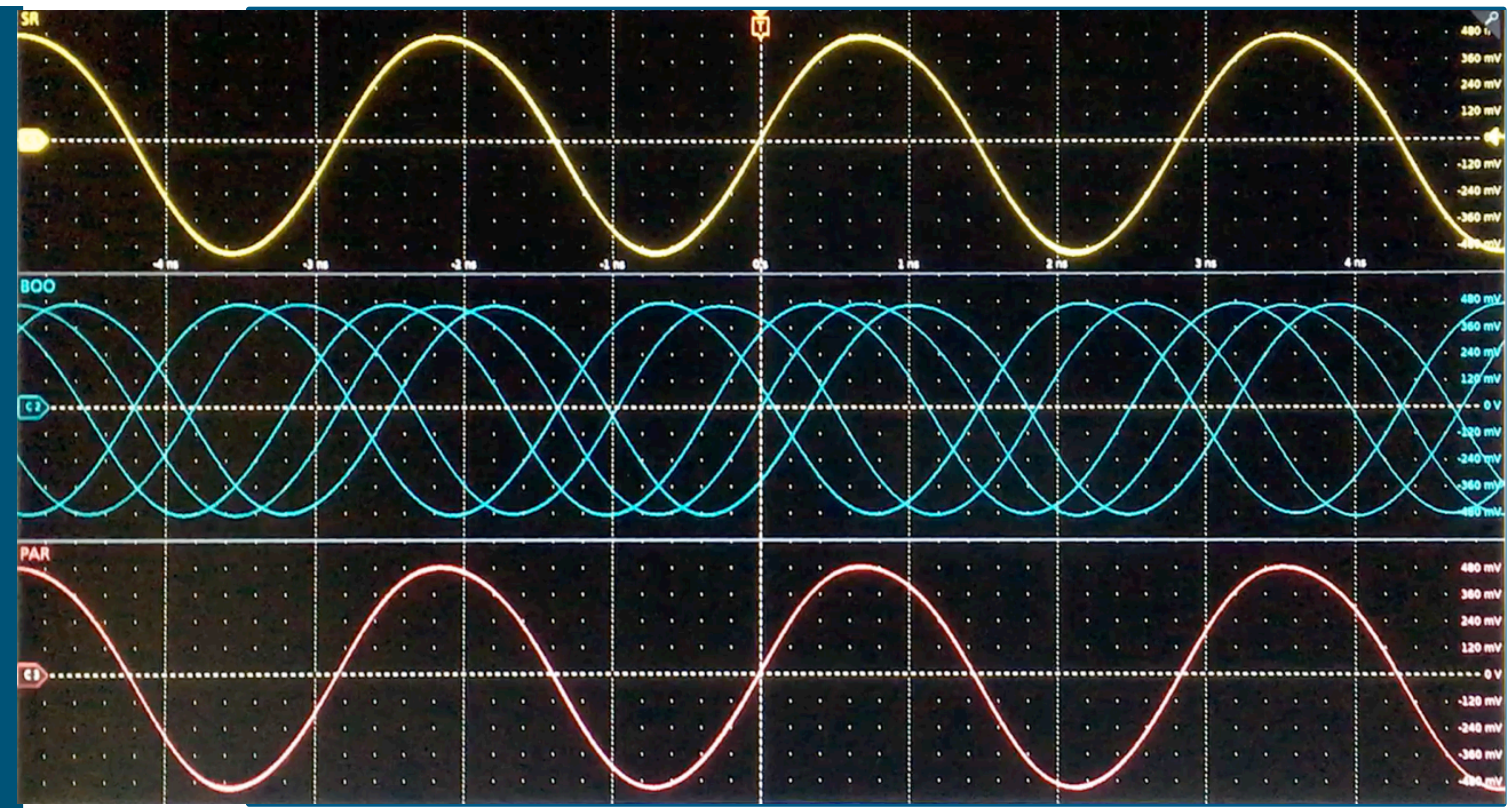
IETS: The APS Injection/Extraction Timing System



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APS-Upgrade Project

- World-class ultra-low emittance upgrade of the APS
  - 40-period MBA Lattice with reverse bends to lower emittance
  - 6 GeV, 200 mA, 42 pm-rad electron-beam emittance MBA lattice.
  - 100-fold increase in X-ray beam brightness.
- Superconducting bunch-lengthening cavity running at 2K
  - presently at 550 kV design 1.25 MV.
- Swap-out injection rather than top-up due to machine acceptance.
- Completed end of March 2024, in user ops since July 2024.
- Presently running at 140 mA in 162 bunches at nominal 42 pm-rad electron-beam emittance.
- Uptime ≈ 93%

Project Key Performance Parameters

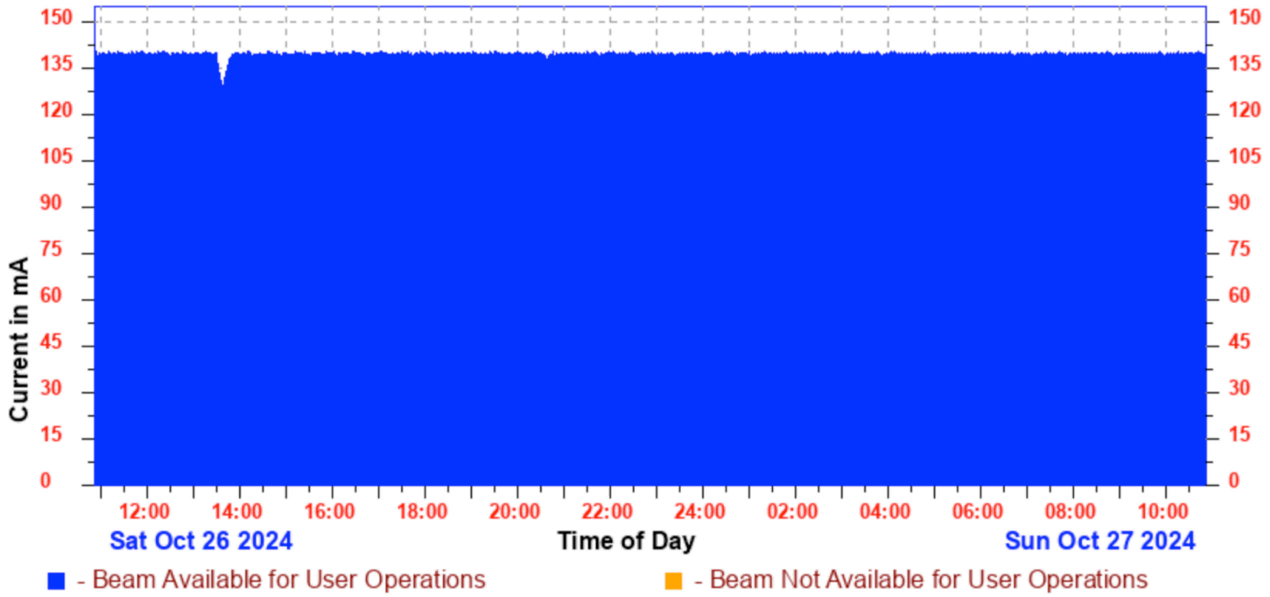
Key Performance Parameter	Thresholds (Performance Deliverable)	Objectives
Storage Ring Energy	> 5.7 GeV, with systems installed for 6 GeV operation	6 GeV
Beam Current	$\geq$ 25 mA in top-up injection mode with systems installed for 200 mA operation	200 mA in top-up injection mode
Horizontal Emittance	< 130 pm-rad at 25mA	$\leq$ 42 pm-rad at 200mA
Brightness @ 20 keV[1]	> 1 x 10^{20}	> 1 x 10^{22}
Brightness @ 60 keV[1]	> 1 x 10^{19}	> 1 x 10^{21}
New APS-U Beamlines Transitioned to Operations	7	$\geq$ 9

[1]photons/sec/mm^2/mrad^2/0.1%BW

Accelerator, Front Ends and IDs, and Experimental Systems

Upgraded APS 24 hours History

14 beam lines active
for this particular period



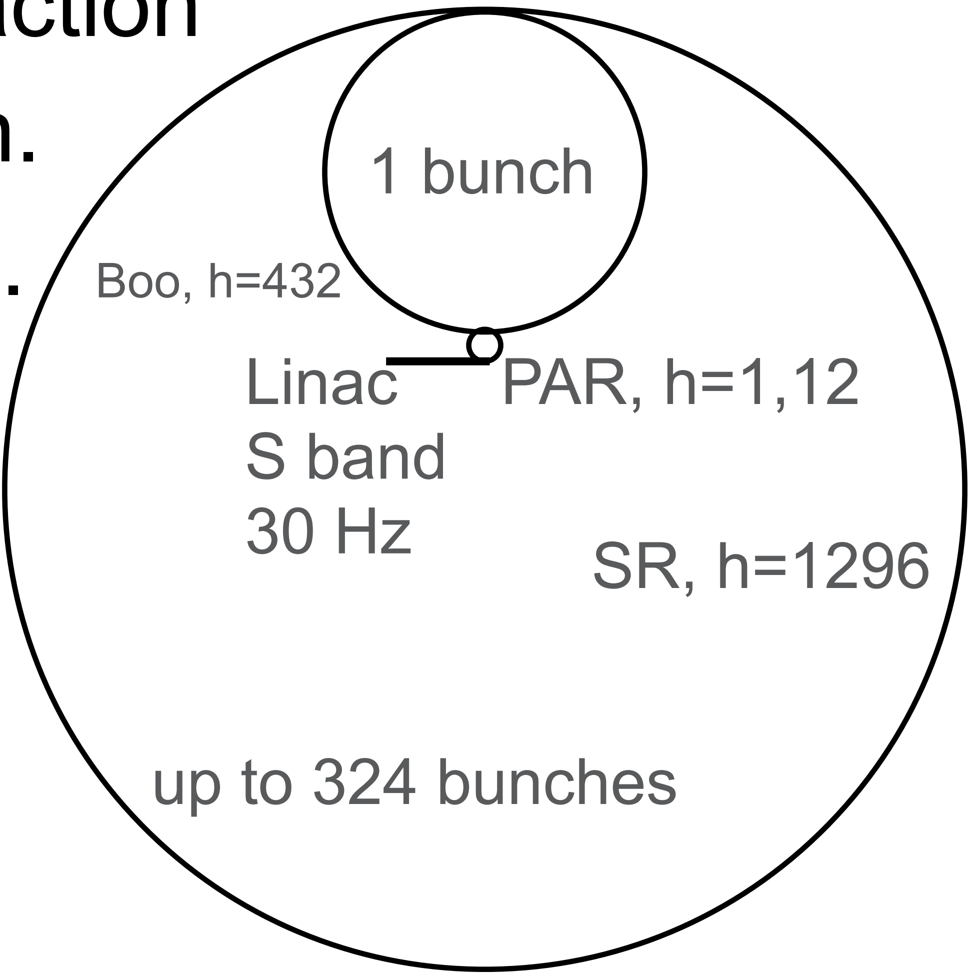
Motivation & Requirements for IETS

- APS had 1104 m circumference and ran at 351.930277 MHz
  - Booster at 1/3 the circumference ran at SR rf
- APS now has 1103.682 m and runs at 352.055282 MHz
  - 125 kHz difference, Booster could not follow that
- Adjusting Booster length would have been non-trivial rebuild
- => Consider running Booster at different rf than APS sr
  - Vary Booster frequency to synchronize and target bunch into sr bucket.

- Requirements
  - ≤ 50 ps timing jitter (bunch vs SR rf; triggers of strip-line kickers)
  - Ability to prevent swap-out if substandard bunch in Booster
  - "Slow Beam Abort" decohere-dump bunches in short order.

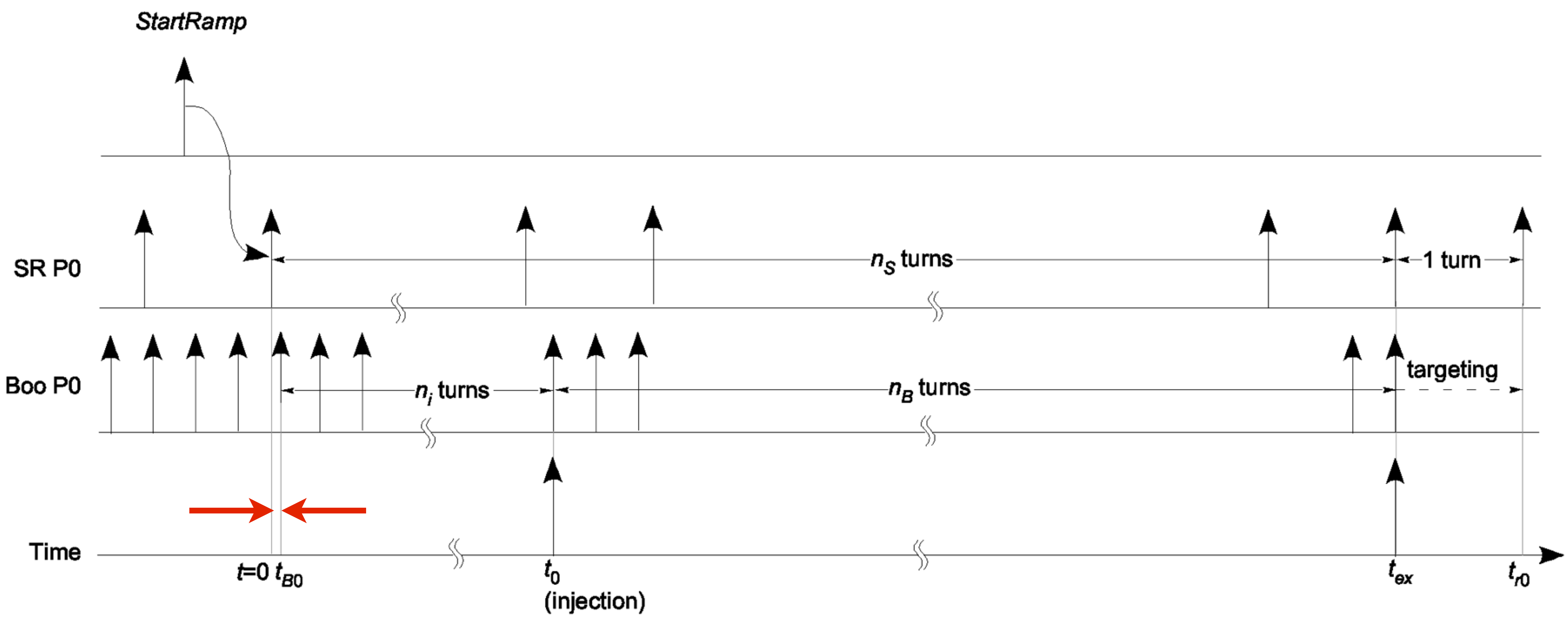
Fundamental Idea

- Rational relation between Booster and sr rf:
  - $f_{Boo} = f_{SR}\bullet(1\text{-}1/N) = f_{PAR}\bullet 36$, N integer, at Booster injection
- Vary Booster rf to target sr bucket and back before extract. After Booster extraction, ramp Booster rf back so Booster appears as if variation never happened.
- **Bonus**: Can ramp Booster rf to extraction and back, for emittance manipulation.
- Frequency ramp and targeting bump.
- **Pipelining**: PAR accumulates linac pulses while Booster accelerates.



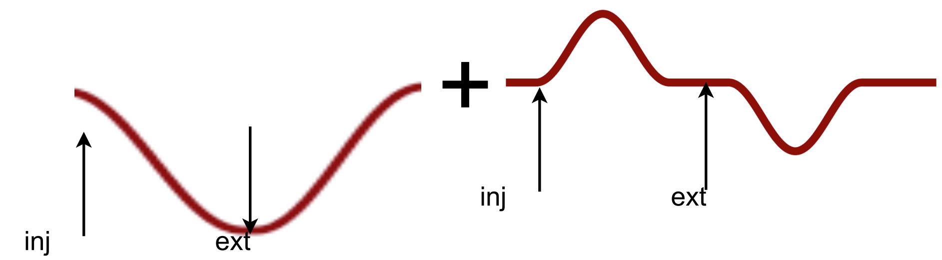
Booster Acceleration Cycle

- The Booster magnet cycle is aligned to the 60-Hz phase of the mains
  - Jitters by 100s of μs against absolute time; rf cycles not reproducible.
  - The rings have an arbitrary orientation against each other at StartRamp.
- This is dealt with by detecting the sr revolution clock “P0” and tie the algorithm to that.
  - Booster orientation kept track of by “Orientation Counter”



Frequency Variations

- For the frequency variation in booster, choose cosine-like shape to minimize transients.
  - Frequency ramp and “bump” for targeting:
  - c is time in sr rf periods



$$\Delta f_{Boo} = \Delta f_{ramp}\left(\begin{cases} 0 & c \le c_0 \\ \frac{1}{2} - \frac{\cos\left(\frac{\pi(-c_0+c)}{c_1-c_0}\right)}{2} & c_0 < c \le c_1 \\ 1 & c_1 < c \end{cases}\right) + \frac{\left(\Delta f_{tgtfwd} + \Delta f_{0\,fwd}\right)}{2}\left(\begin{cases} 0 & c \le c_0 \\ 1-\cos\left(\frac{2\pi(-c_0+c)}{c_1-c_0}\right) & c_0 < c \le c_1 \\ 0 & c_1 < c \end{cases}\right)$$

$c_0 > c_{inj}$
$c_1 < c_{ex}$

  - time shift can be calculated (from the integral of the above):

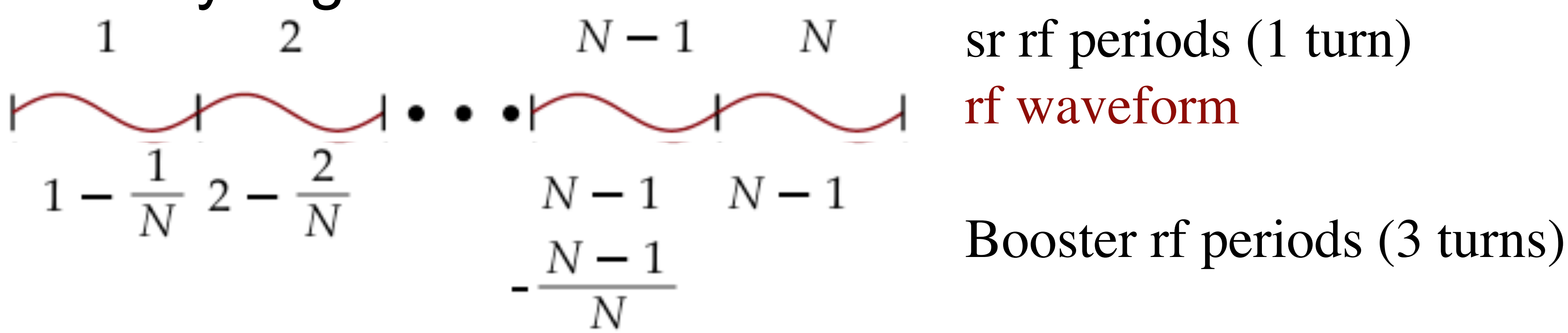
$$\Delta c = \frac{\left(-\frac{c_0}{2} - \frac{c_1}{2} + c_{ex}\right)\Delta f_{ramp}}{f_{SR}} + \frac{\left(-\frac{c_0}{2} + \frac{c_1}{2}\right)\Delta f_{0\,fwd}}{f_{SR}} + \frac{\left(-\frac{c_0}{2} + \frac{c_1}{2}\right)\Delta f_{tgtfwd}}{f_{SR}}$$

time shift in sr rf periods

- The time-shift expression can be solved for the bump height coefficient.

Keeping track of Ring Orientations

- To calculate the targeting bump, system needs to know relative orientation of sr and Booster at Booster injection.
- This is done with the "Orientation Counter"™:
  - $n_{sr} \bmod (N^*1296)$. Count sr rf periods. Goes through 0 every time the rings are precisely aligned.



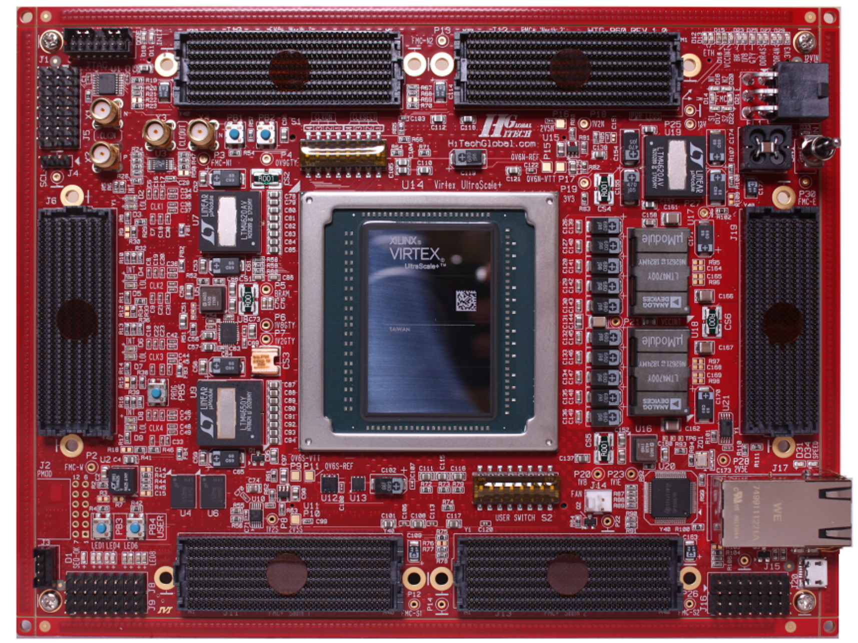
  - After 1296*N sr rf periods, Booster had made 1296 less rf periods than SR, => perfect alignment as at beginning, OC = 0. Resolution is $1/N$.
  - Sampling OC at "Start Ramp" provides the info to calculate the exact bump amplitude, hence generate the frequency program.
- bump+ramp add integer no. of Booster turns in one cycle.

Implementation

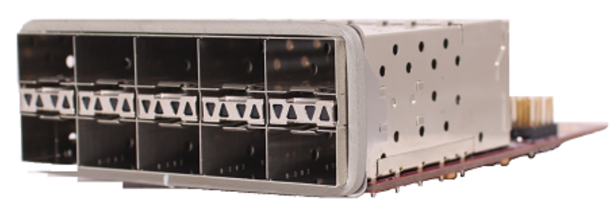
- Rf reference generation using DDS (firmware).
  - 48 bit tuning word; 16 bit DACs.
- BTC (Booster Timing controller) central component
  - Rf cycle counting, internal turn clock generation
  - Interface to IOC for cycle parameters
  - Calculate rf program, upload to the DDSs for play-out.
  - Two MicroBlaze cores, one with FPU, for IOC interface and for start-up calculations for frequency program.
    - actual frequency tables calculated in FPGA fabric, ≈1500 pts. for Booster cycle.
  - works at 187.5-MHz clock frequency $(f_{SR}+f_{IF})/2$
- Integrate with existing APS timing and IOCs
  - This allowed frequent testing of the new system at the APS, as it was being built up.
  - Biggest difference is N: 92377 at APS; 2713 at APS-U.

Major Hardware Components

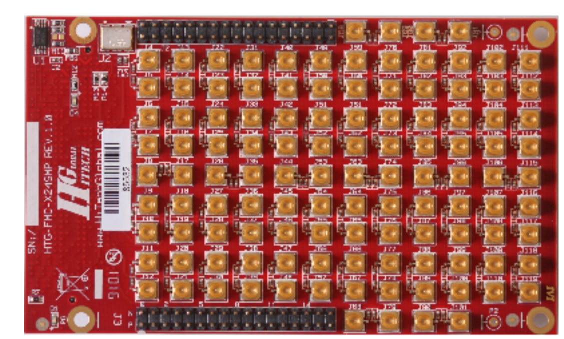
- **HiTech Global HTG-960**
  - Virtex Ultrascale+ FPGA
  - 8,938K Logic Cells
  - 75.9 Mb Block RAM
  - 3,840 DSP Slices
  - 80 GTY (32.8Gbps)Transceivers
  - 6 FMC+ Connectors
  - 80 GPIO pins
- **HiTech Global HTG-FMC-X10SFP+**
  - 10 SFP+ cages
- **HTG-FMC-x24MSMP**
  - Provides Mini SMP connector interface to transceiver data and clock signals
  - 64 GPIO pins
- **DC2303A (x3) not shown**
  - 16-bit DAC from Analog Devices



HTG-960



HTG-FMC-X10SFP+



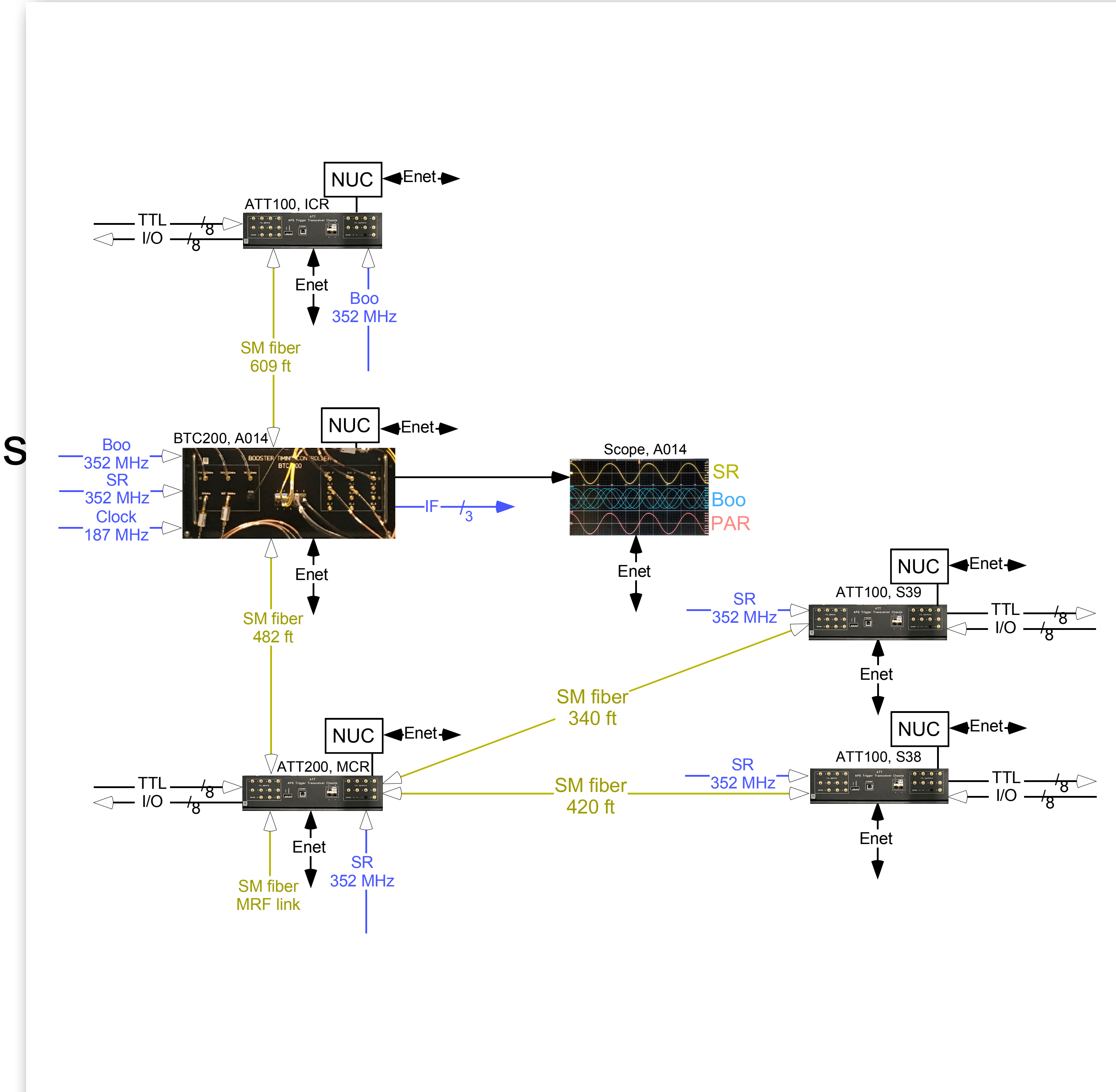
HTG-FMC-x24MSMP

Details

- The BTC has three clock domains to work with:
  - BTC clock; $(f_{SR}+f_{IF})/2$, ≈ 187.5 MHz
  - f_{SR} = 352.055282 MHz
  - Booster/PAR rf, 319.933083 MHz
- Each counting input is run through a 2-stage synchronizer (shift register) to reduce jitter to an acceptable level
- The frequency program is calculated in terms of BTC clock periods, which is $(1/f_{SR})/(f_{clk}/f_{SR})$. (f_{clk}/f_{SR}) is a *rational* number
- A "rear porch" (frequency offset) added to each program cycle ensures Booster rf program is exactly transparent at the end of the cycle (done in tuning-word space).
- About 30 ms are available after StartRamp to calculate and setup the frequency program. Actual use is about 100 µs.

High-Level Schematic

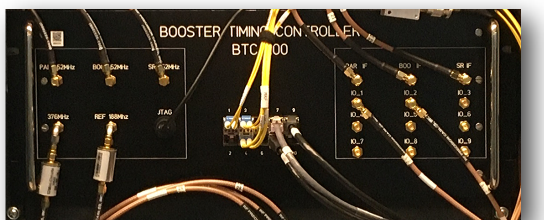
- BTC
  - implements the DDSs
  - calculates frequency program parameters
  - calc. & uploads the targeting bumps and the ramp to the DDSs
  - reads & monitors fiducials and frequencies.
  - counts the rf periods
  - monitors charge in Booster
- ATTs
  - generate hardware triggers
- Fibers are 8b/10b encoded SM fibers.

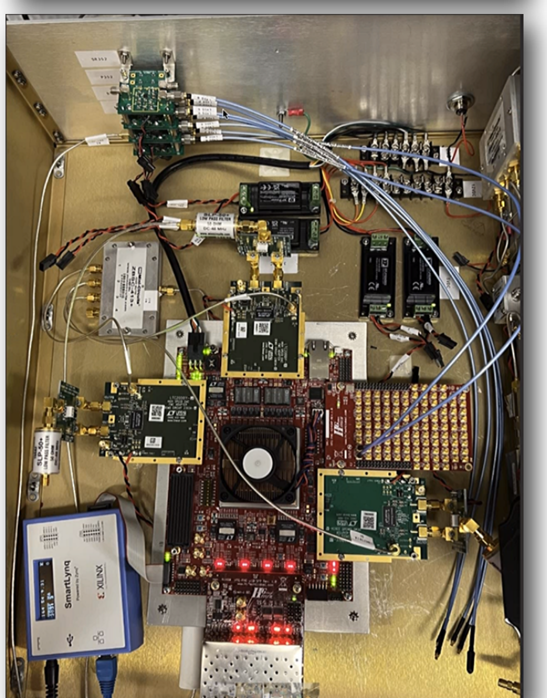


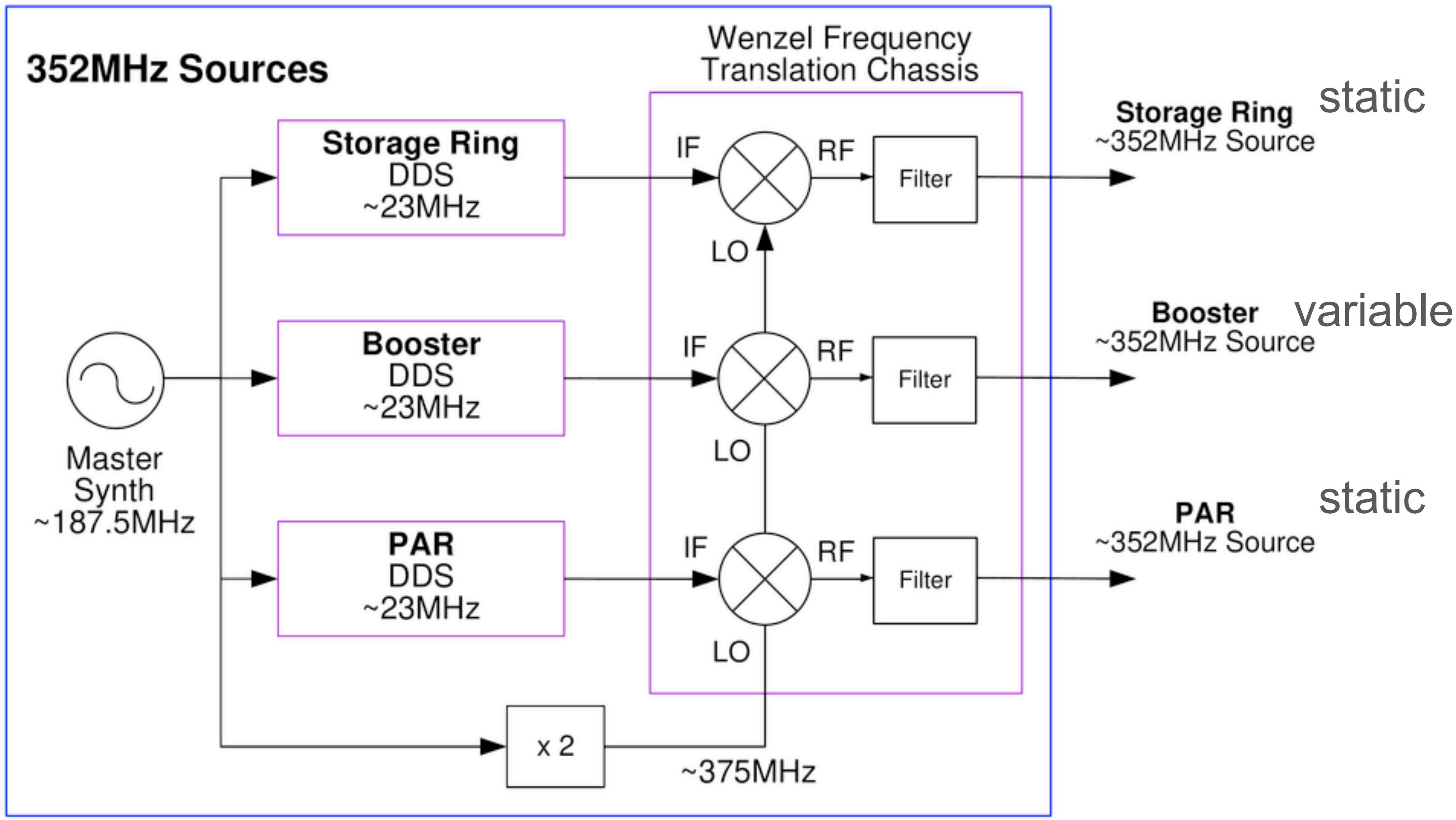
Frequency Sources

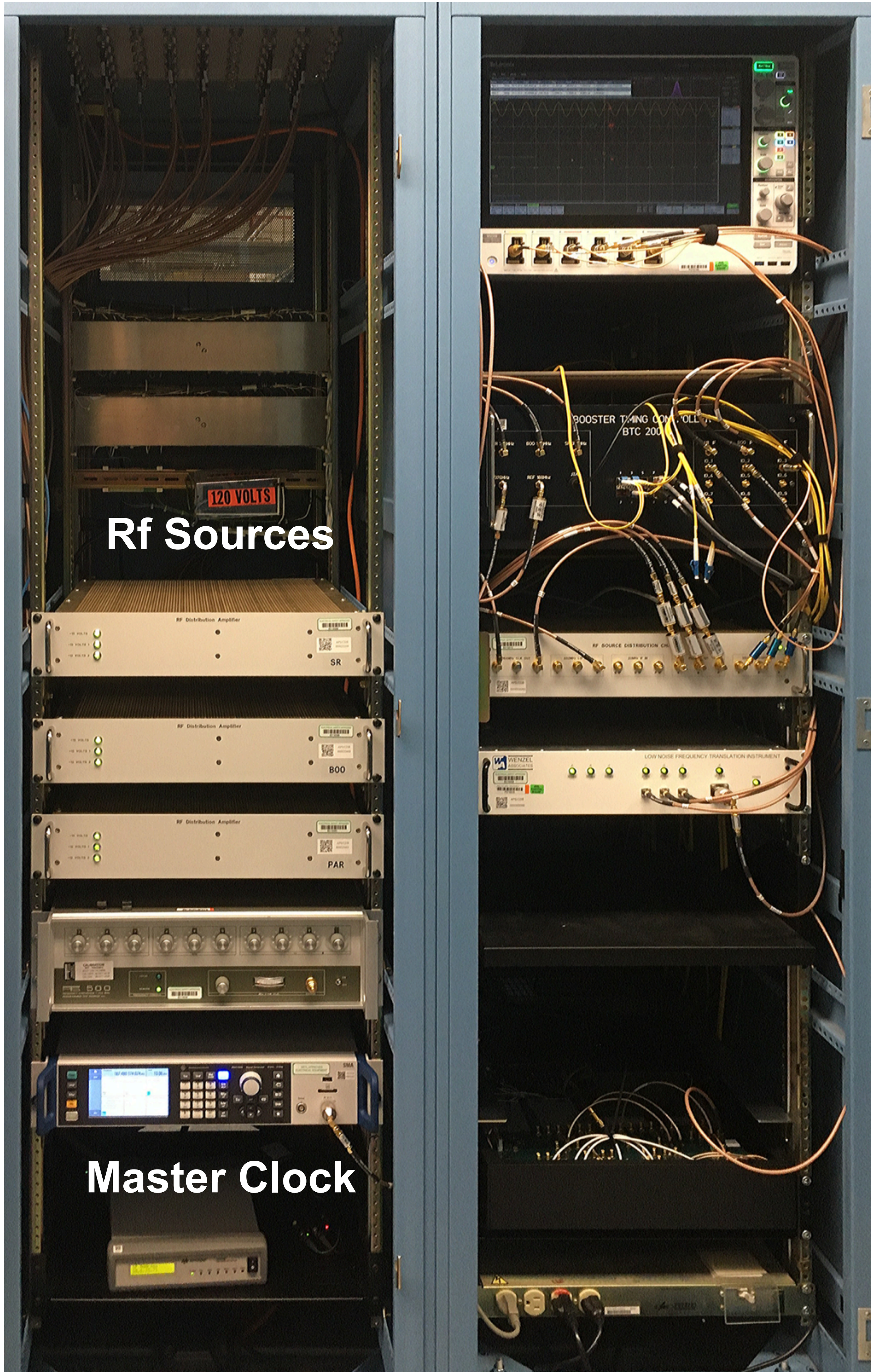
- 48-bit DSSs with 16-bit ADCs are being used to generate references for SR, Booster and PAR
- all in BTC200

T. Berenc









<-- BTC

<-- Rf converters

Rf --> distribution

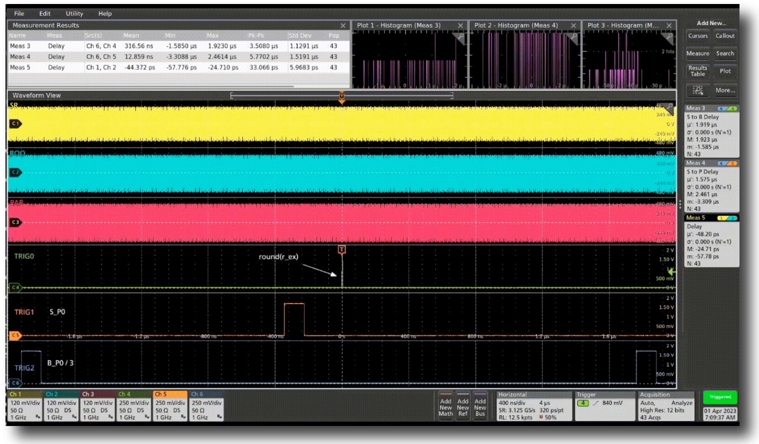
Diagnostics

- IETS scope (3 rf waveforms plus 3 selectable triggers or other signals)
- Bunch-arrival monitor (BAM), bunch time in BTS *vs* SR rf.
- Libera Spark to monitor charge in Booster by BTC.

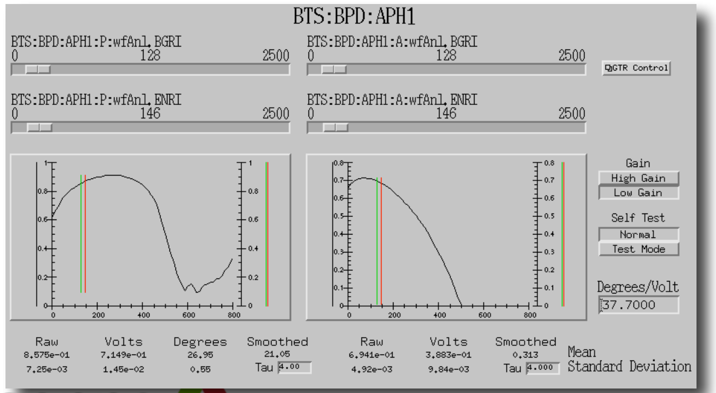
  Also useful in cross-checking time scales.
- IETS panel for setup and data presentation.
- DAQ system can log a number of BTC parameters each fill

IETS scope (6 ch)

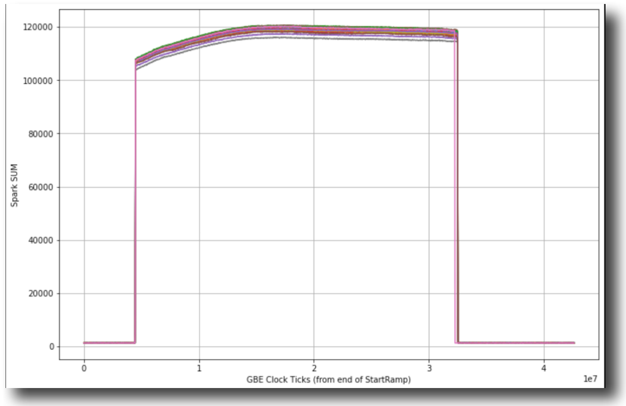
SR Rf
Boo Rf
PAR Rf



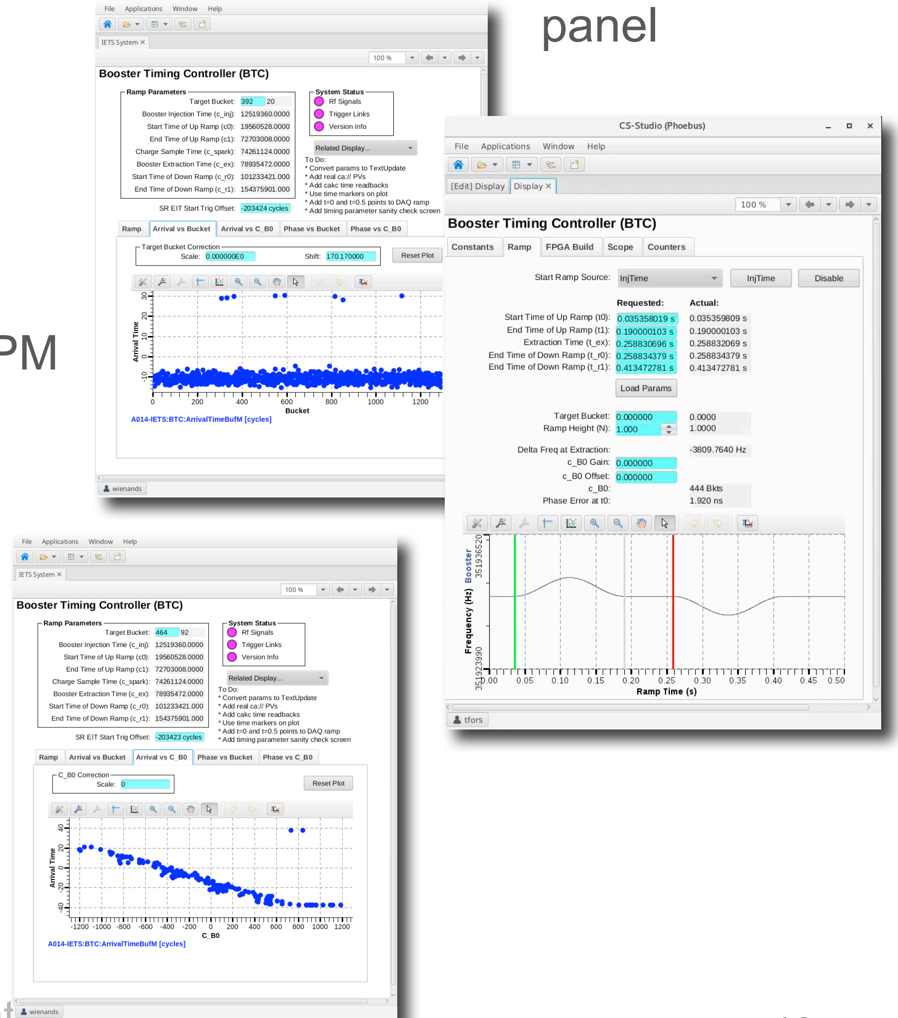
BAM waveforms



Spark Sum data from Booster BPM



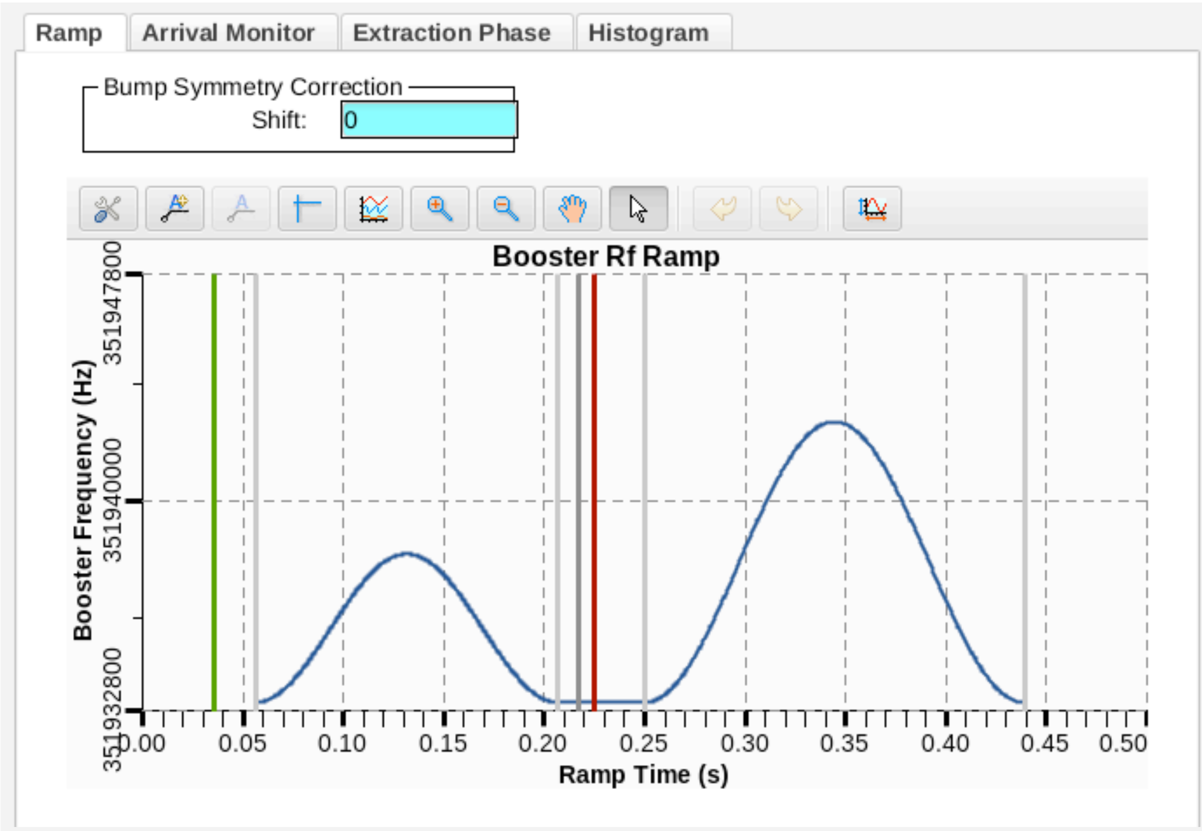
IETS Diags panel

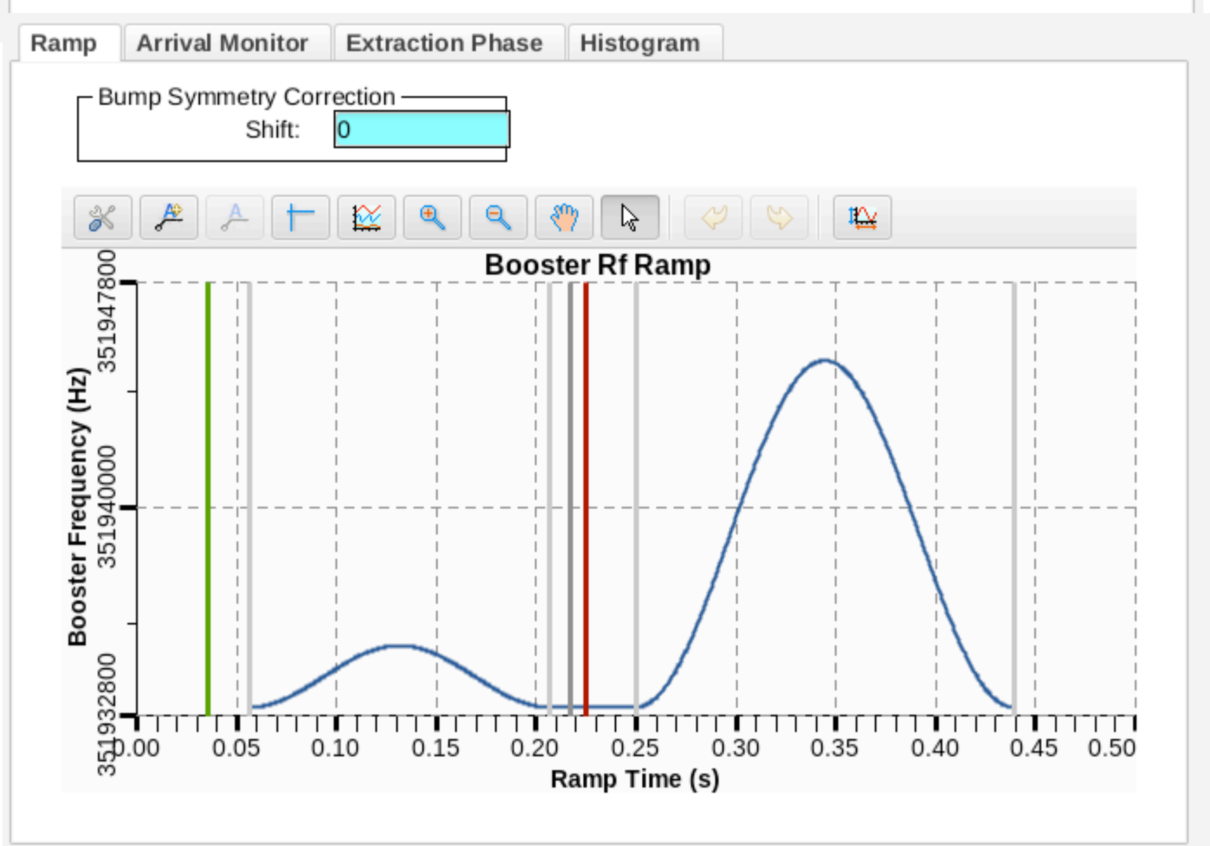


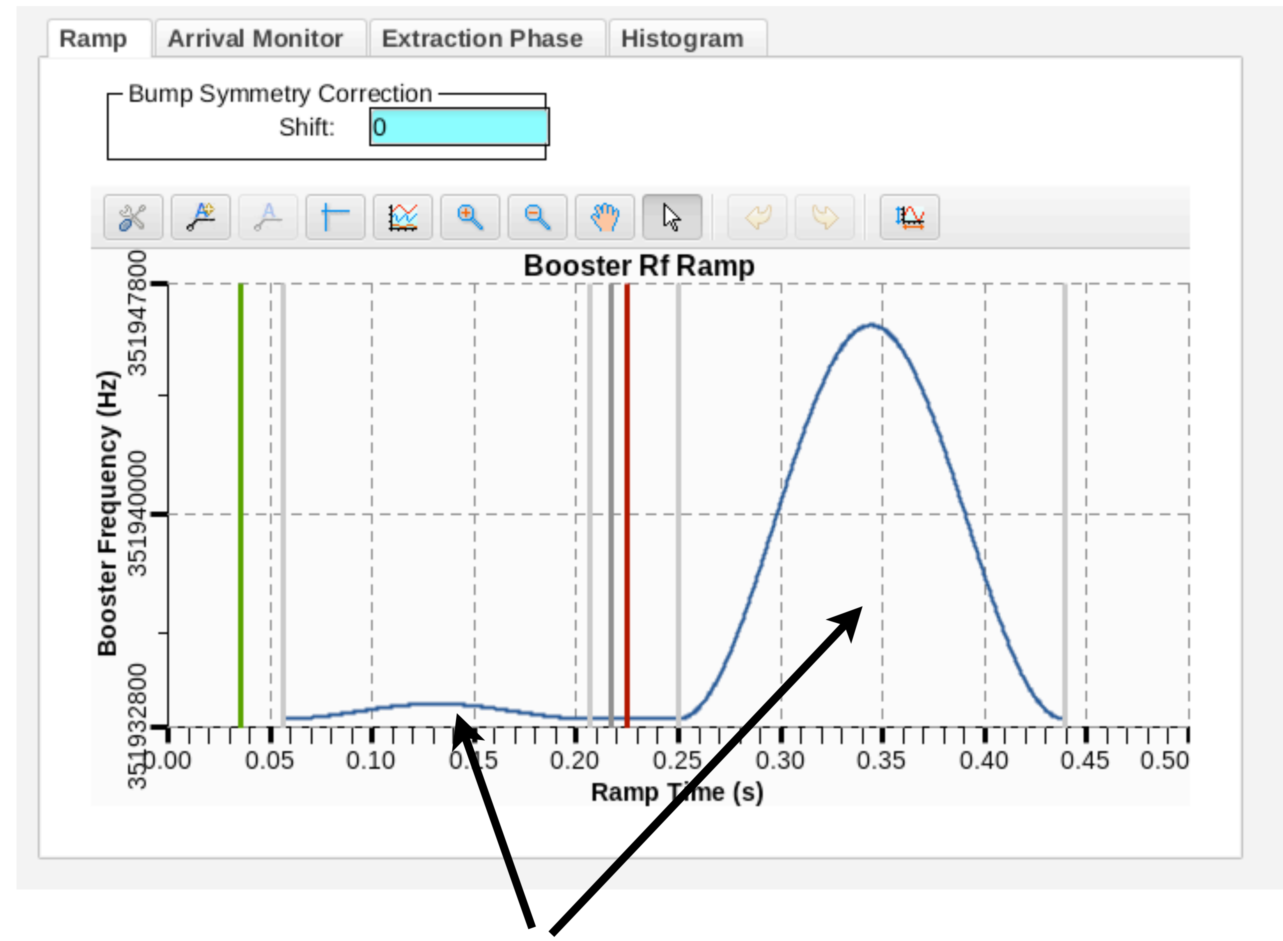
System tests & Performance

- System tests using the prototype and temporary RS-422 links quickly showed that the system was able to meet the requirements: < 50 ps jitter and random access to all sr buckets.
- A persistent issue experienced was the occasional bad shot due to Booster skipping a turn. This was eventually tracked down to synchronization issues between the three clock domains the BTS has to work in.

Live Display of Frequency Program

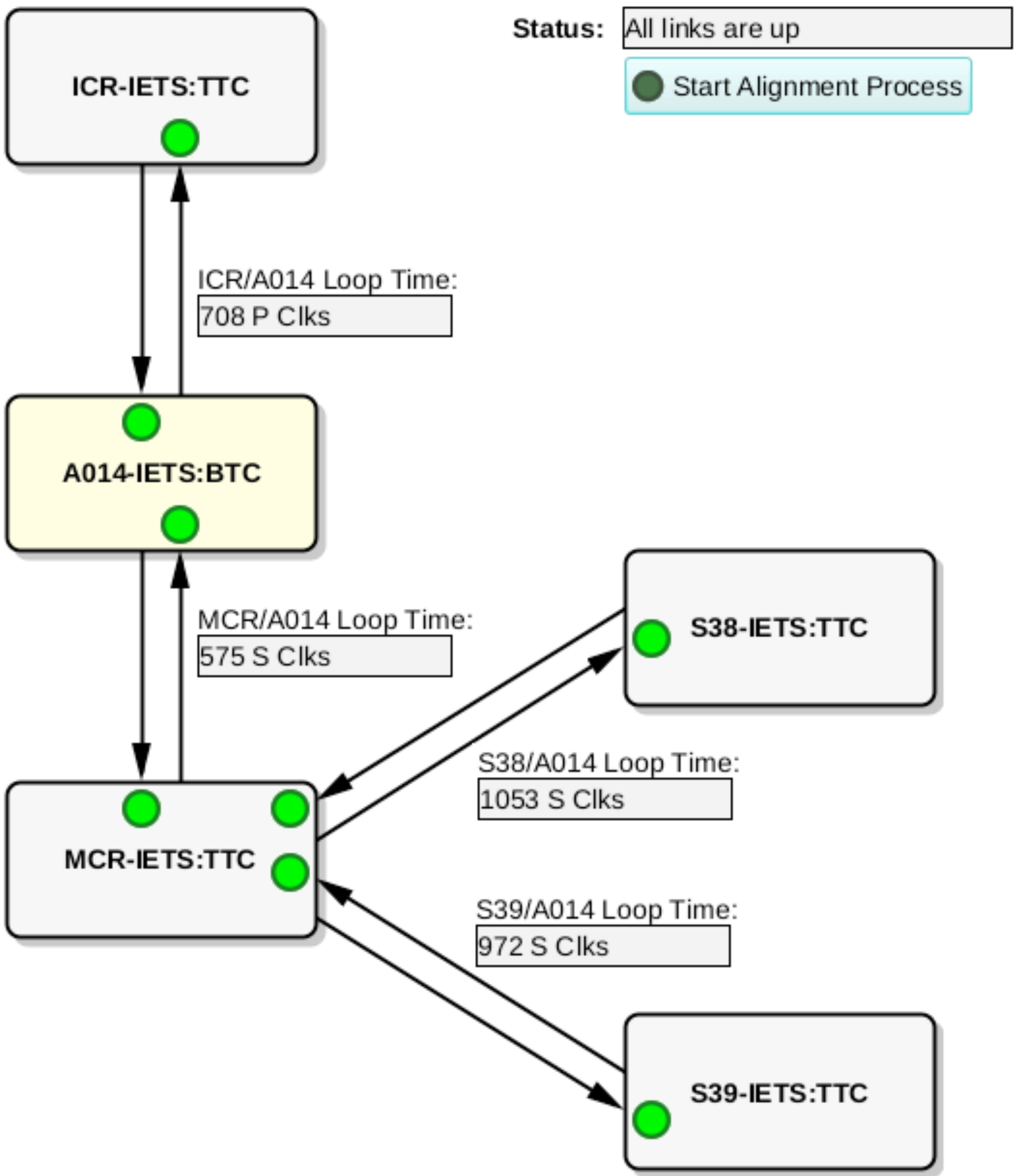


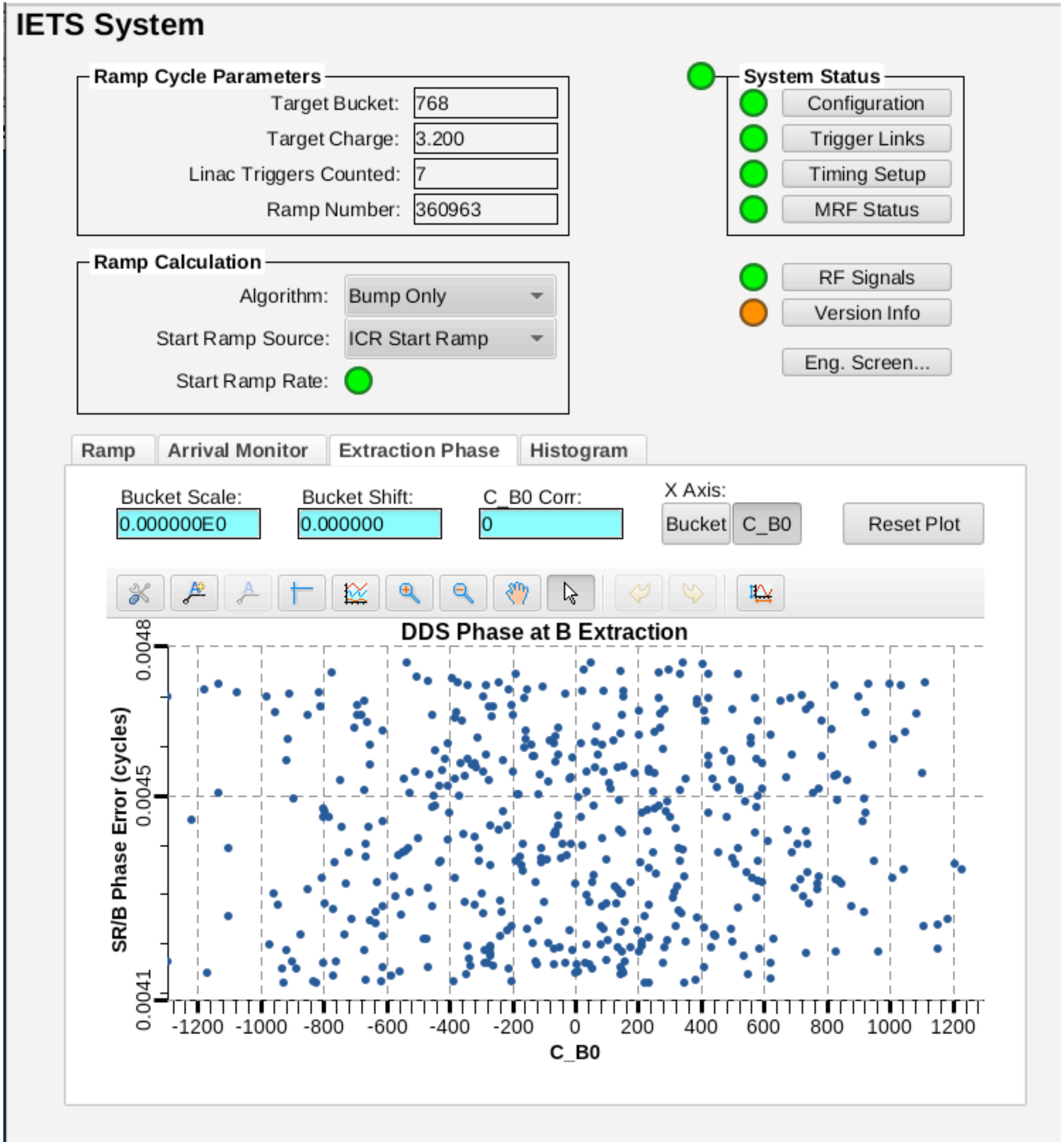




Total area: 1 Booster turn

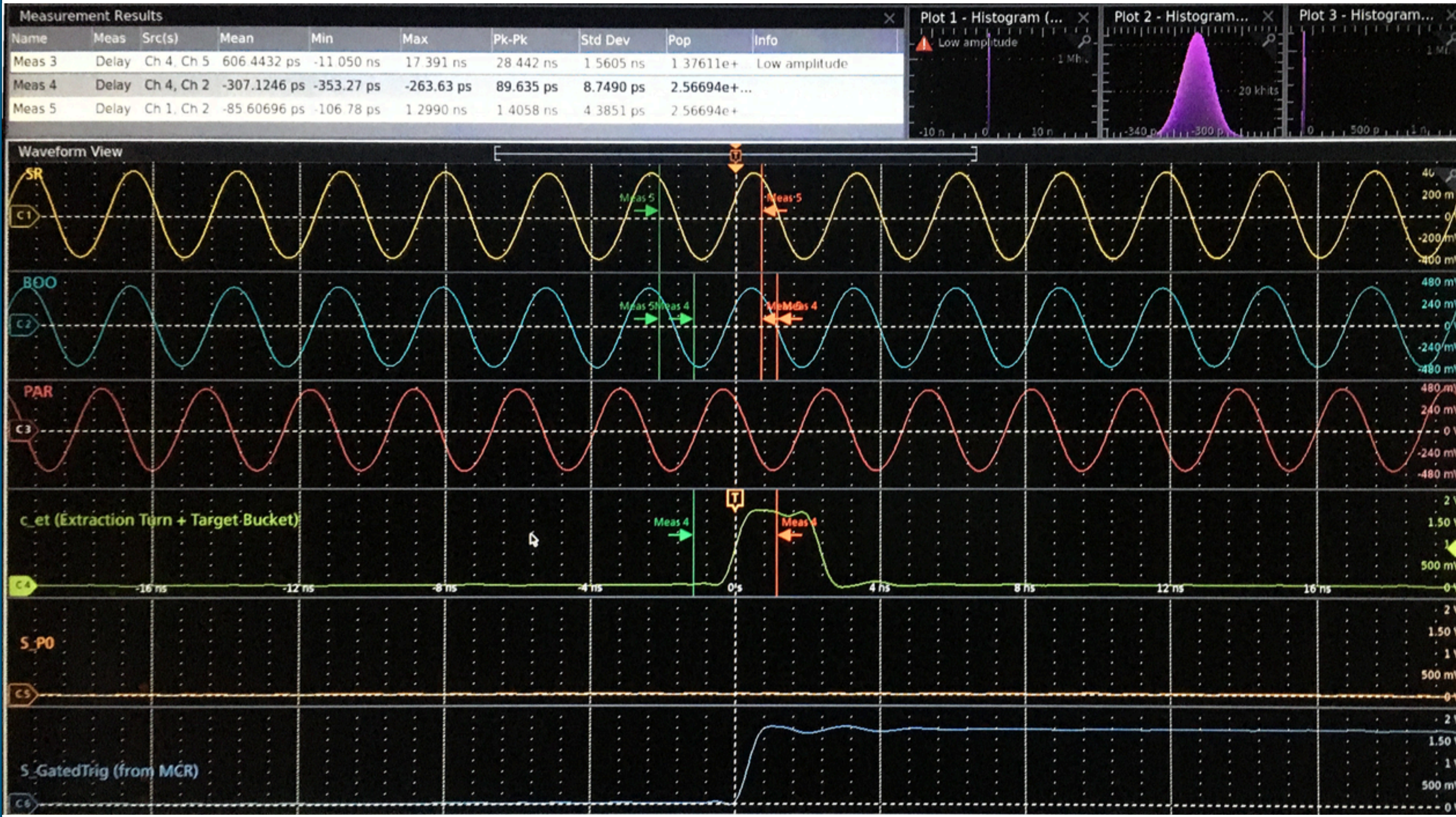
Trigger Links




IETS System
Ramp Cycle Parameters
Target Bucket: 768
Target Charge: 3.200
Linac Triggers Counted: 7
Ramp Number: 360963
System Status
Configuration
Trigger Links
Timing Setup
MRF Status
Ramp Calculation
Algorithm: Bump Only
Start Ramp Source: ICR Start Ramp
Start Ramp Rate:
RF Signals
Version Info
Eng. Screen...
Ramp
Arrival Monitor
Extraction Phase
Histogram
Bucket Scale: 0.000000E0
Bucket Shift: 0.000000
C_B0 Corr: 0
X Axis:
Bucket
C_B0
Reset Plot
DDS Phase at B Extraction
SR/B Phase Error (cycles)
0.0048
0.0045
0.0041
-1200 -1000 -800 -600 -400 -200 0 200 400 600 800 1000 1200
C_B0

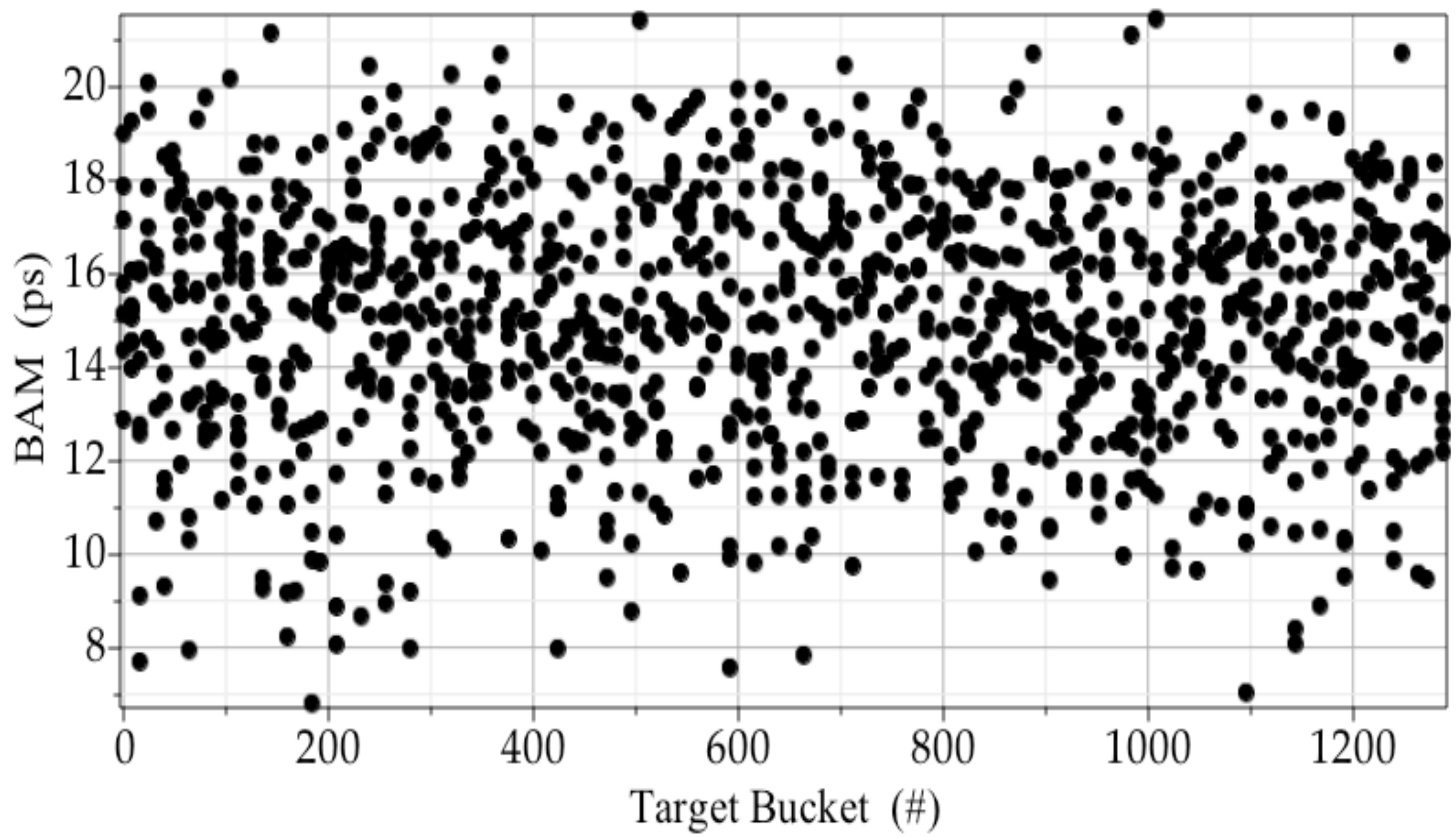
IETS Scope

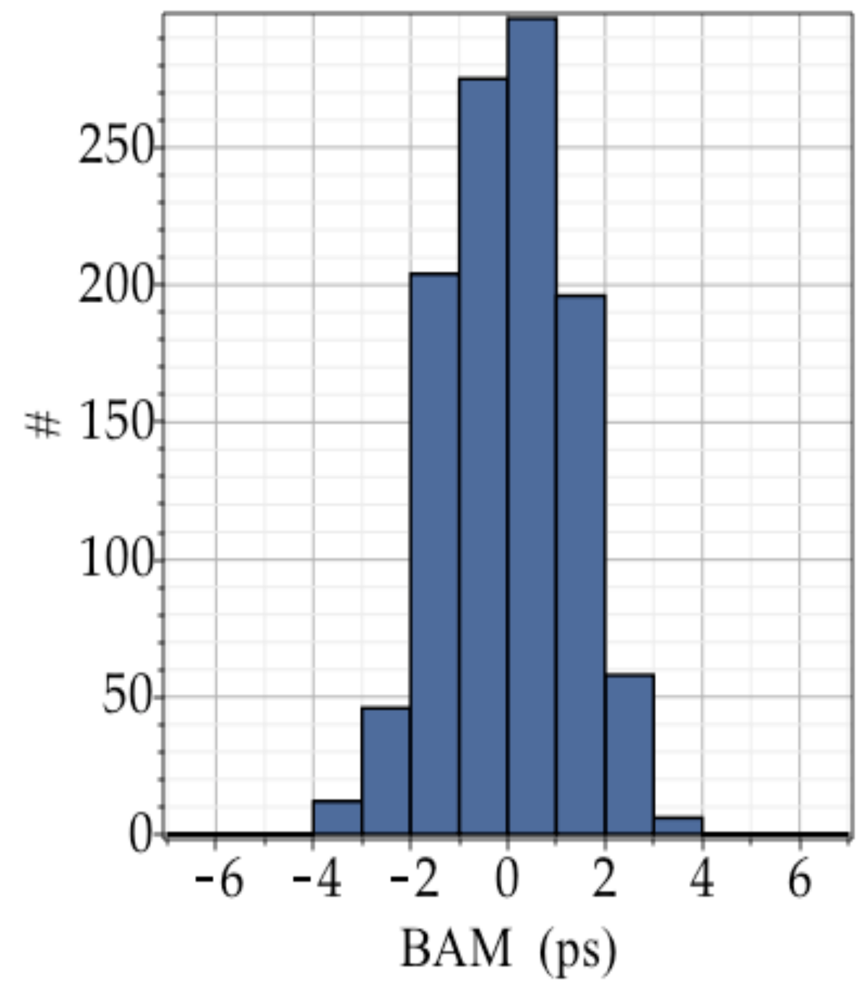
Booster rf phase against Extraction time (long-term trace): σ = 8.75 ps.



Bunch Arrival Monitor

- Extracted bunch time vs SR rf.
  - should not vary with targeted sr bucket

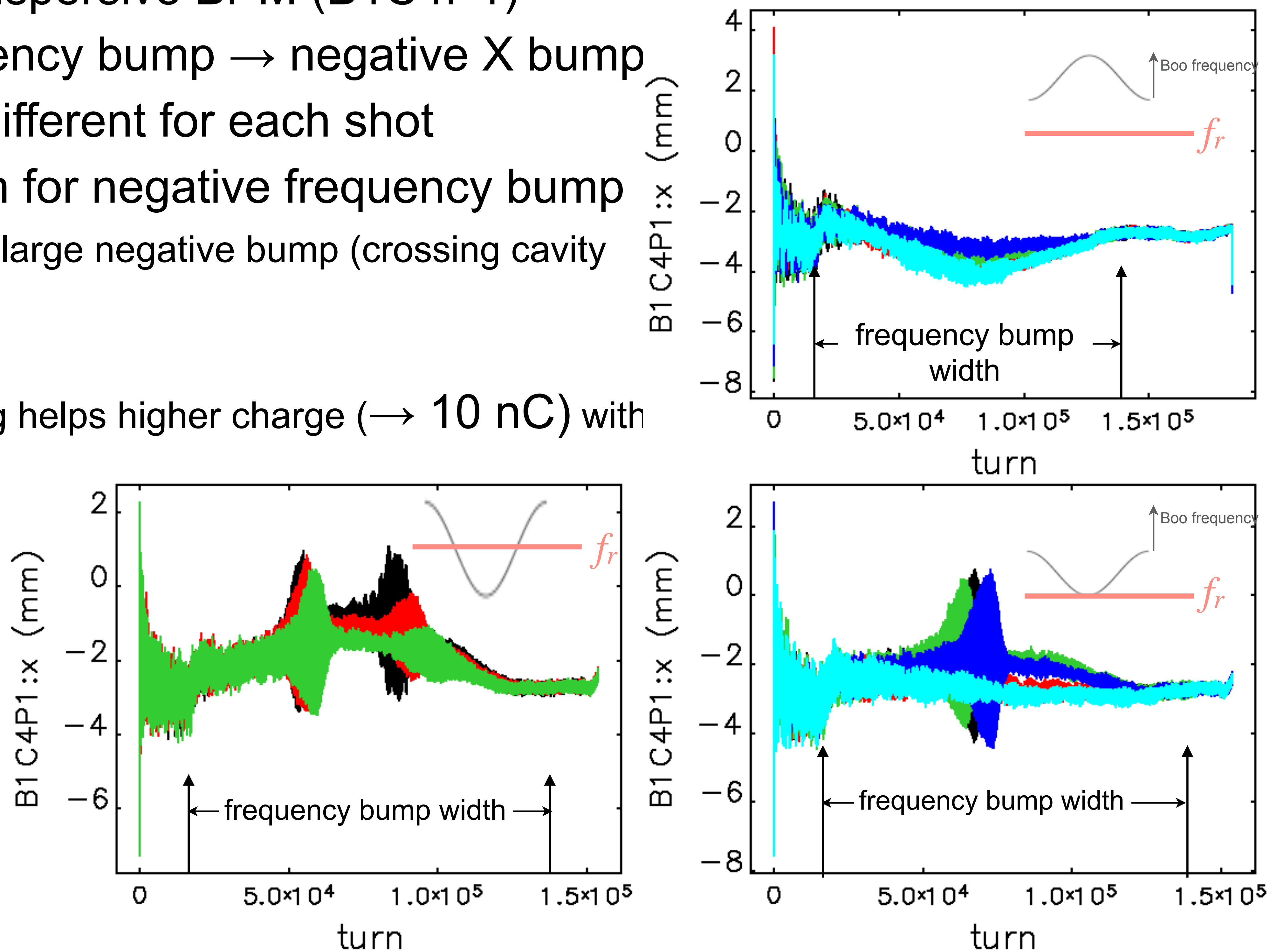




  - rms spread ≈ 2.6 ps. Well within performance spec. of 50 ps.
    - no variation with target bucket => targeting algorithm works!
  - rms Trigger jitter ≈ 17 ps (after DG645 delay unit) against sr turn clock

Varying Targeting Bumps (Calvey, Harkay, Fors, UW)

- X position in dispersive BPM (B1C4P1)
- Positive frequency bump → negative X bump
- Bump height different for each shot
- Instability seen for negative frequency bump
  - See it twice for large negative bump (crossing cavity res.)
  - No beam loss
  - Larger detuning helps higher charge (→ 10 nC) with ramp



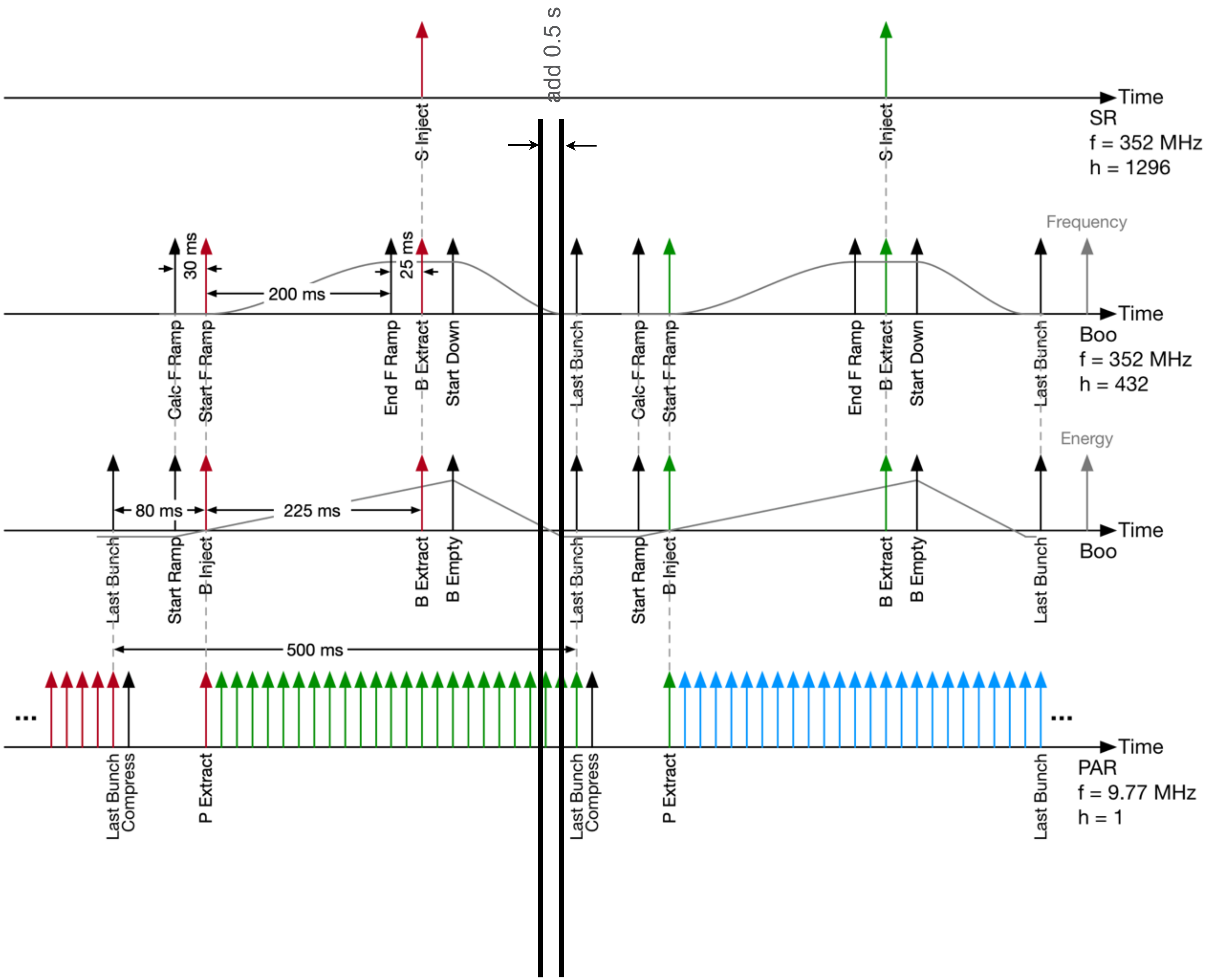
Summary

- IETS allows Booster and sr rf to decoupled from each other
- The necessary program for the Booster rf achieves accurate targeting with negligible error.
- Ramping the Booster rf to extract further off momentum has been tested and works, but has limited effectiveness without the high-power coupler for the rf cavities (descoped from APS-U).
- IETS is largely transparent to operation.

Backup Slides

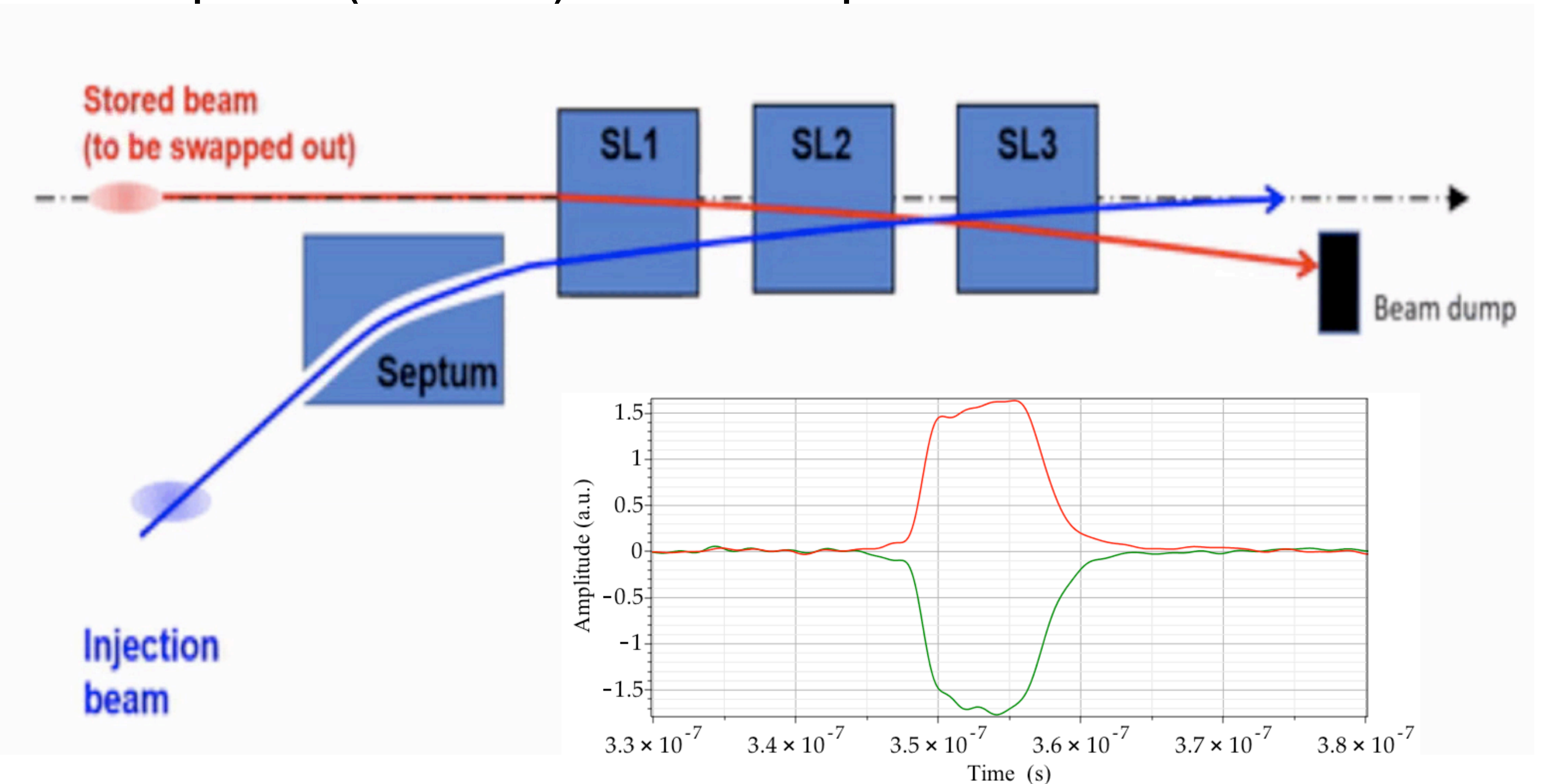
Timing diagram (APS-U)

F. Lenkszus, UW, T. Fors



Swap-out Injection

- On-axis injection
- Existing stored bunch will be kicked out.
- Short-pulse (≈ 10 ns) kickers to pick out individual bunches.



SR Rf Noise Spectrum

- Yellow: R&S SMA100B; blue: PTS500
  - need to understand origin of the lines (mostly *not* 60-Hz harmonics)