Coherent Electron Cooling: Timing and Synchronization

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Coherent Electron Cooling Proof-of-Principle (CeC PoP) is an experimental accelerator system currently commissioned at Brookhaven National Laboratory (BNL). The purpose is to demonstrate cooling of a single hadron bunch circulating in the relativistic heavy ion collider (RHIC) with co-propagating electron beam. To support CeC operation, FPGA based LLRF Controllers provide system controls, monitoring, RF references and instrumentation timing signals. Synchronization between the Laser source, photocathode electron gun, buncher and SRF accelerator cavity is achieved by broadcasting revolution frequency and resets to each LLRF controller through a high-speed fiber link. CeC is one of the essential techniques being studied for high energy strong hadron cooling, to increase the integrated luminosity goal of the future Electron-Ion Collider (EIC) at BNL.

CeC PoP Layout

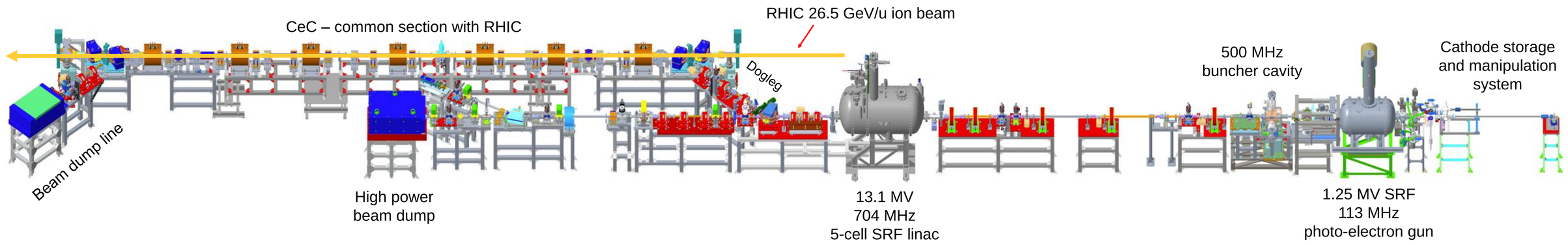

Figure 1: A Laser source shines on the cathode to produce a bunch of electrons, which passes through photocathode electron gun, buncher and SRF accelerator cavities. The electron beam is diverted through the dogleg kicker magnets to co-propagate with the RHIC hadron beam. The co-traveling ion and electron bunches interact in a cooling section consisting of a modulator, an amplifier, and a kicker [1]. In the modulator, each individual ion leaves an "imprint" in the electron bunch which is amplified in the amplifier section. Finally, in the kicker section, each ion interacts with its own amplified wake to reduced the longitudinal momentum spread of the ion bunch.

Laser Timing

Items	requirements	Beam parameter effect
Laser jitter (ps, rms)	5	2e-4 energy jitter
Laser intensity (rms)	1%, transverse uniformity needs improvement	Peak current variation
Trim PS (A, rms)	5e-5	10 um orbit jitter in common section
Gun phase (deg, rms)	< 0.1	<0.2 kV/ps energy chirp for core
Gun voltage (kV, rms)	< 0.5 kV	For less than < 1 ps separation between peak current and energy slices
buncher phase (deg, rms)	0.2	Energy jitter < 2e-4, chirp jitter < 0.2 kV/ps
buncher voltage (kV, rms)	1.4	Chirp jitter < 0.2 kV/ps

Figure 2: The laser jitter requirement is 5 ps, and the Irisiome seed laser is < 3 ps of RMS jitter

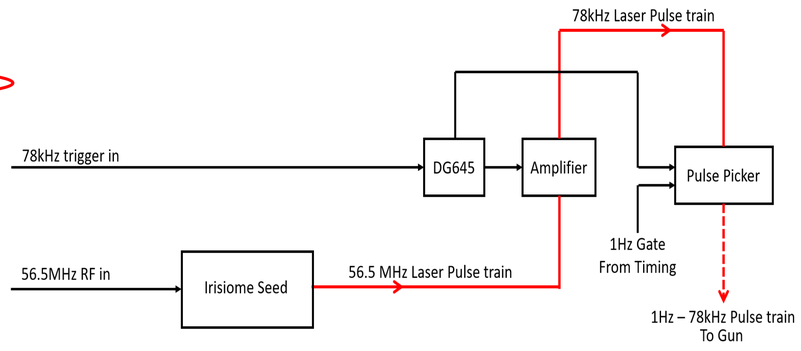

Figure 3: The Irisiome seed laser creates a pulse train from the LLRF 56 MHz signal. The 78kHz signal from LLRF acts as a trigger for the amplifier and pulse picker to select a single laser pulse from laser pulse train.

Cogging

Cogging is used in CeC to phase align multiple local Numerically Controlled Oscillators (NCOs) with a global NCO. An event from the Update Link Master (ULM) enables cogging for a long enough time to allow the phases to converge. An update event latches the global and local NCO phase every 10 µs and a scaled-down phase difference is added to phase increment. This way, the phase will slowly converge to the global NCO phase over the many clock cycles.

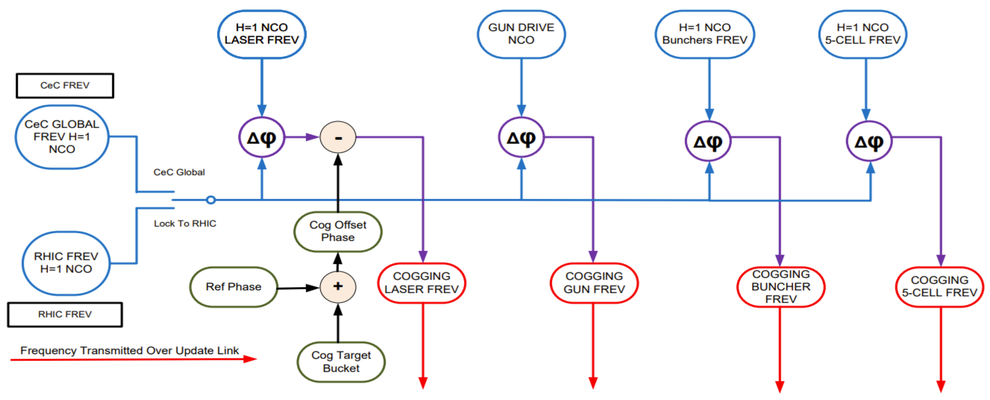

Figure 4: Cogging layout for the CeC cavities. The difference between the local and global NCO phases is added to the revolution frequency to minimize the phase difference between the NCOs.

Synchronization with RHIC beam

Figure 7: Beam Position Monitor (BPM) signal: No overlap between hadron and electron beam (50 ns, 10 mV per division)

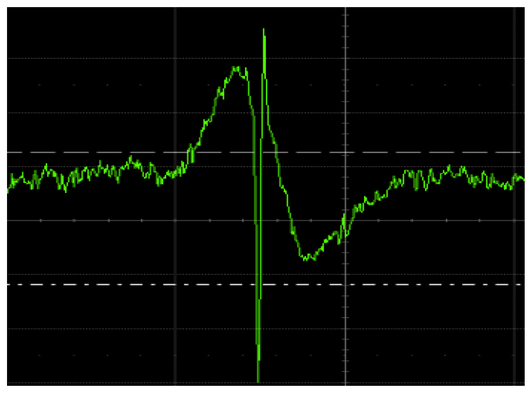

Figure 8: BPM signal: Overlap between hadron and electron beam (20 ns, 2 mV per division)

Synchronization is achieved by cogging CeC NCOs to that of RHIC. When co-propagating electron and hadron bunches, the electrons are placed in the middle of a hadron bunch for cooling as seen in Figure 8. During experimental tests, the electron bunch is placed in the RHIC abort gap to limit the interference with RHIC operations.

LLRF Controller

LLRF Controller is a stand-alone configurable, modular, hardware/software platform that contains a carrier and daughterboard [2].

- Carrier Board: Control system interface, daughter host platform, communication hub, timing, data acquisition management, power monitor.
- Daughter Module: Provide system specific functionality (ADCs, DACs, DSP, Motor Controller).

The Update Link is a multi-gigabit serial link that provides a deterministic data path to broadcast information to multiple local LLRF controllers [3].

- Downstream deterministic (i.e. fixed latency) 2 Gb/s serial link distributing encoded timing and data.
- Key to ease of system integration, flexibility, scaling and synchronization.
- A common 100 MHz system clock for all LLRF systems is crucial in for a repeatable, deterministic relationship between all parts of a distributed LLRF system.

Clocking/Sampling:

- RF asynchronous fixed frequency is used as the primary system clock and signal processing.
- Can be sourced from an external clock to provide RF synchronous clocking used for specific applications (e.g. trigger generation for e-gun lasers).

EIC Common Hardware Platform will be the next-generation LLRF controllers to replace the current Collider-Accelerator Department (C-AD) hardware.

- Knowledge gained from C-AD controller played a significant role in the development of the Common Platform.
- Contains a custom Xilinx Zynq Ultrascale+ carrier board to interface with up to 2 application-specific daughter cards [4].

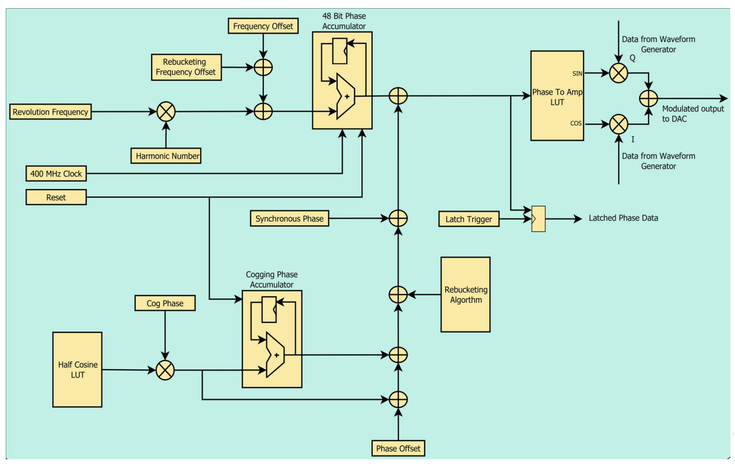

Figure 5: Block diagram of a generic LLRF controller firmware. 48-bit phase accumulator is used for direct digital synthesis. The cogging phase accumulator provides smooth phase shifts for injection phase cogging.

Figure 6: LLRF Controller with carrier and daughterboards (top), EIC Common Hardware Platform (bottom)

Summary

- To prevent emittance growth during long stores of the proton beam at the future EIC, CeC can be used to provide fast cooling of the dense proton beams. It uses an electron beam to both "measure" the positions of protons within the bunch, and then apply energy kicks which reduces their longitudinal and transverse actions.
- The C-AD LLRF Platform used for CeC Experiment proved to be extremely flexible, readily scalable, and high performance. Design of EIC Common Platform took into account the lessons learned from the C-AD LLRF Platform.
- A common distributed 100 MHz system clock and the Update Link is crucial to ensure all LLRF systems are deterministic. Cogging makes use of the Update Link to synchronize the LLRF controllers.

References

[1] V. N. Litvinenko et al, "Coherent Electron Cooling Experiment at RHIC: Status and Plans," proceedings of 12th Workshop on Beam Cooling and Related Topics, Russia

[2] K. Smith et al, "BNL Lab Talk: Recent Applications and Performance of the RHIC LLRF Platform Across the Collider-Accelerator Complex," proceedings of LLRF Workshop 2013, California

[3] T. Hayes et al, "A Deterministic, Gigabit Serial Timing, Synchronization and Data Link for the RHIC LLRF," proceedings of PAC 2011, New York

[4] G. Narayan et al, "Electron-Ion Collider Common Platform System Architecture," proceedings of LLRF Workshop 2022, Switzerland

Electron-Ion Collider

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