

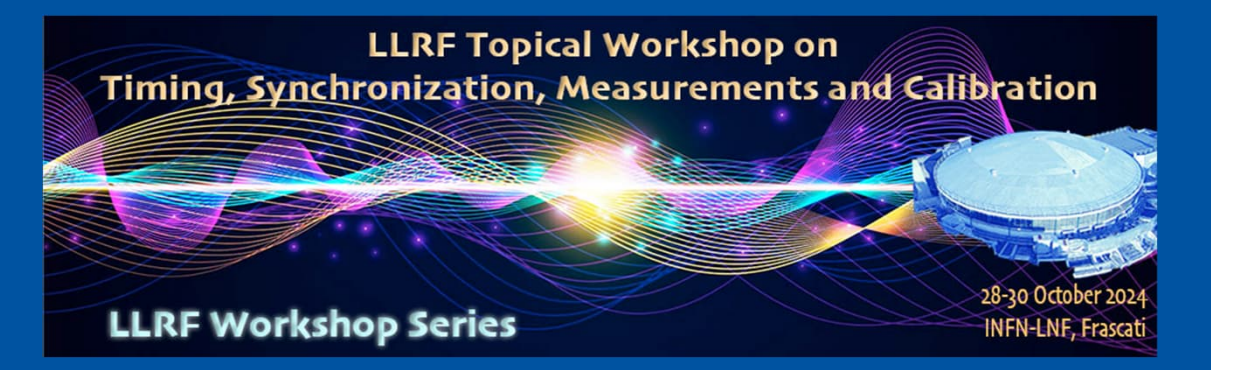


# HL-LHC RF Distribution over White-Rabbit

## The WR2RF and eRTM modules



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### Introduction

The Hi-luminosity Large Hadron Synchrotron (HL-LHC) is an upgrade of the LHC which aims to increase the instantaneous luminosity by 5 to 7.5-fold with respect to the LHC nominal value. During LS3 (2026-2028), Super-conducting crab-cavities will be installed around the ATLAS (point 1) and CMS (point 5) experiments which are located several kilometres away from the existing main RF system (point 4). The RF signal distribution for RF users (Experiments, Beam-Instrumentation) will also be upgraded, with use of WR2RF modules on the RF user side, and with an upgrade of the LHC Beam-Control for a new White-Rabbit (WR) RF-train master (frequency program). The crab-cavities LLRF and WR2RF modules will be synchronized to the main RF system through a White-Rabbit network and re-constructing the frequency program locally.

An upgrade of the LHC machine timing distribution (GMT) over WR is also on-going, a single WR architecture will be deployed and shared for both timing distribution and RF distribution.

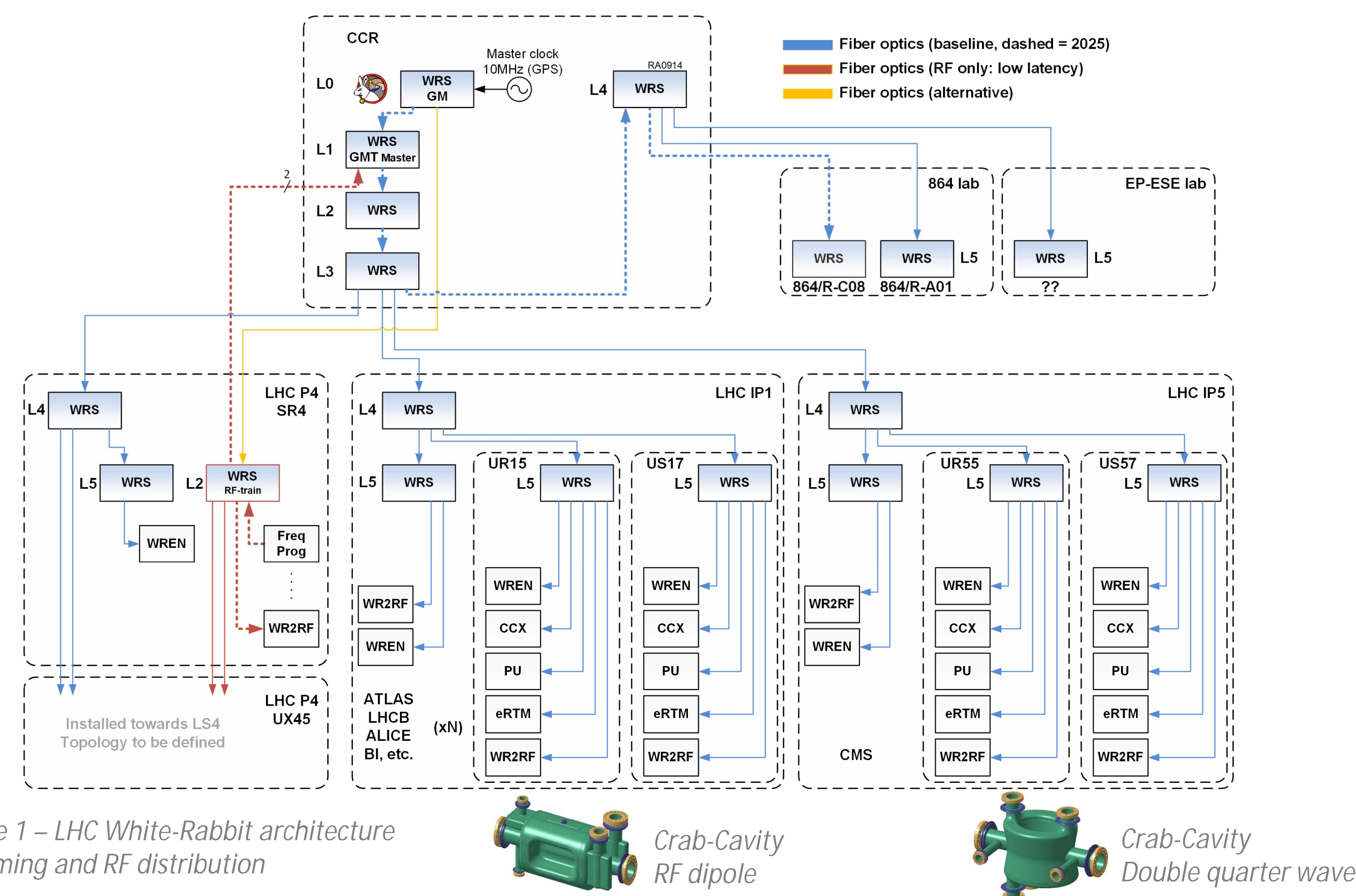
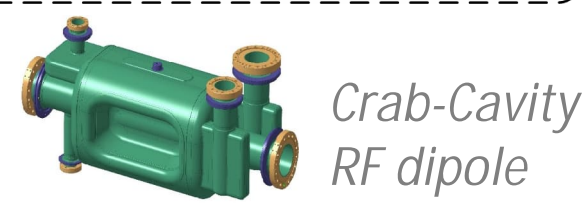


Figure 1 - LHC White-Rabbit architecture for timing and RF distribution



### WR2RF module

The WR2RF module is a standard VME A24D16 module. It receives the instantaneous RF frequency from the RF-train (FTW, h=1) over White-Rabbit and re-constructs the following analog RF signals:

- **FRF** - Main accelerating cavity frequency (~200MHz for SPS, ~400MHz for LHC)
- **Orbit clock** - (Revolution frequency  $F_{REV}$ , short 1ns pulse)
- **Bunch Clock** - (40MHz for 25ns bunch spacing)

A dual PLL locks a low noise 100MHz OCXO and a 1GHz VCXO (surface acoustic wave Oscillator) on the WR base clock frequency of 62.5MHz. The first PLL (BW~10kHz) locks the VCXO onto the OCXO with a phase detector frequency at 100MHz. The second digital PLL (BW~10Hz) in the FPGA, locks the divided version of the 1GHz oscillator onto the WR base clock.

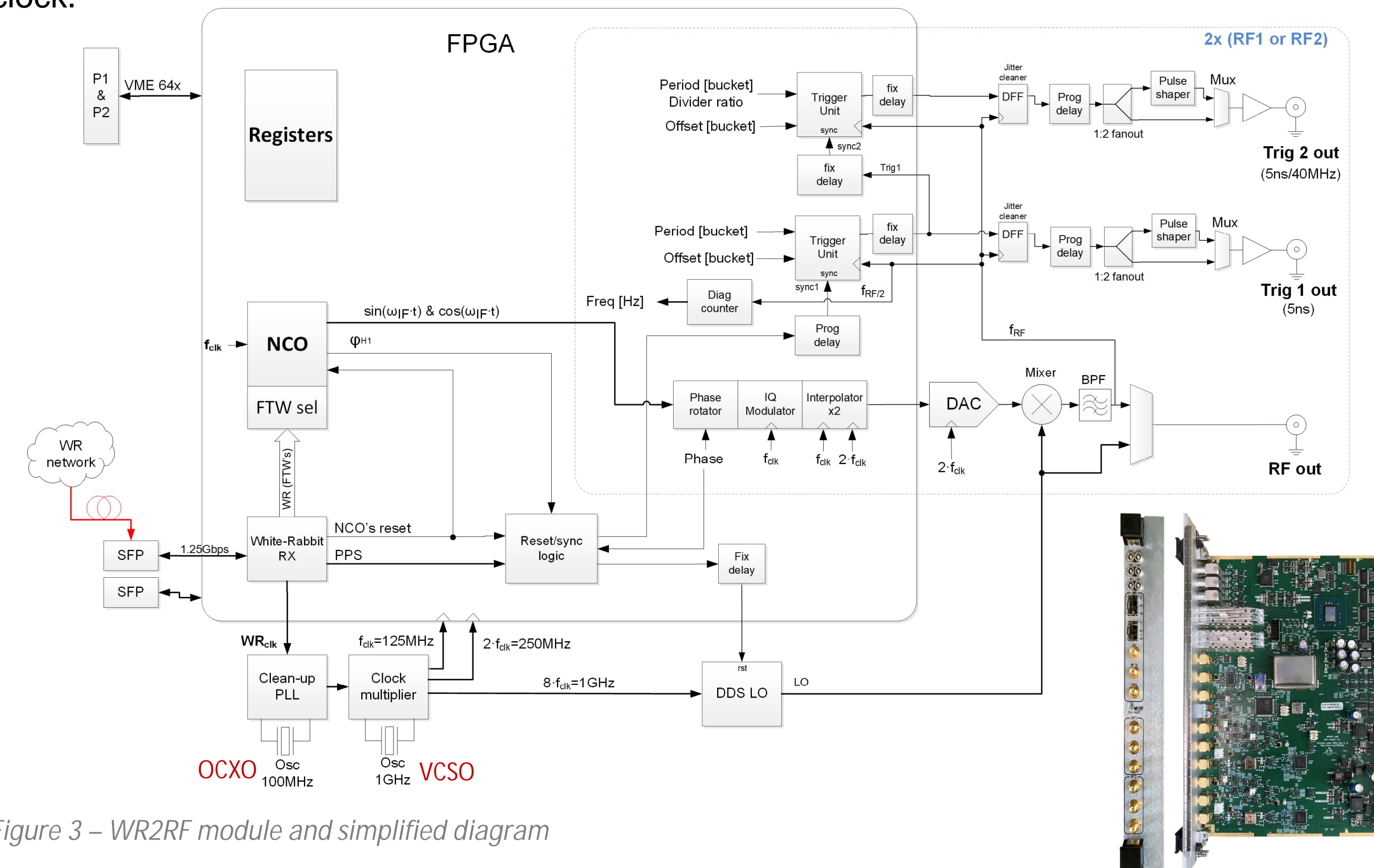


Figure 3 - WR2RF module and simplified diagram

### eRTM module

The crab-cavity LLRF Controller electronics uses fixed frequency sampling and processing clocks which are reconstructed locally in the eRTM module from the WR data stream and low noise PLL's. The challenging RF noise requirement to limit the total Emittance Growth Rate (EGR) below 2%/h for the crab-cavity, calls for a single-sided phase noise plateau of  $5 \cdot 10^{-3} \frac{\mu rad^2}{Hz}$  in the cavity, that is  $\mathcal{L}(f) = -143 \frac{dBc}{Hz}$  from 3kHz to 136kHz [1].

An eRTM module [2] was developed for the SPS LLRF system and includes the generation and distribution of the clocks and LO from the WR link. To achieve lower clock and LO phase noise (PN), an upgrade of the eRTM15 is planned together with a new development of an external Master reference module (Master REF).

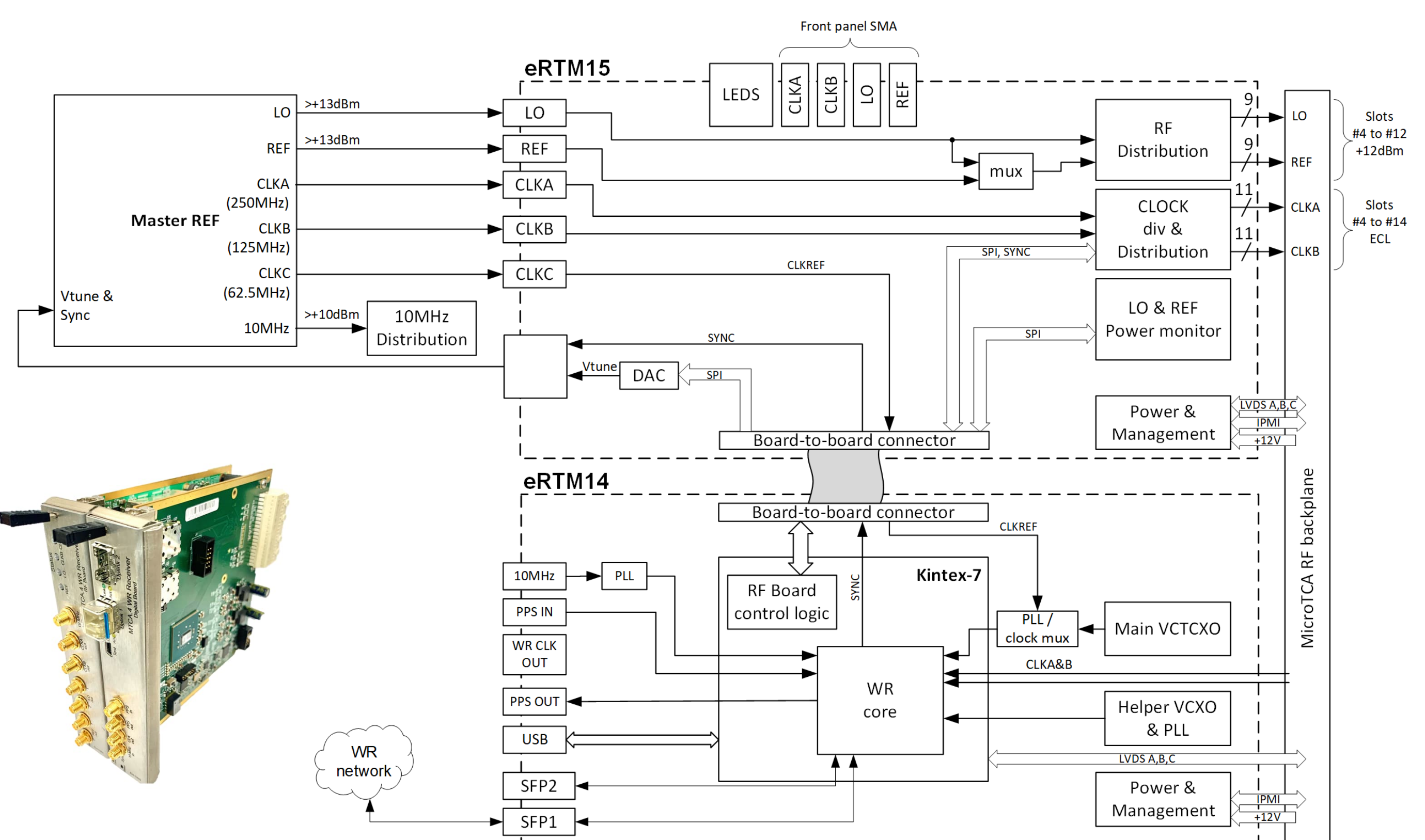


Figure 2 - Block diagram of the LHC Crab-cavity eRTM and Master REF modules

The eRTM module is made of two PCB's: the eRTM14 and eRTM15. The eRTM14 controls the Master REF module and locks the 62.5MHz generated clock (CLKC) onto the WR clock inside the FPGA. The eRTM15 distributes the generated clocks and LO in the MTCA shelf.

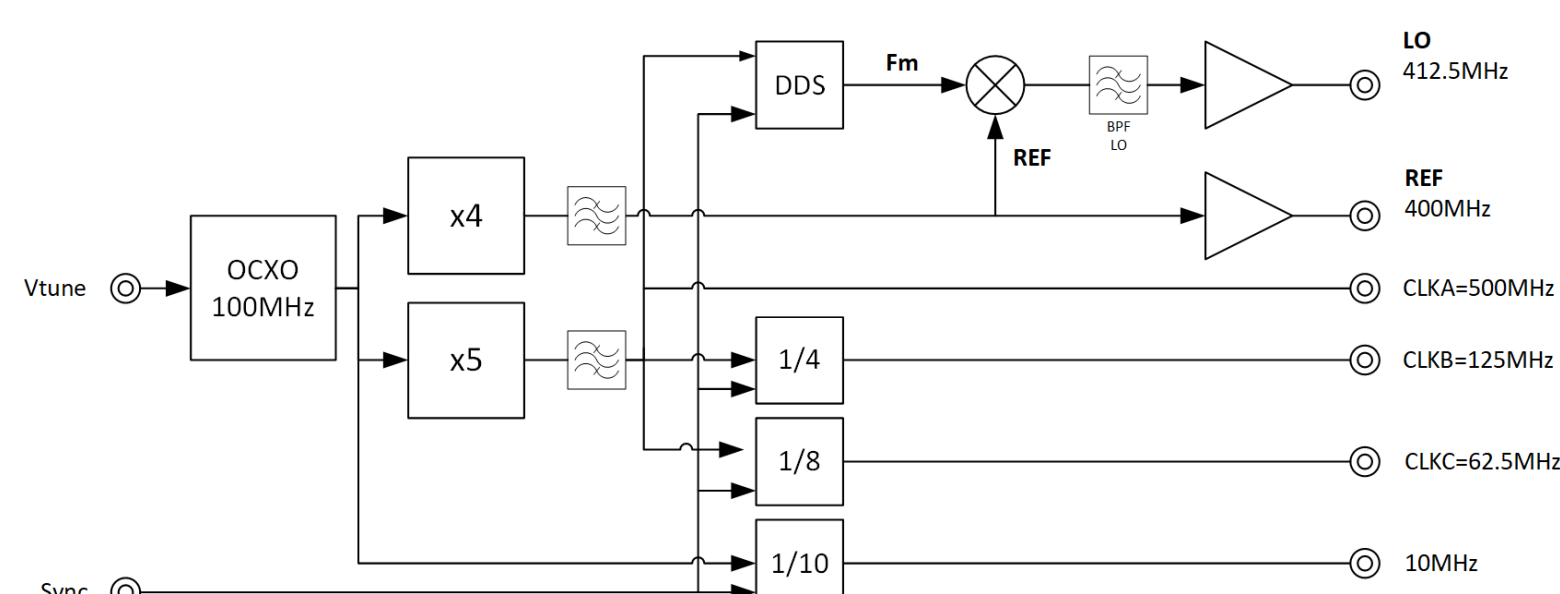


Figure 3 - Master Reference module block diagram

### Results

The WR2RF module has undergone an extensive test campaign [3] to evaluate both its phase noise (PN) performance and its phase reproducibility. The PN requirements are based on the current LHC RF noise of the main accelerating cavities (dominated by the LO of the RF noise receiver, orange curve).

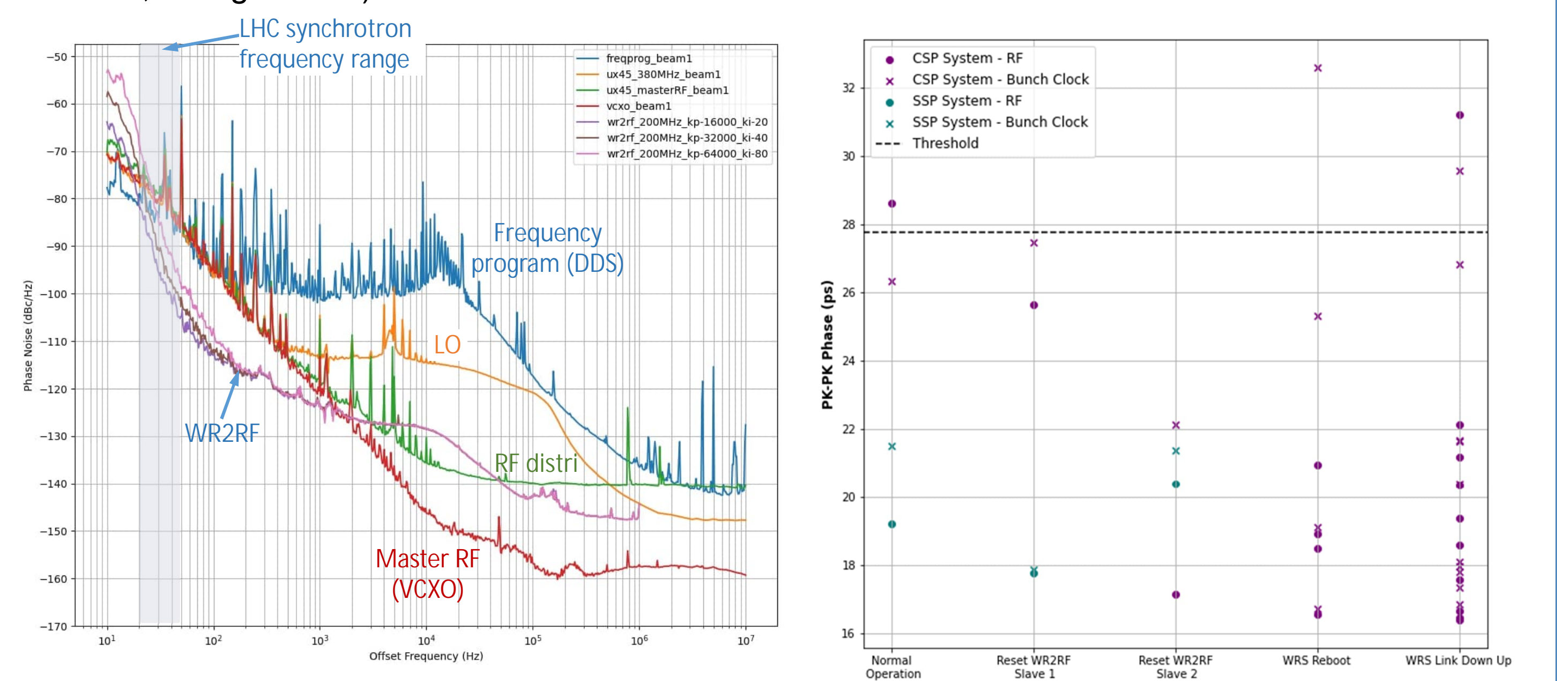


Figure 4 (left) - WR2RF phase noise (200MHz output normalized to 400MHz) and LHC RF clocks distribution phase noise of beam 1 (right) - WR2RF Phase reproducibility between two slaves (right), one marker per measurement "run" with one measurement being the phase difference averaged over 12.5ms window. (Normal operation: 1000 meas./run, Reset SSP: 250 meas./run, Reset CSP: 100 meas./run, Reboot & link down/up: 100 meas./run.)

With optimized PLL settings ( $kp=16000$ ,  $ki=20$ ), the WR2RF PN is lower from the synchrotron frequency (20 to 50Hz) except in the middle region (3kHz to 40kHz) for the RF distribution but always lower than the LHC RF receiver (LO).

Figure 5 (right), shows the WR2RF phase reproducibility (<33ps pk-pk) of the RF and bunch clocks with two different Proof of Concept (PoC) WR architectures. The Single Switch PoC (SSP) with two WR2RF slaves connected to the same WR switch (WRS) shows better performances (~22ps pk-pk) than the Cascaded Switch PoC (CSP). The CSP reproduces the planned LHC WR architectures (6 layers of WRS) and shows the phase difference between the master WR2RF (LHC point 4) on layer 2 and a slave WR2RF connected on layer 5 (RF user).

