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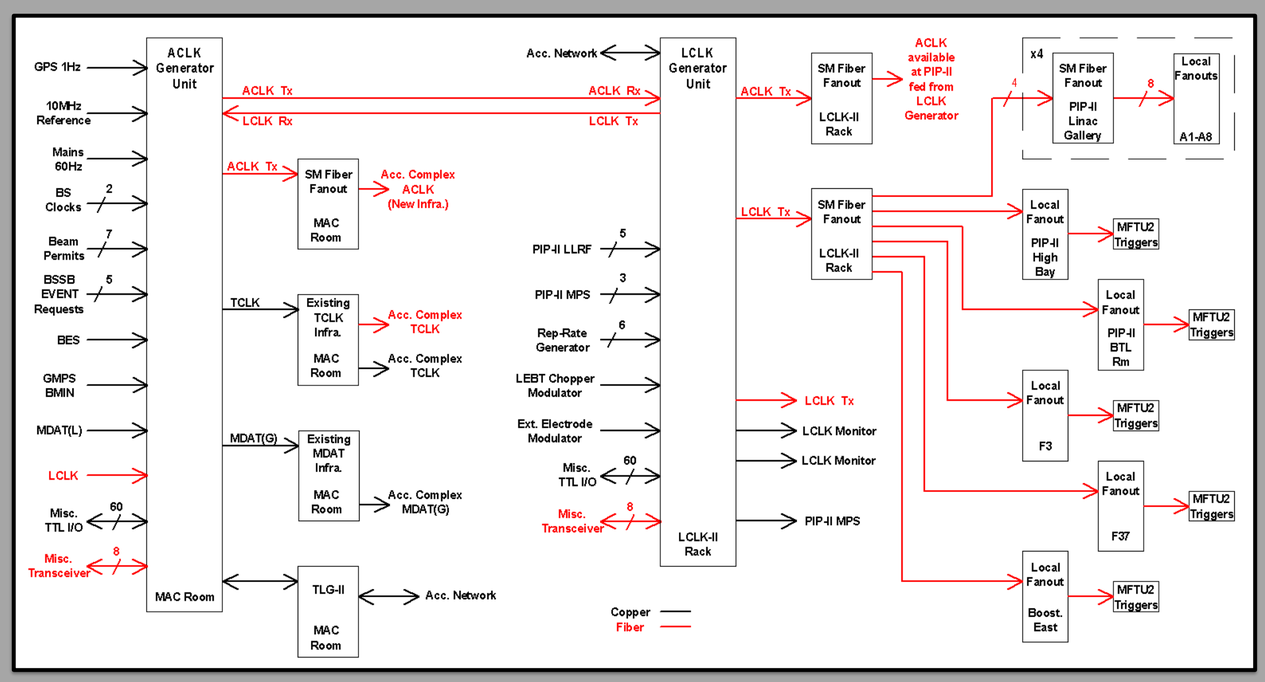
Proton Improvement Plan II (PIP-II) Clock and Timing

Introduction

The PIP-II timing system is planned to be a two-part system consisting of a global timing system (referred to as ACLK) that provides high level, event-based timing for the whole Fermilab accelerator complex while the second part is a RF synchronized clock system unique to the PIP-II Linac itself (referred to as LCLK). The ACLK System will make use of an external 10 MHz GPS based signal source as a reference for its 650 MHz phase lock as it is the reference frequency for the TCLK output of the system (needed to support legacy hardware around complex). The LCLK System will use a PIP-II Linac RF reference (162.5 MHz) from the Linac LLRF system to allow beam synchronized event placement. Both the ACLK and LCLK systems will have a clock output with a data frame of 16 event bits + 32 data bits with frames broadcast at 650 MHz, phase locked to the 10MHz reference in the case of ACLK and the PIP-II LLRF sourced 162.5 MHz reference in the case of LCLK.

Timing System Diagram



Frame Definitions

ACLK uses a GPS based 10 MHz source to create a 650 MHz PLL. This allows for encoding the data within consecutive 65-bit wide frames played out every 100 nS in the format as shown below.

ACLK Frame	00	MSB LSB	MSB LSB	XXXXXXXX	X	111111
65-bit	2 start bits	16-bit EVENT	32-bit Data	8-bit CRC	Parity bit	Pad bits #60-65

The 100 nS frame width corresponds to the 10 MHz source which is compatible with the creation of the existing TCLK. Currently, TCLK can not have two EVENTs closer than 1.2 uS. Therefore, if ACLK plays a TCLK compatible EVENT in frame 1, as shown below, ACLK will need to wait 11 more frames before another TCLK compatible EVENT can be played. TCLK compatible EVENTs on ACLK are defined by the lower 8 bits of the EVENT. TCLK would also be played out on a functionally equivalent TCLK output to be distributed to the rest of the Fermilab complex to maintain backwards compatibility with existing hardware.

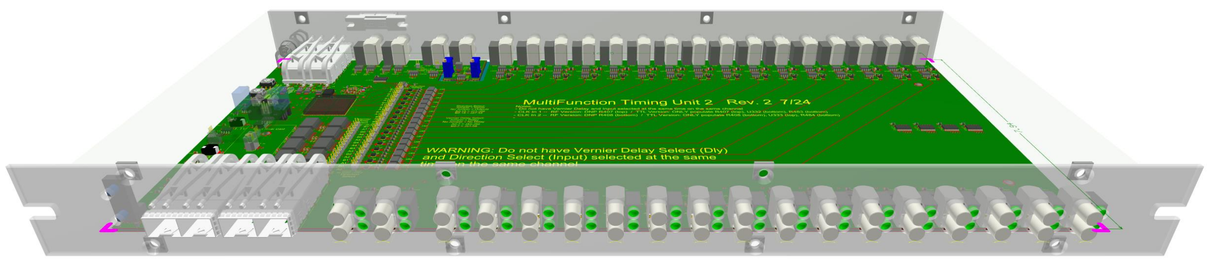
ACLK 650 MHz	Multiple ACLK frames each 100 nS wide with 65-bits each												
	1	2	3	4	5	6	7	8	9	10	11	12	1
TCLK 10 MHz	1.2 uS minimum between possible TCLK EVENTs												
	0	X	X	X	X	X	X	X	X	X	1	1	0
	Start bit	MSB	8-bit EVENT						LSB	Parity	Pad Bits		Start bit
	TCLK EVENT												Next TCLK EVENT

LCLK uses the PIP-II 162.5 MHz RF to create a 650 MHz PLL. This allows for encoding the data within consecutive 72-bit wide frames with 1 frame corresponding to 18 ticks of the 162.5 MHz RF.

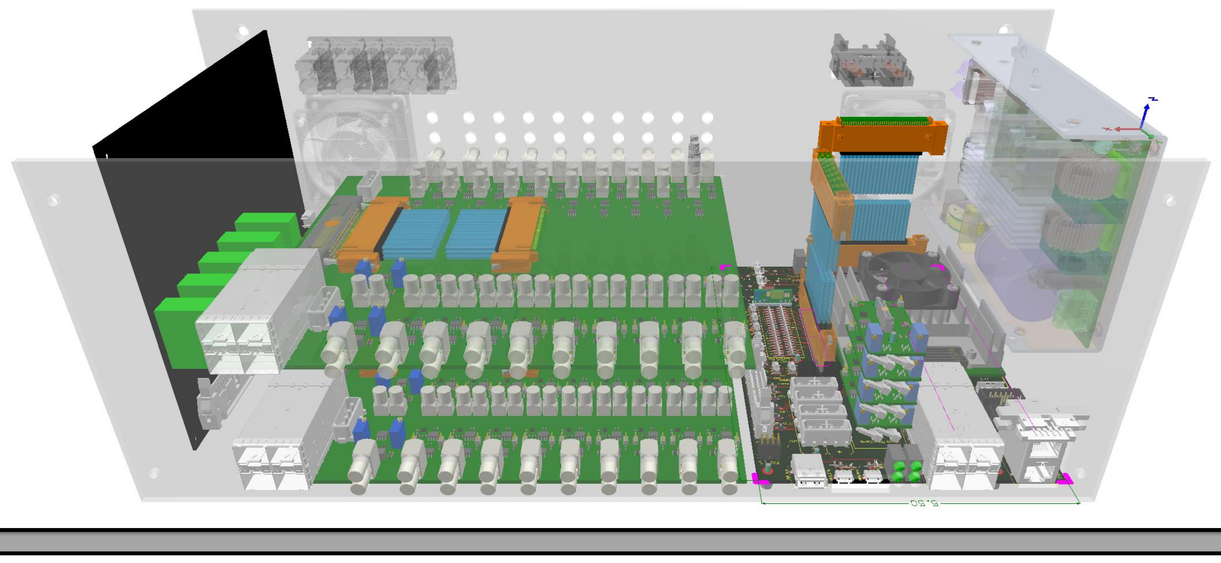
LCLK Frame	00	MSB LSB	MSB LSB	XXXXXXXX	X	111111 111111
72-bit	2 start bits	16-bit EVENT	32-bit Data	8-bit CRC	Parity bit	Pad bits #60-72

Triggering

The MultiFunction Timing Unit 2 (MFTU2) is used for decoding EVENTs from ACLK or LCLK and providing settable trigger delays.

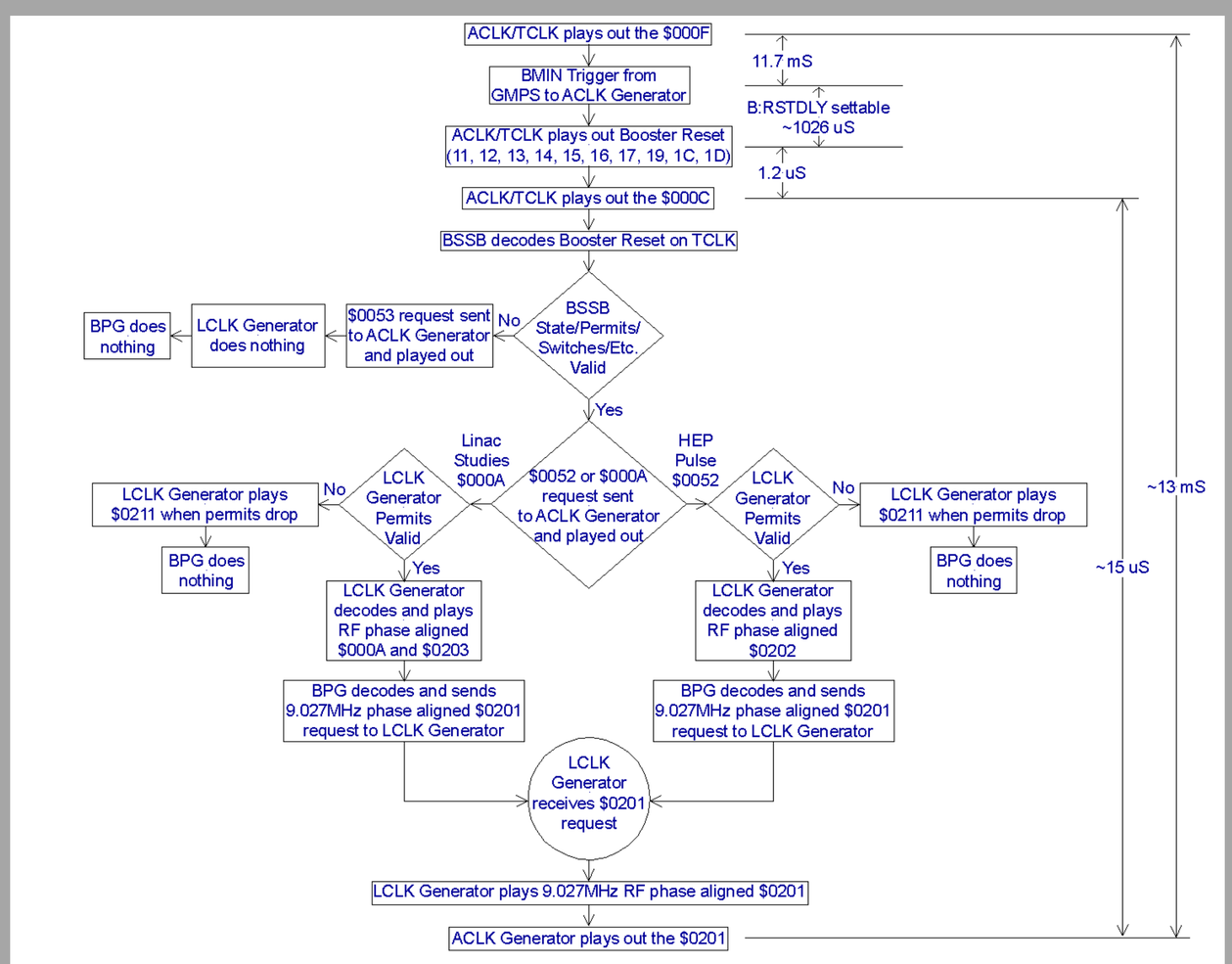


ACLK and LCLK Generators



- Comparable hardware
- Front End communication comparable to the TLG for TCLK
- Console Applications for user interface
- General purpose clock decoders using an FPGA design
- 650MHz based clock for both systems that uses Manchester encoding
- Data rate will be 1.3 Gbps
- 16-bit EVENTs have been defined for beam operation
- 32-bit Data could easily be a timestamp, status bits, or some other pertinent information

Timing Flow of Beam Request



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