

Novel phase-averaging reference system for the CiADS facility

Abstract

The China initiative Accelerator Driven System (CiADS) requires a stable phase reference distribution system (PRDS) to provide low-drift reference signals for over 300 radio-frequency (RF) clients on its superconducting linac and beam transport lines. PRDS is realized using a coaxial cable that transmits 162.5 MHz reference signals, and the phase averaging technique will be employed to counteract phase drift caused by changes in the cable length due to temperature variations. To address the limitations of the traditional phase-averaging solutions due to the presence of reflected signals, such as standing wave effects, demanding directivity requirements of directional coupler, and difficulties in phase reference line expansion, we propose an improvement based on a bi-line structure with unidirectional transmission of the reference signal and front-end phase locking. The design of the PRDS for the CiADS, the signal processing in the low level RF (LLRF) system and the test results of a prototype are detailed.

Phase reference requirements for CiADS

PRDS is required to provide RF reference signals for the RF clients (162.5/325/650 MHz), including 157 LLRFs and 169 beam diagnostic systems (BDS) distributed over more than 300m of beam transport line.

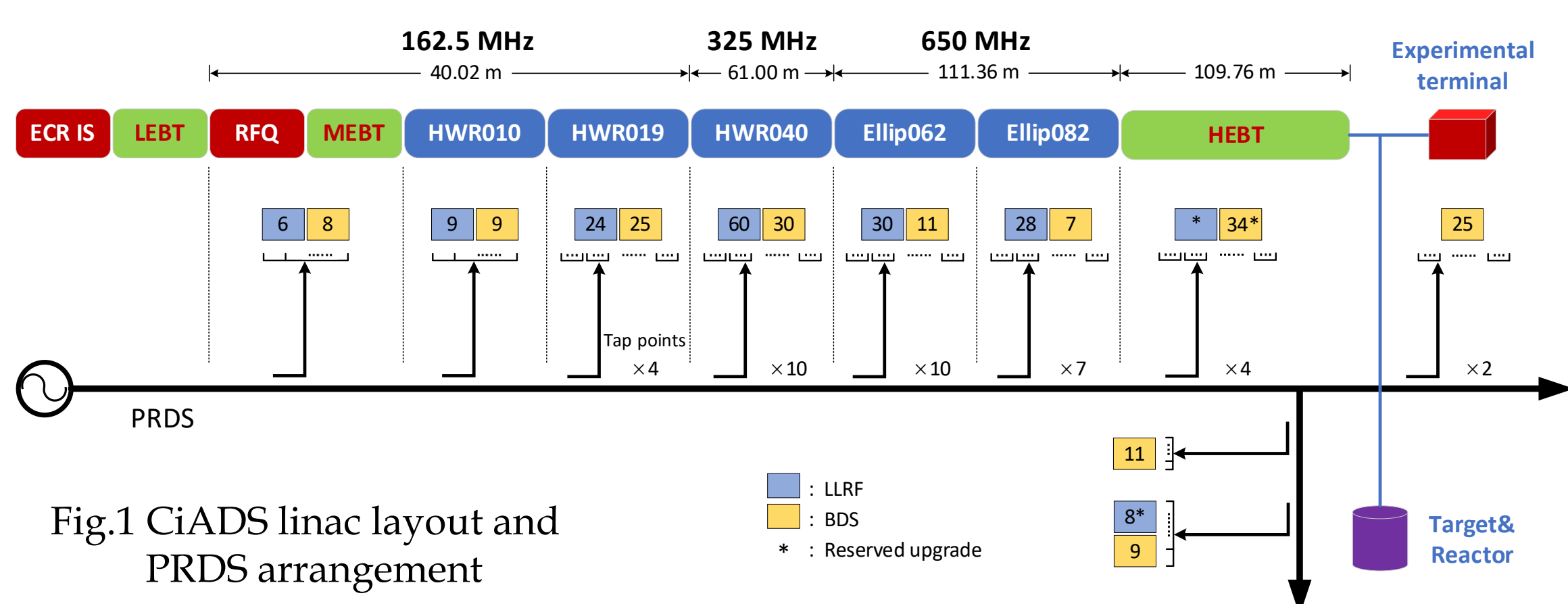


Fig.1 CiADS linac layout and PRDS arrangement

Phase averaging and key issues

The phase averaging technique can counteract the phase drift on the phase reference line (PRL) by extracting the forward and backward signals and phase-averaging at each tap point.

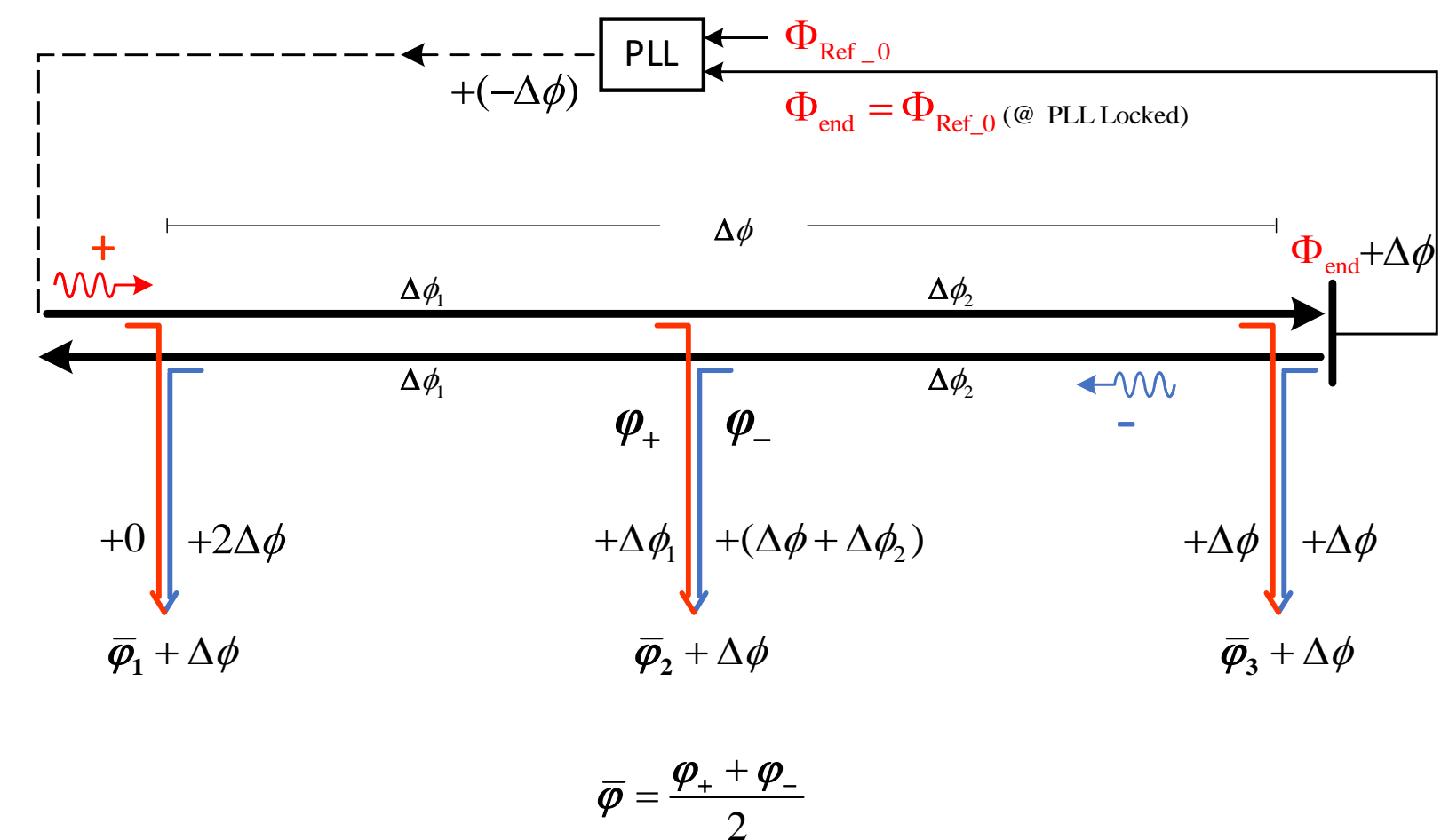


Fig.2 Principle of phase averaging

Traditional solutions usually use the reflected signal formed by a short circuit to perform phase averaging, and the forward and reflected signals are transmitted bidirectionally on the same transmission line.

- ! Standing wave between two taps, limitation on the number of tap points
- ! Signal crosstalk in couplers, demanding directivity
- ! Difficulty in PRL expansion

Bi-line front-end-phase-locked structure-based PRDS (BL-FPL scheme)

Phase reference line

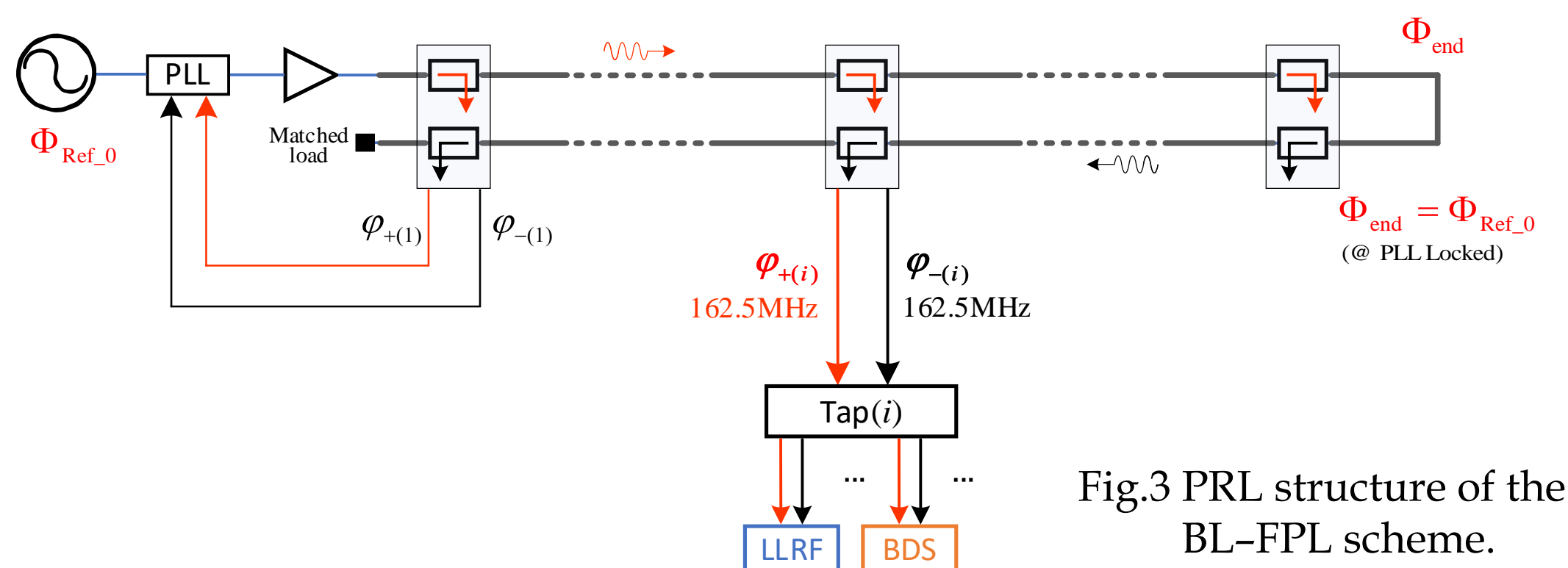
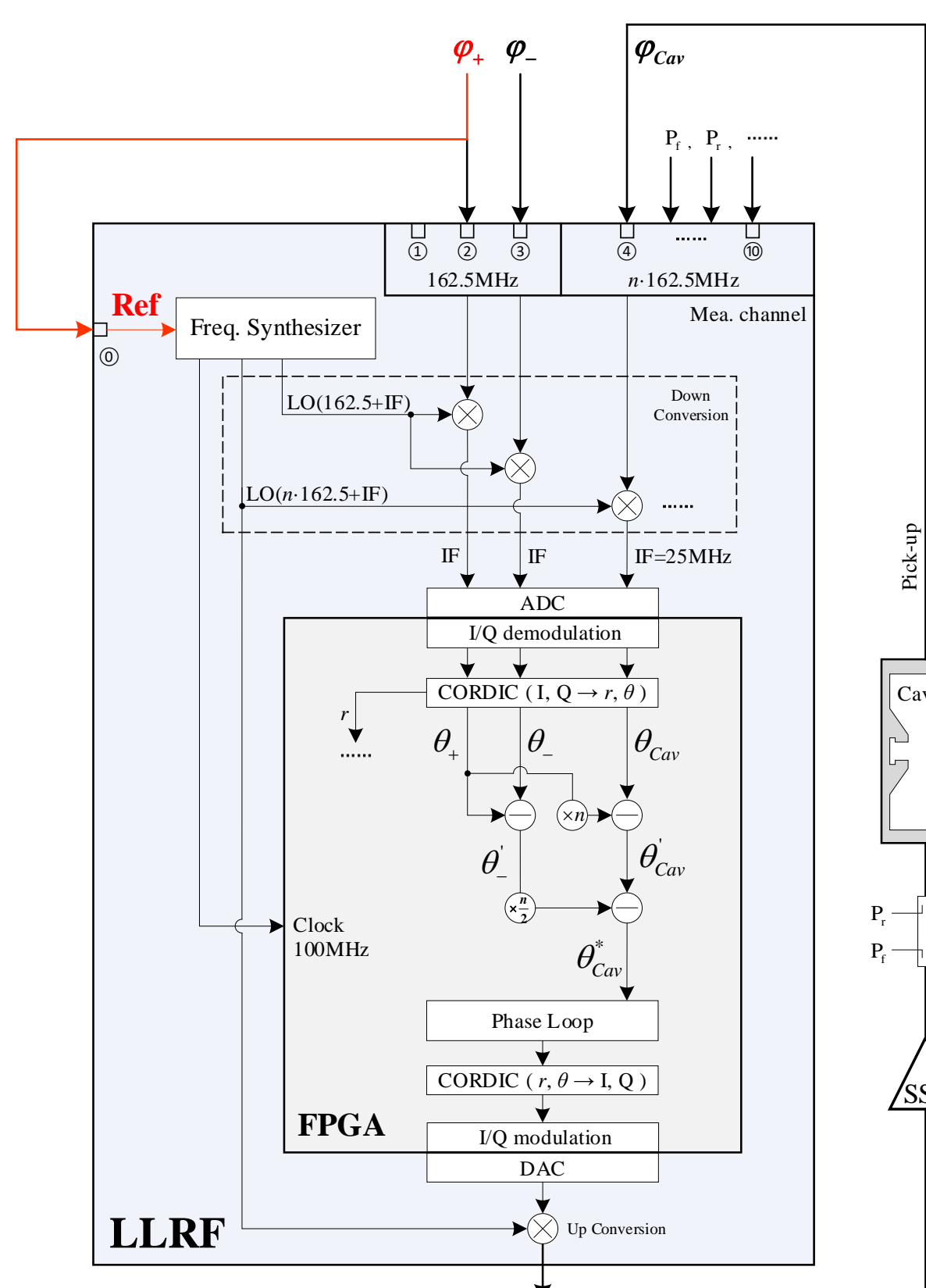


Fig.3 PRL structure of the BL-FPL scheme.

- Single-frequency 162.5 MHz signal transmitted unidirectionally via two coaxial cables.
- Terminal matching, no reflection.
- Two corresponding couplers extract two signals as “forward-backward” signals for LLRF/BDS reference.

LLRF and signal processing



- Forward signal is utilized as the reference clock of the LLRF.
- Forward signal self-test and channel phase drift calibration

$$\begin{aligned} \theta_+ &= 0 & \theta'_- &= \theta_- - \theta_+ \\ \theta_- &= \theta_- - \theta_+ & \theta'_{Cav} &= \theta_{Cav} - n\theta_+ \\ \theta_{Cav} &= \theta_{Cav} - n\theta_+ \end{aligned}$$

- Backward signal calibration and phase averaging

$$\begin{aligned} \theta^*_{Cav} &= \theta'_{Cav} - n \frac{\theta'_+ + \theta'_-}{2} = \theta_{Cav} - n \frac{\theta_+ + \theta_-}{2} \\ &= \theta_{Cav} - n \frac{\theta_+ + \theta_-}{2} = \theta_{Cav} - n\bar{\varphi} \end{aligned}$$

New internal reference $\bar{\varphi}$ is generated, $\bar{\varphi}$ of each LLRF is synchronized with Φ_{end} .

Fig.4 Schematic of the LLRF.

Front-end phase locking

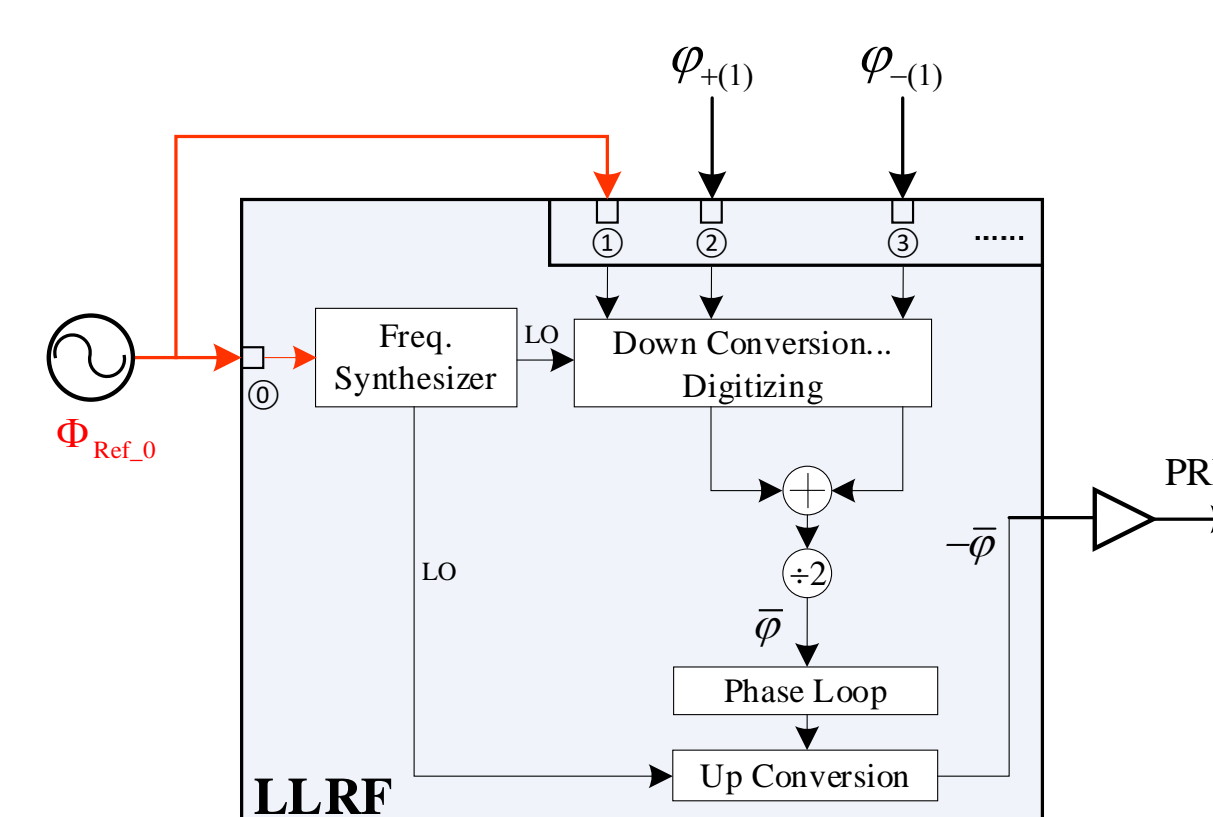


Fig.5 Schematic of the phase-locking process.

- Tap1 is used to construct a PLL at the PRL source end.
 - 1/2 Phase calibration
- $$\Delta\phi_{Feedback} = -\frac{\varphi_{+(1)} + \varphi_{-(1)}}{2} = -\bar{\varphi}$$
- The front-end phase (foldback point of the bi-line) is locked, Φ_{end} is indirectly locked to $\Phi_{Ref,0}$.

- A signal extracted from the foldback point can be used directly as the reference input for the secondary PRL.

Overall structure design

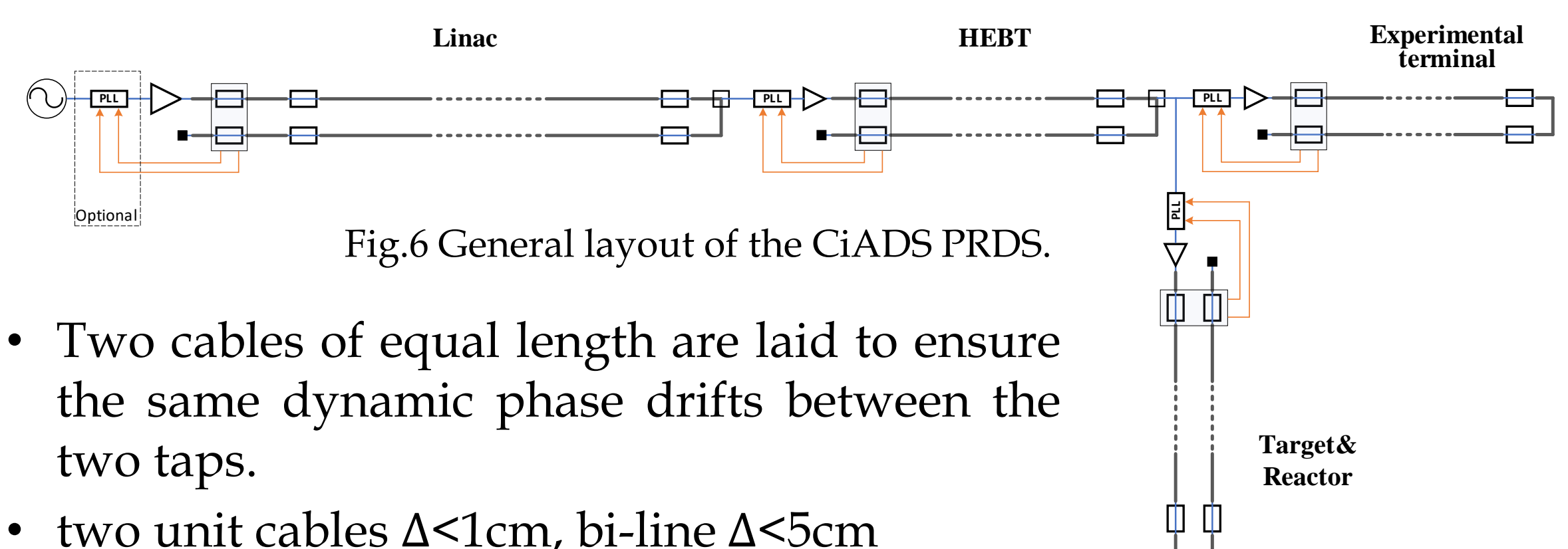


Fig.6 General layout of the CiADS PRDS.

- Two cables of equal length are laid to ensure the same dynamic phase drifts between the two taps.
- two unit cables $\Delta < 1\text{cm}$, bi-line $\Delta < 5\text{cm}$

Prototype testing

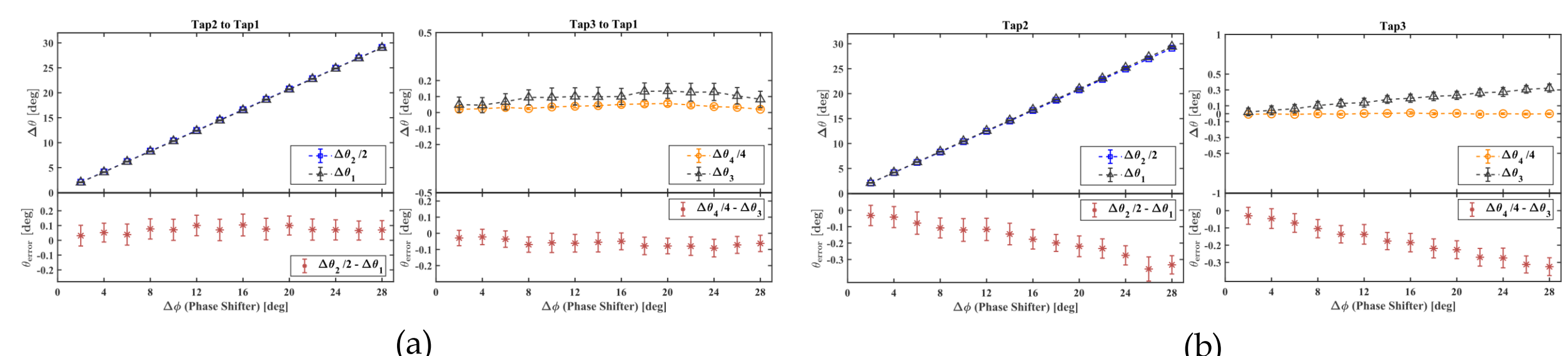


Fig.7 Test results of two prototype structures (both have three taps). (a) for the PLL-less structure and (b) for the front-end phase-locked structure. Two identical phase shifters are positioned on the bi-line, adjusting the same angle each time to simulate phase drift.