Status of the development of the new digital LLRF for ALBA Synchrotron Light facility

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Abstract

The Low-Level Radio Frequency (LLRF) system is a critical component in the control infrastructure of any synchrotron, responsible for generating and maintaining a stable electric field within the accelerator cavities by precisely controlling both amplitude and phase.

Safran Electronic & Defense Spain S.L.U. is currently engaged in the development of a new digital LLRF system to upgrade the existing infrastructure at the ALBA Synchrotron Light Source in Barcelona. This project is being executed in accordance with ALBA's technical specifications and will integrate with the ALBA LLRF firmware. On-site testing of the 500 MHz version is anticipated by end of 2024, with the 1.5 GHz third harmonic version scheduled for testing in the first quarter of 2025.

This work will cover the architecture, design, development, and performance evaluation of the LLRF system.

Hardware architecture used for the prototype at 500MHz

Timing Analog board

- RF input channels (MMCX connectors):
  - RF input for F_ref: this signal is the reference of the facility, and it is used to get the phase reference for all the RF signals in the system.
  - Up to 9 additional RF inputs to monitor RF signals.
- RF output channels (MMCX connectors);
  - Two RF outputs to drive 2 different cavities.
  - Output amplifier in both channels.
- Band pass filters in all the RF paths.
- Temperature sensor
- EEPROM memory

**Digital LLRF using Direct Sampling data acquisition**
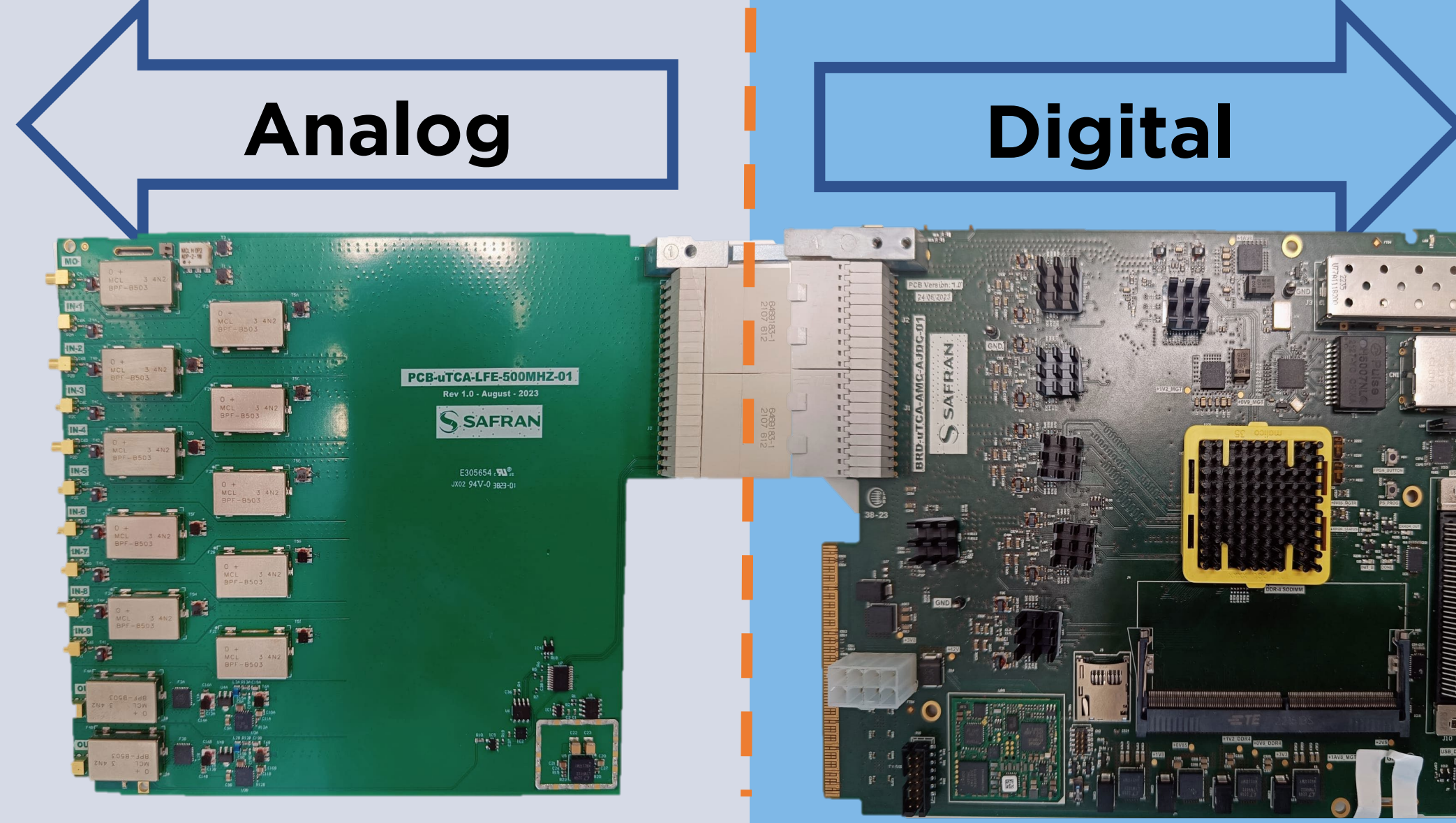
Analog Digital

ADC board (AMC digitizer controller)

- 5 x dual channel analog to digital converters (16 bits, 250MSPS ADC)
- 2 x Digital to analog converters (16 bits DAC)
- 32 x GPIO ports
- Zynq UltraScale+ FPGA from Xilinx
- PLL to generate internal clock signals
- 8GB DDR4 memory for processor and data storage (postmortem analysis)
- uTCA MMC stamp
- Temperature sensor
- uSD socket, uUSB port
- ETH & SFP port (White Rabbit compatible)
- EPICS/TANGO compatible (control system)
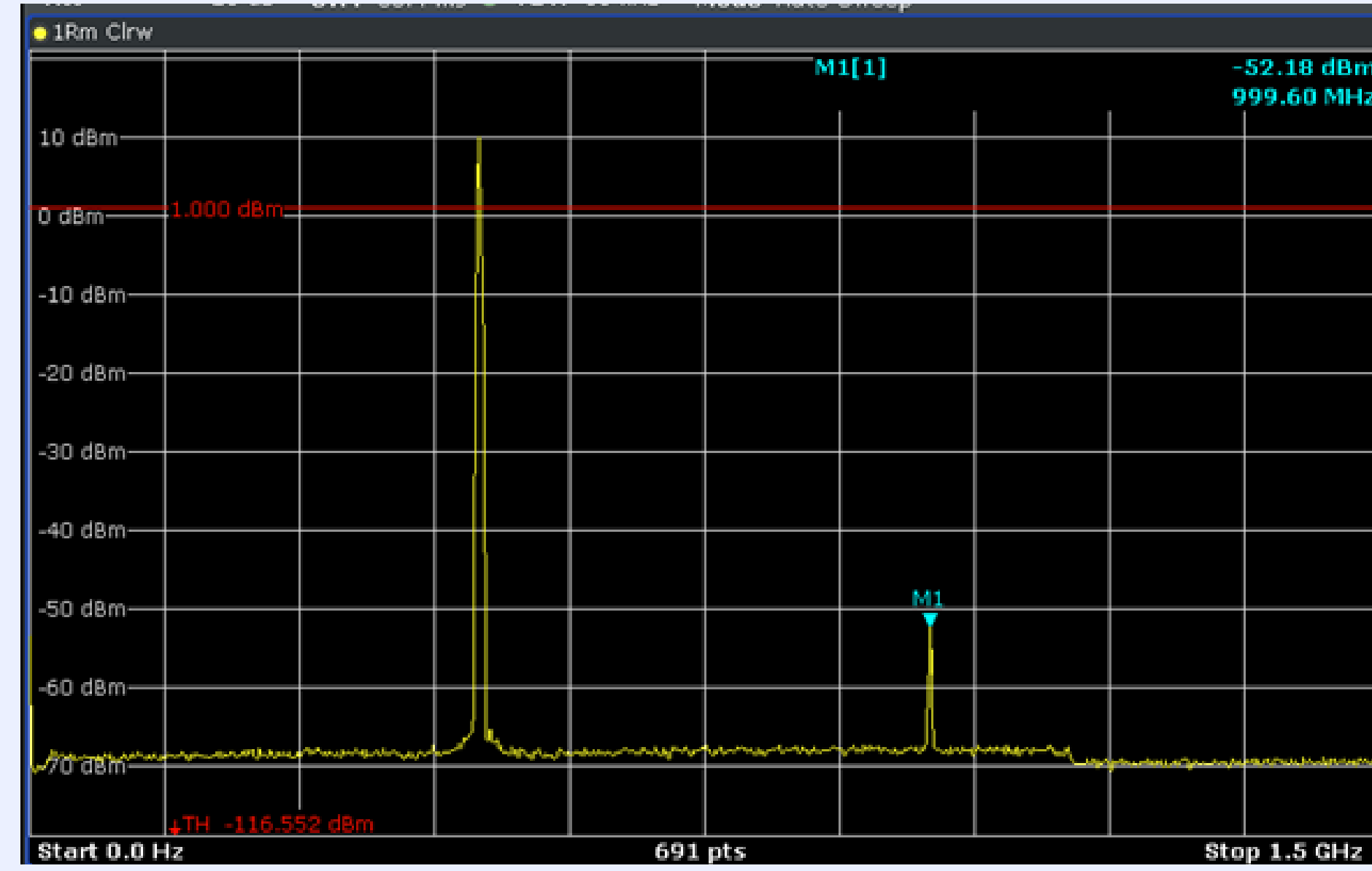
System performance measured

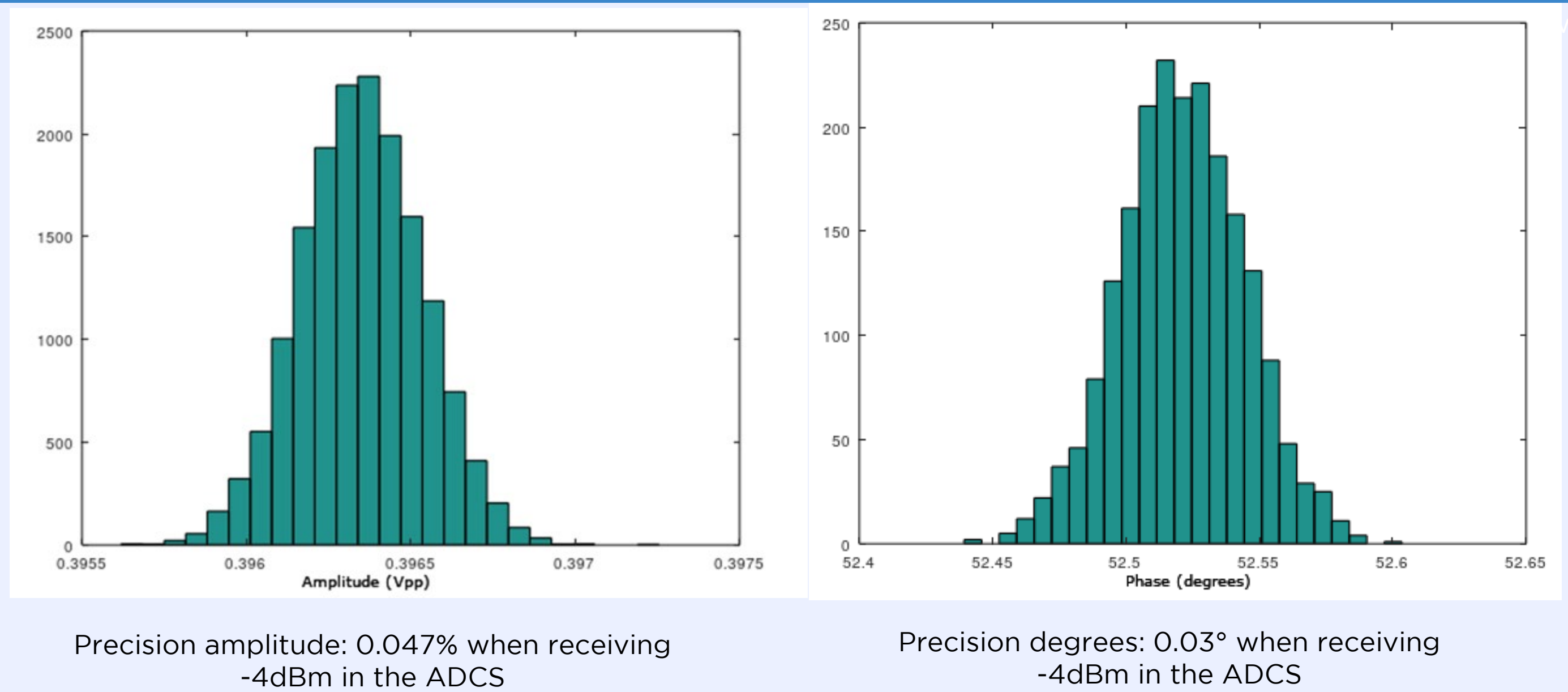### System added rms Jitter
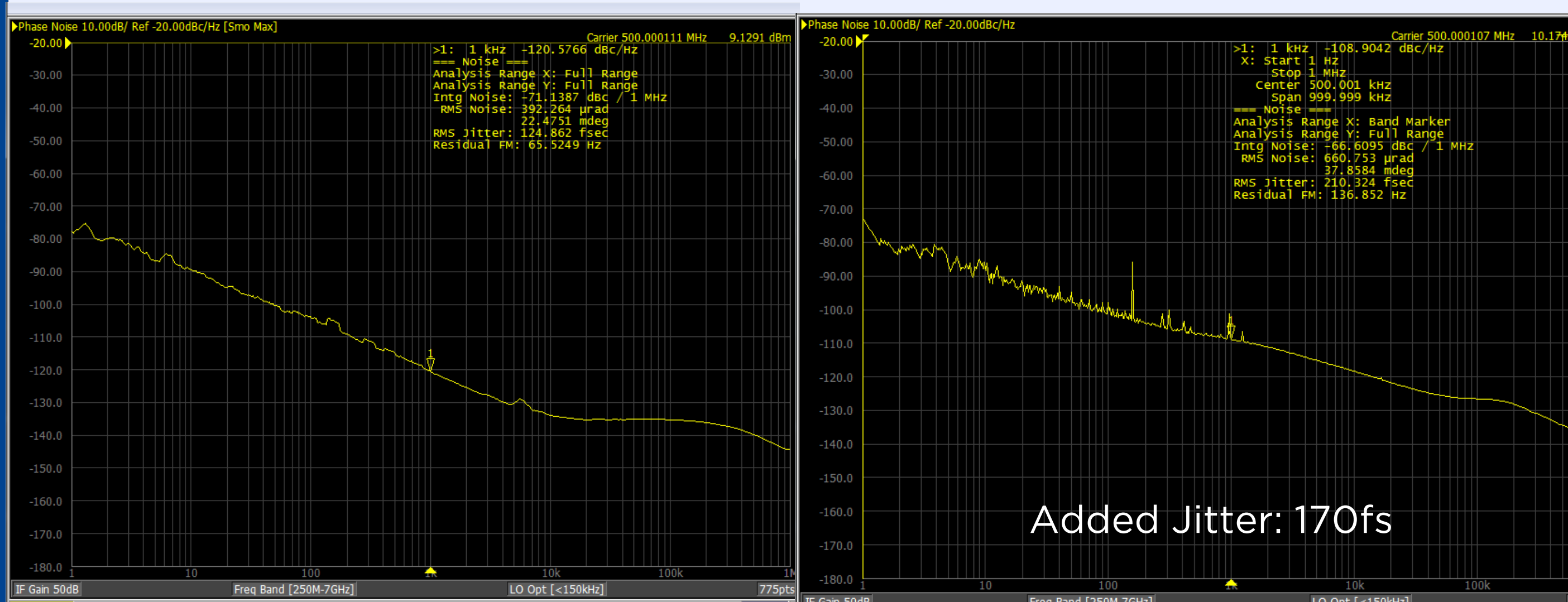
Jitter of the reference at 500MHz - 125fs (rms)

Added Jitter: 170fs

Jitter of the RF output at 10dBm - 210fs (rms)

Output signal level – 10 dBm

First harmonic level is 62dB below the fundamental
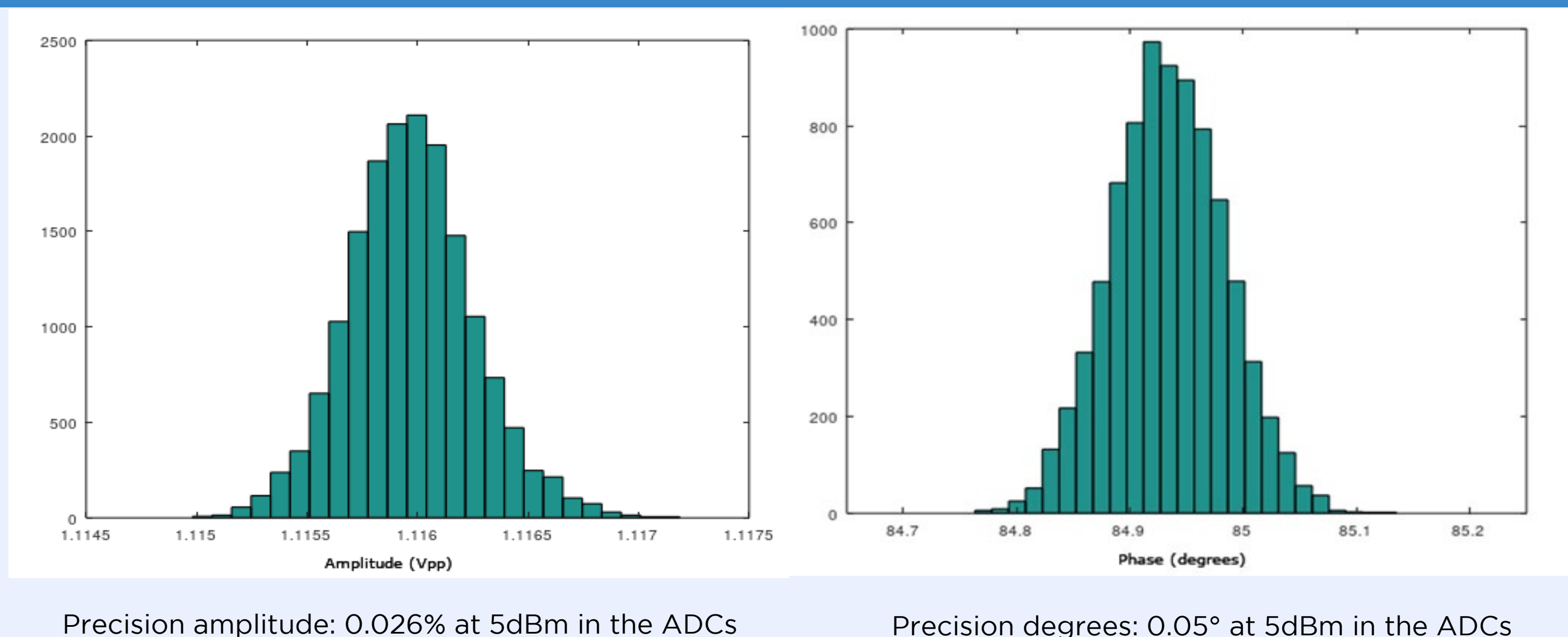
RF input precision amplitude/phase – single channel

Precision amplitude: 0.047% when receiving -4dBm in the ADCS

Precision degrees: 0.03° when receiving -4dBm in the ADCS

RF input amplitude/phase precision – all channels

- Amplitude precision (%)
- Phase precision (º)
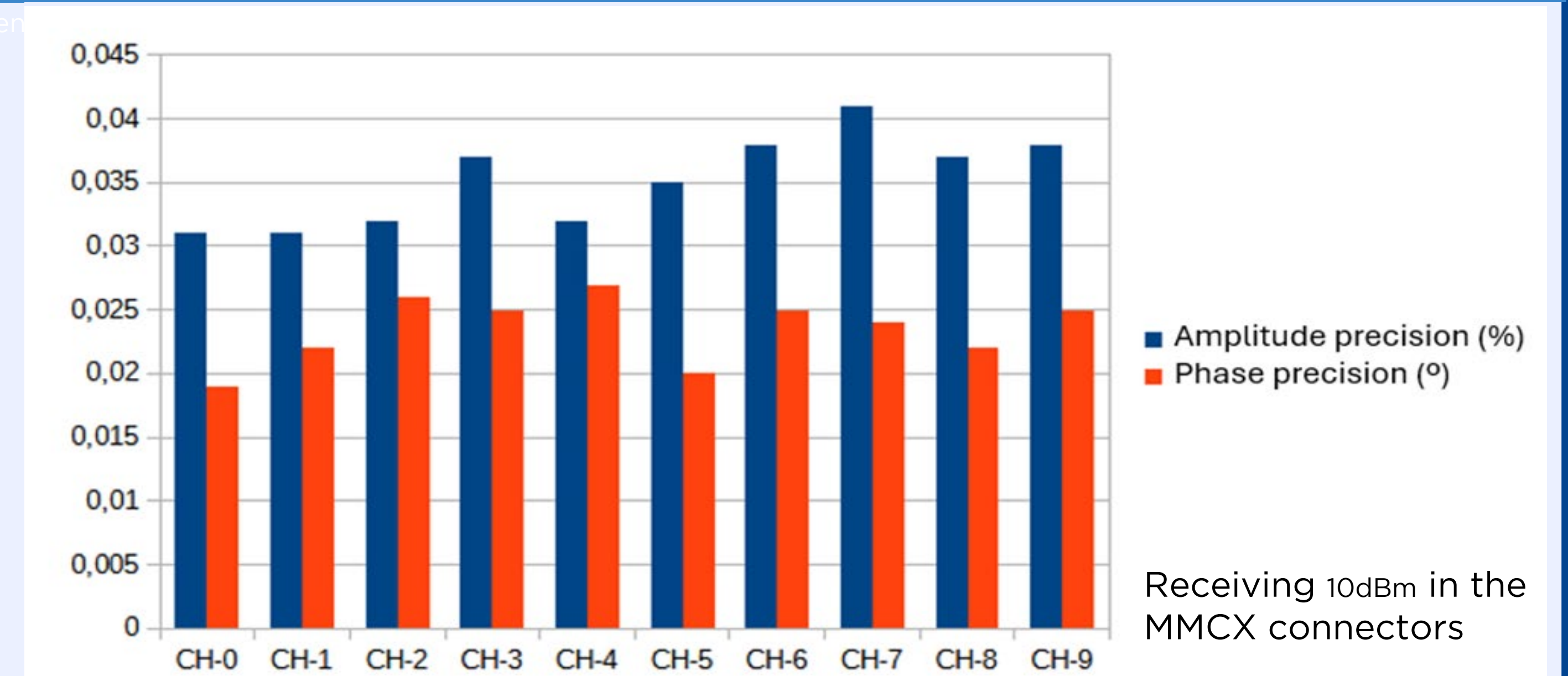
Receiving 10dBm in the MMCX connectors

RF Output precision amplitude/phase

Precision amplitude: 0.026% at 5dBm in the ADCs

Precision degrees: 0.05° at 5dBm in the ADCs

Crosstalk between inputs channels (dB)

	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	Ch9
CH1		-74,38	-67,04	-64,81	-66,22	-67,1	-66,55	-67,19	-67,51
CH2	-64,1		-64,14	-64,59	-71,42	-67,52	-67,83	-68,49	-68,6
CH3	-61,65	-61,17		-58,23	-59,66	-53,96	-61,8	-62,71	-61,43
CH4	-67,91	-64,22	-68,97		-61,06	-72,7	-69,53	-73,57	-77,34
CH5	-71,99	-74,43	-62,73	-63,91		-63,56	-59,15	-78,25	-70,69
CH6	-66,58	-66,26	-55,01	-65,82	-63,53		-67,42	-64,69	-65,73
CH7	-74,87	-71,99	-72,32	-69,71	-60,17	-67,26		-61,68	-79,14
CH8	-73,43	-72,65	-74,35	-72,98	-81,54	-62,15	-61,98		-63,42
CH9	-74,54	-70,99	-73,46	-74,88	-73,78	-71,77	-72,45	-62,21	

Receiving 10dBm in the MMCX connectors