Status report on the fast front-end design for Layer0-3 strip detectors

M. Manghisoni, L. Ratti

Università degli Studi di Pavia

INFN Pavia

SuperB strip FE phone meeting, 14/10/2011

Analog FE efficiency simulations

- Generation of a random sequence of voltage pulses - output response to background hits of an analog channel with an RC^2-CR shaper
  - hits occur in time as Poisson points – the time interval between two subsequent events is a random number with Poisson distribution (the average hit rate for each layer is provided by physical background simulations)
  - hit energy distribution is provided again by physical background simulations (results supplied by Carlo Stella) – simulation data have been interpolated with Moyal distribution

$$p(E) = \frac{\exp\left[-\frac{1}{2}\exp\left(-\frac{E-E_P}{E_M}\right)-\frac{E-E_P}{2E_M}\right]}{\sqrt{2\pi}\,E_M}$$

E_P is the MPV while E_M accounts for the distribution width

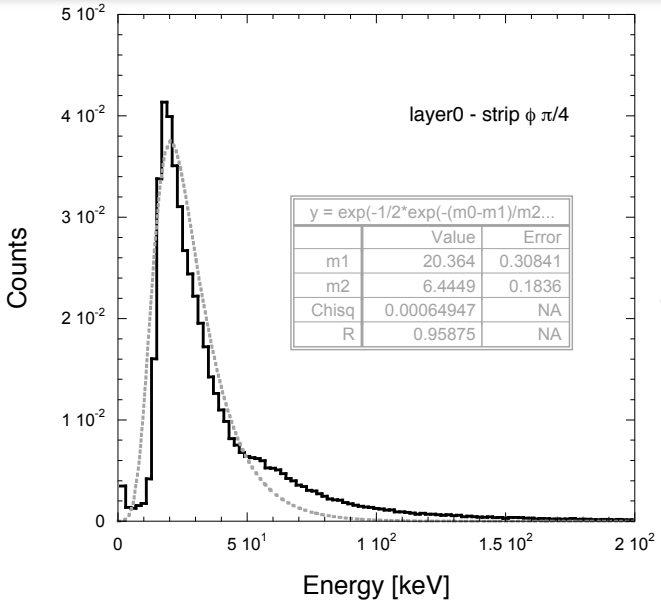
  - Efficiency is computed as

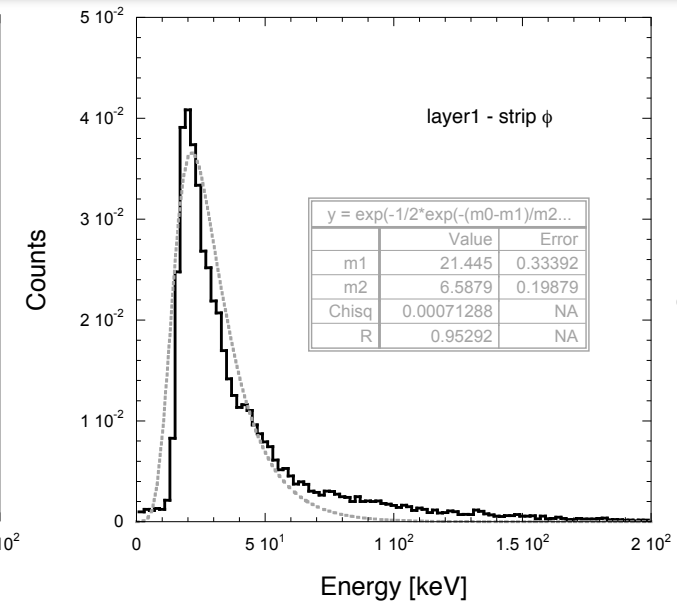
$$\eta = \frac{n-l}{n} = 1-\frac{l}{n} = 1-\frac{TOT_{BG}\cdot r}{\Delta T\cdot r} = 1-\frac{TOT_{BG}}{\Delta T}$$

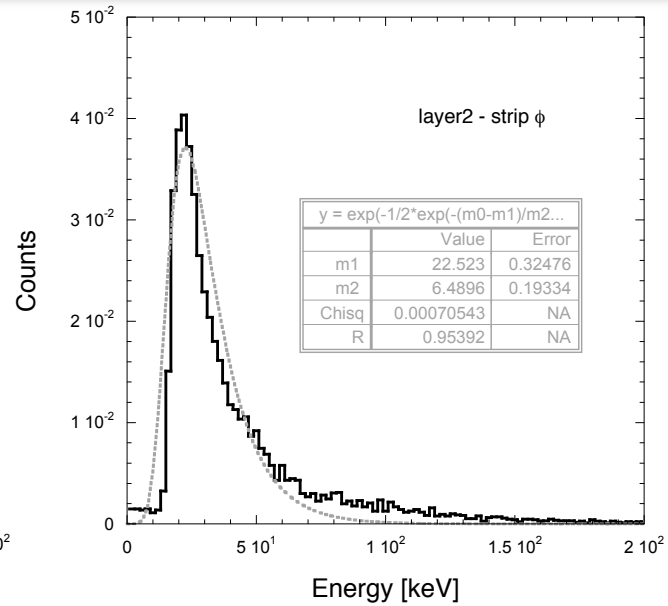
n is the total number of interesting events during ΔT, l the number of lost events in ΔT, TOT_{BG} is the time over threshold during ΔT due to BG events, r is the rate of interesting events

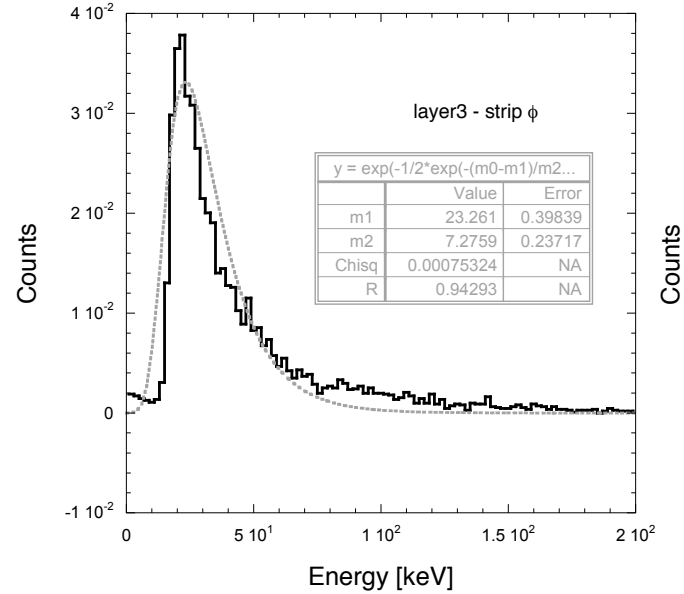
  - On every layer, threshold=MIP/4 (4000 e^- on layer0, 6000 e^- on the other layers)

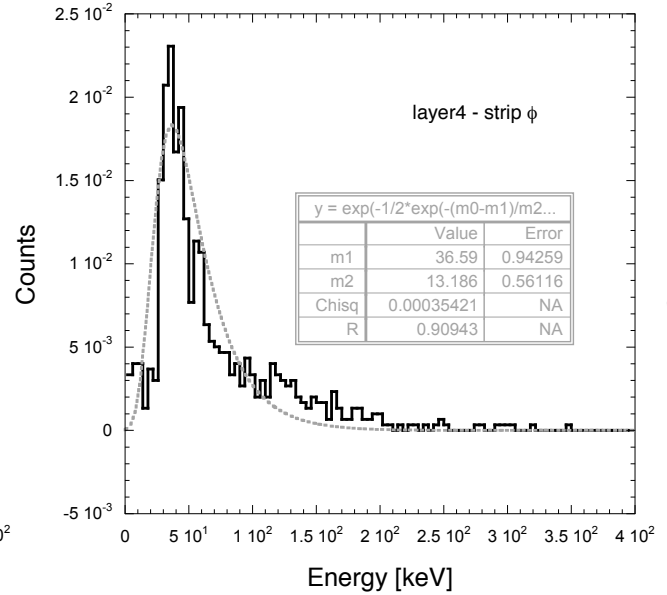
Energy distribution per strip (from TS) and fit

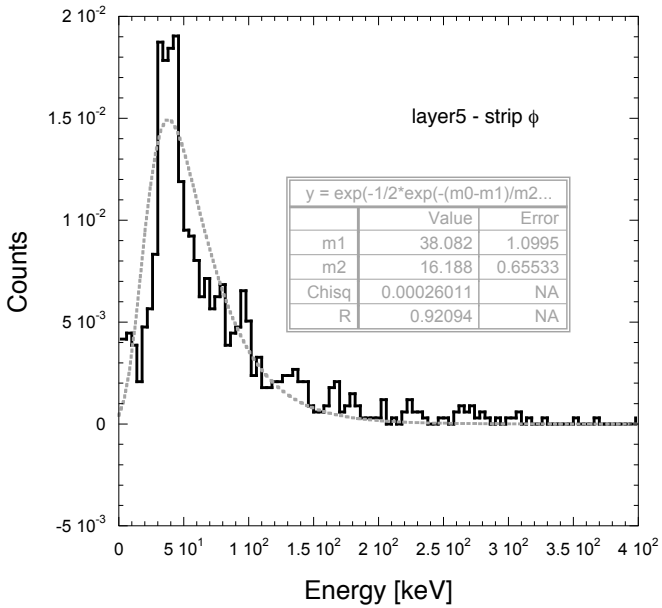












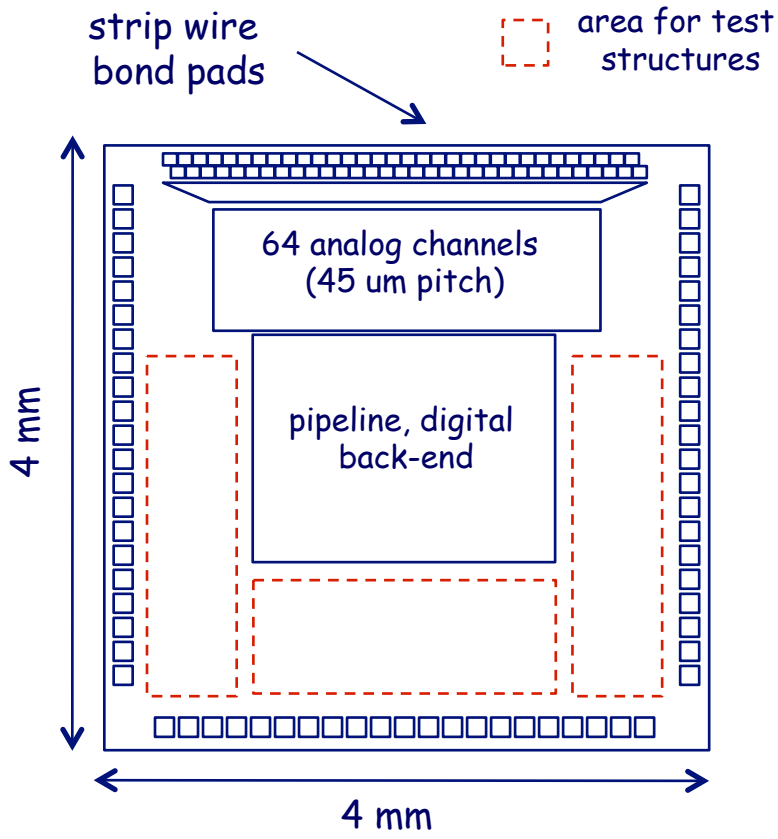
Microstrip detector: proposed layer grouping

Layer	C_D [pF]	available t_p [ns]	selected t_p [ns]	ENC from R_S [e rms]	ENC [e rms]	Channel width [μm]	Hit rate/ strip [kHz]	Efficiency 1-N
0	11.2	25, 50, 100, 200	25	220	**740**	3000	1370	0.948
1	26.7		100	460	**940**		429	0.959
2	31.2		100	590	**1100**		268	0.976
3	34.4		200	410	**940**		105	0.982
4	52.6	400, 600, 800, 1000 (or 500 and 1000)	500	490	**1000**	9000	17.5	0.993
			600	440	**940**			-
5	67.5		800	560	**1090**		11.3	-
			1000	500	**1030**			0.990

- RC^2-CR shaping, I_D=500 μA, L=200 nm, N-channel input device, efficiency based on BG hit energy distribution (from TS simulations)

Strip front-end development

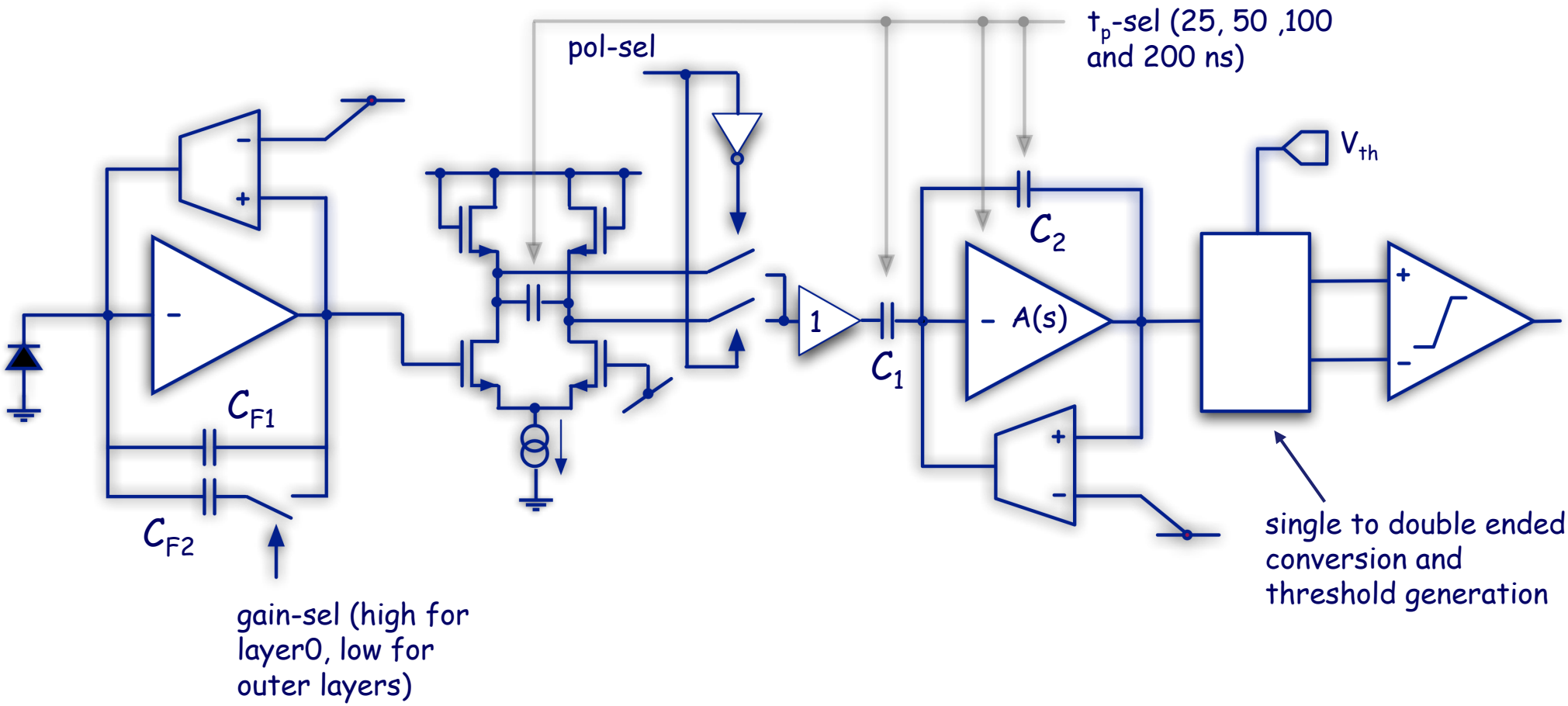
- Fast and slow front-end prototype chip (IBM 130 nm)



- Milestones for strip front-end development
  - 2012: first test structures - 2 x 64 channels (fast and slow front-end), auxiliary blocks – completion by Q3-Q4
  - 2013: first fully operational prototype chip – 2 x 128 channels (fast and slow readout)
  - 2014: production run
  - Account for some contingency after the first or the second step

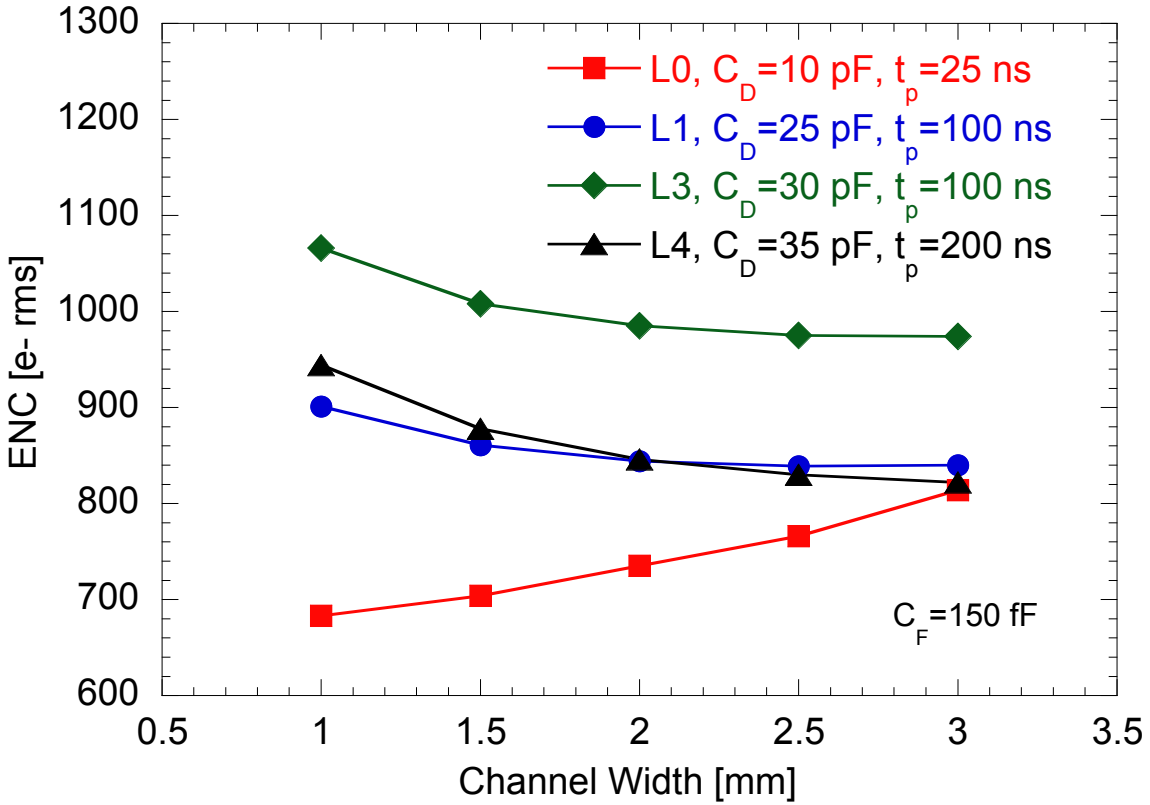
Fast front-end block diagram

- Schematic simulations of charge preamplifier + integrator (I_D=500 µA in the preampli input device, 1.33 mW power consumption in the preampli including bias networks)



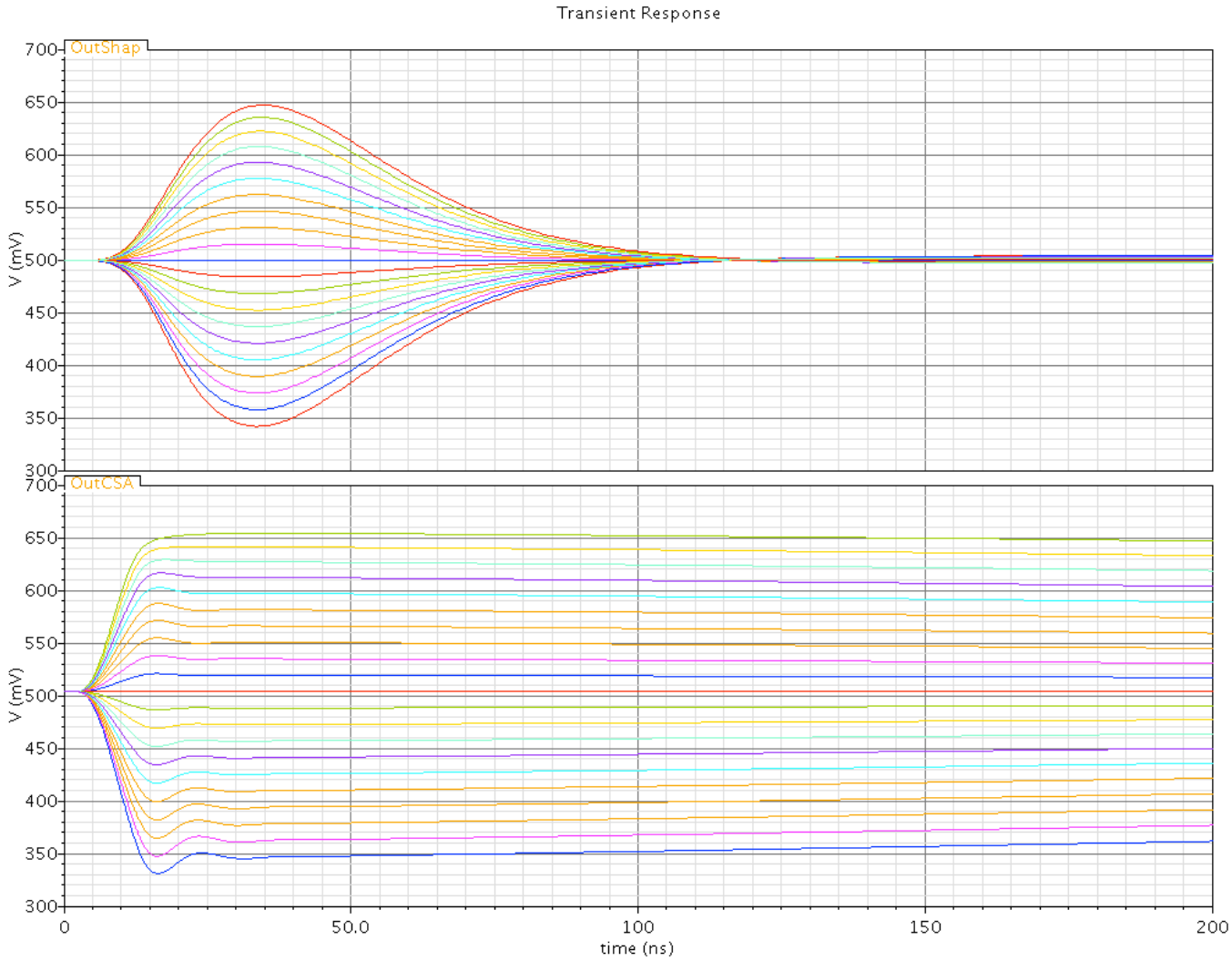
Equivalent noise charge

- Results obtained with ideal RC^2-CR shaper and including real bias networks



Response to a charge signal

- Response to varying input charge (-100 ke$^-$ to 100 ke$^-$, C_F=100 fF)



Charge preamplifier response linearity

Input charge from -100 ke$^-$ to 100 ke$^-$ (low and high gain configuration)