

ALICE3 Timing
WG meeting

May 13th 2024

Beam test April 2024: short summary

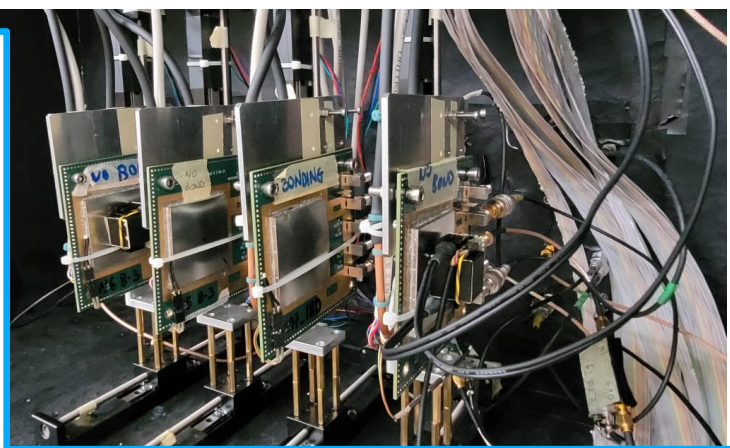
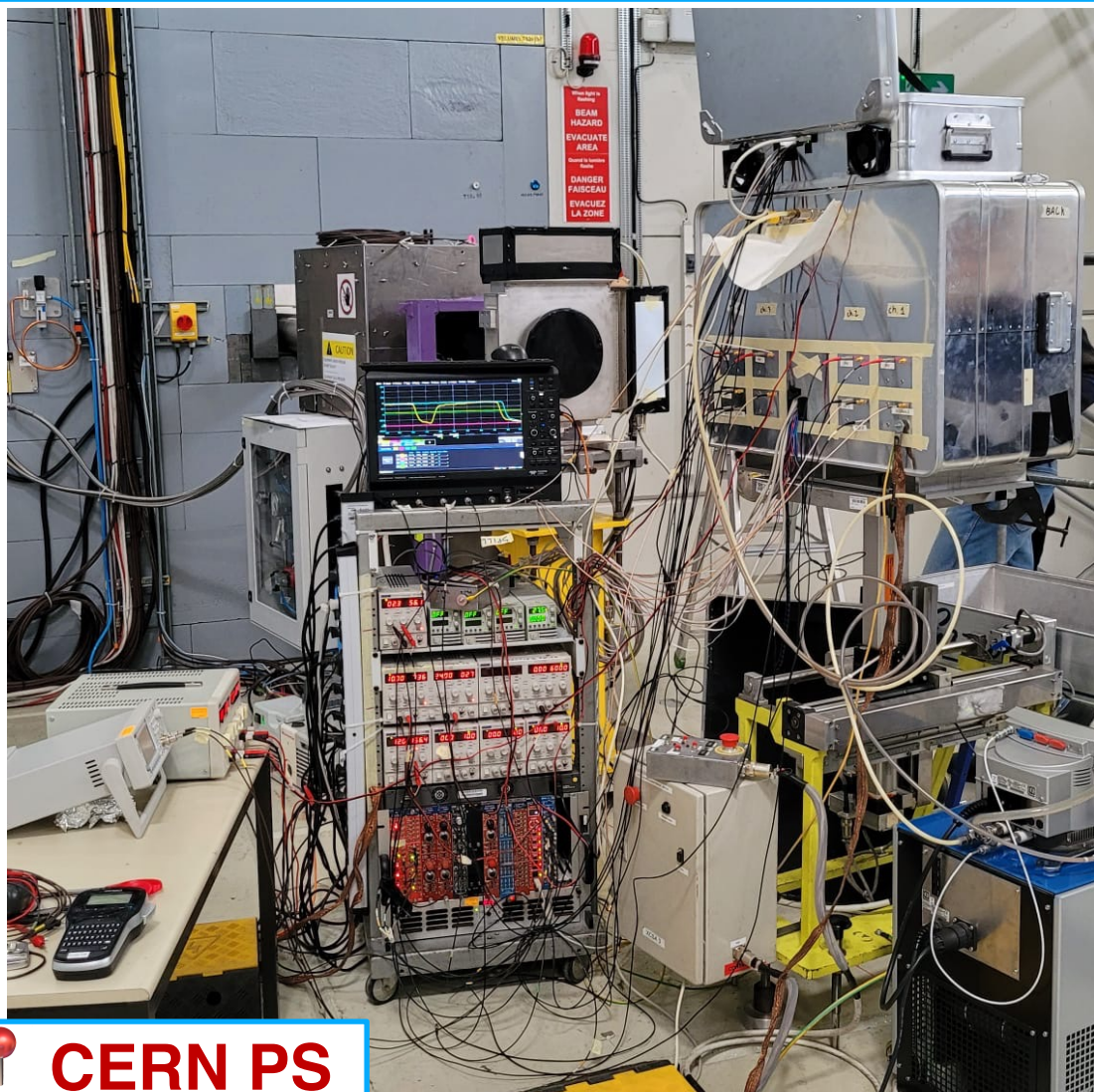
Manuel Colocci, Sofia Strazzi



ALICE



TEST BEAM SETUP



 **CERN PS**

x2 picoTDC board

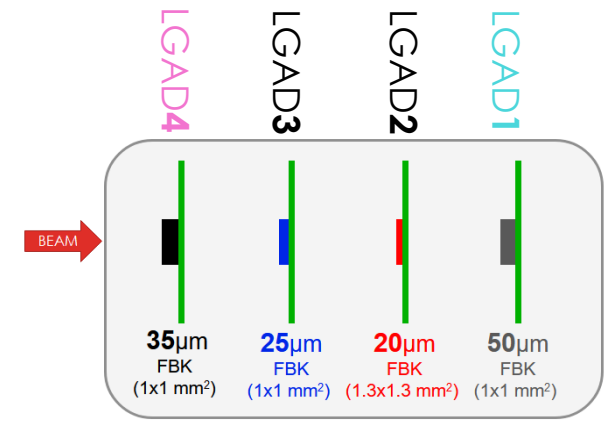
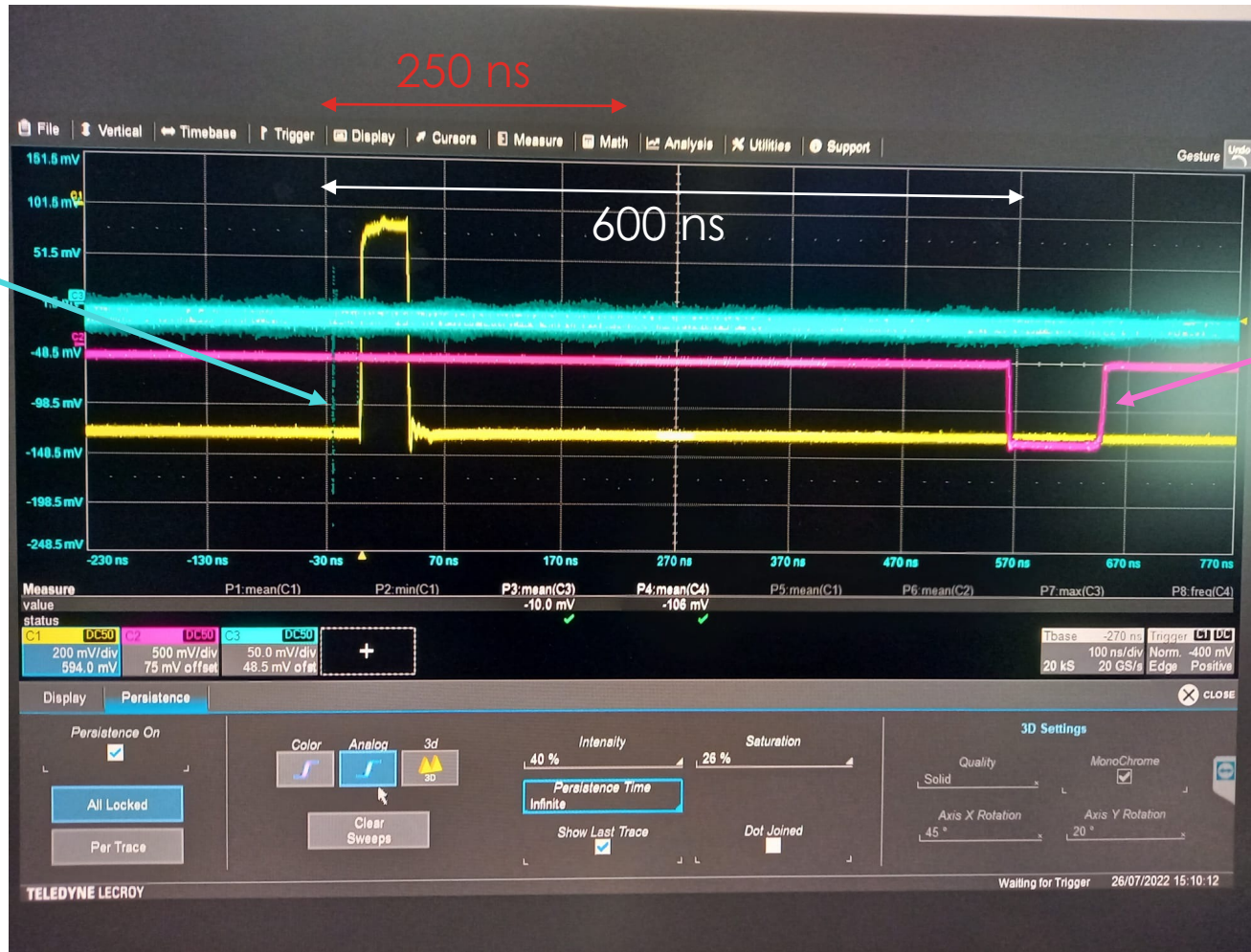
Liroc (discriminator)

ALIGNMENT, TRIGGER AND THRESHOLDS

- The **alignment** was done in the most of the cases with the **oscilloscope**; some last configurations aligned **directly with the picoTDC** looking at the number of events taken by each DUT
- ~~Trigger baseline: external trigger with 4 SiPMs signals discriminated by LIROC, in AND with LogicUnit~~
 - **Trigger backup**: single coincidence with **one LGAD**
(3 channels available on the oscilloscope)
- **Thresholds** could **not** be chosen on the picoTDC using the **direct signals** on the oscilloscope → Necessity to see the signals from LIROC (internal amplification stage)

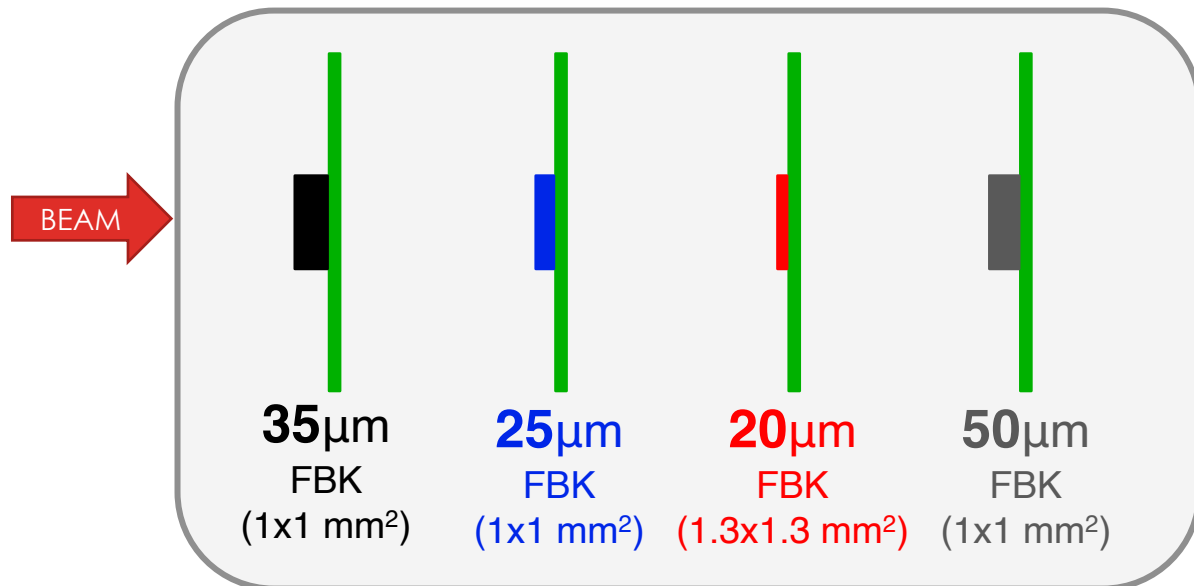
Trigger at work

LGAD1
analog
signal



LGAD4 Trigger
signal to picoTDC
(here in NIM format,
instead of TTL)

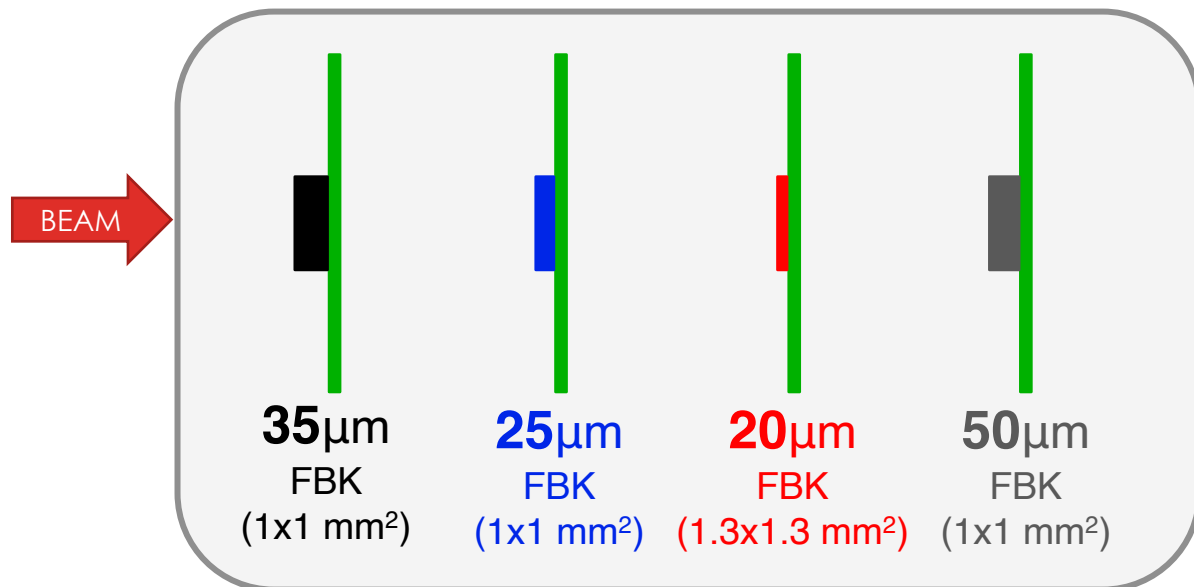
(for reference) In C1: LGAD4
trigger signal directly out the
CAEN discriminator (-10 mV
threshold) before being
stretched and delayed



- Only oscilloscope
- LIROC (oscill. readout)
- LIROC + picoTDC

→ **Comparison of the performance of sensors connected to the different stages of electronics**

- Different number of amplification stages
- Different voltages
- Different threshold on picoTDC



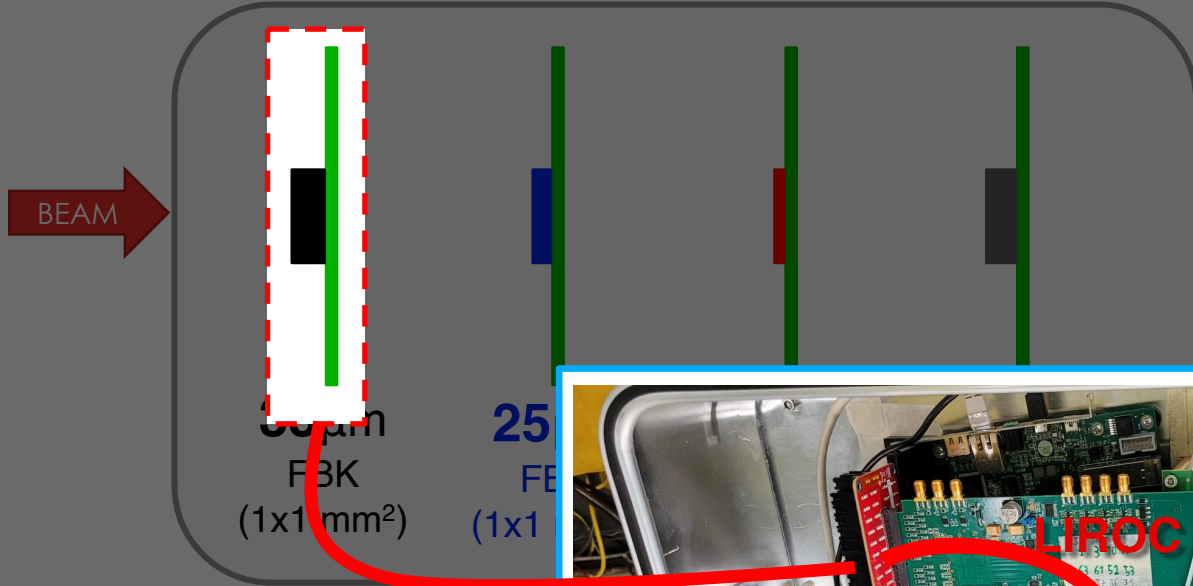
Results in agreement with previous TBs 😊

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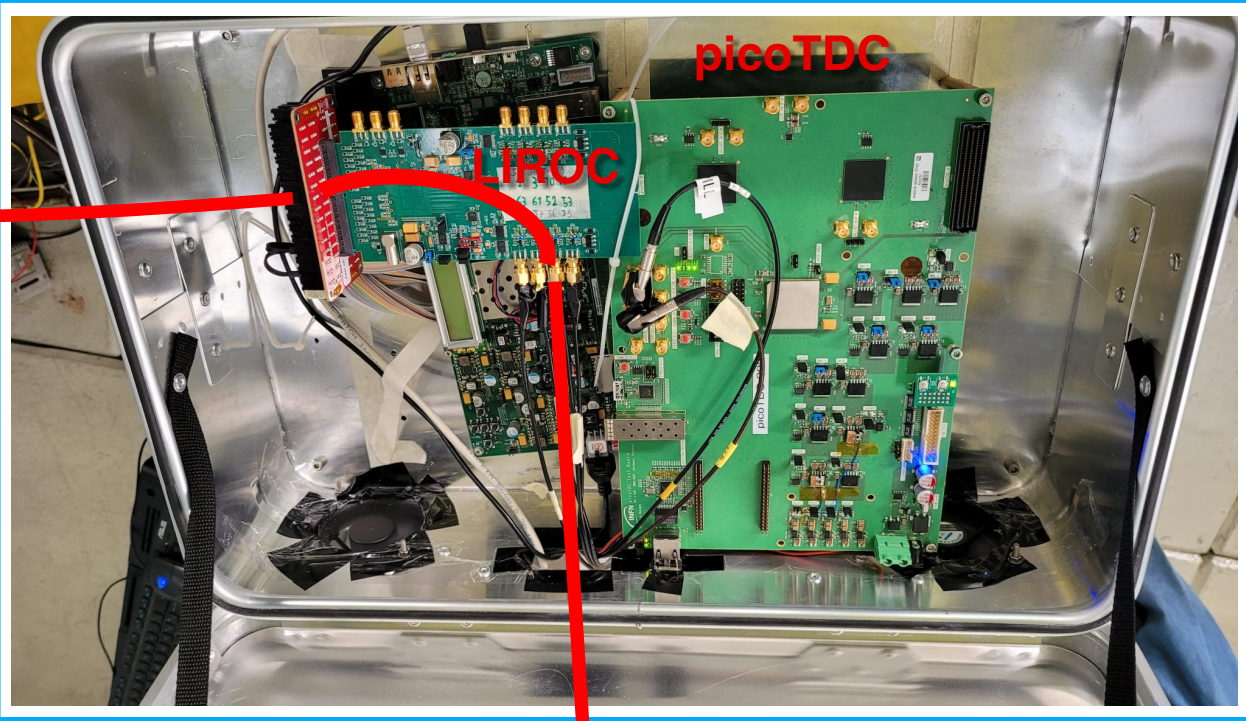
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LGADS



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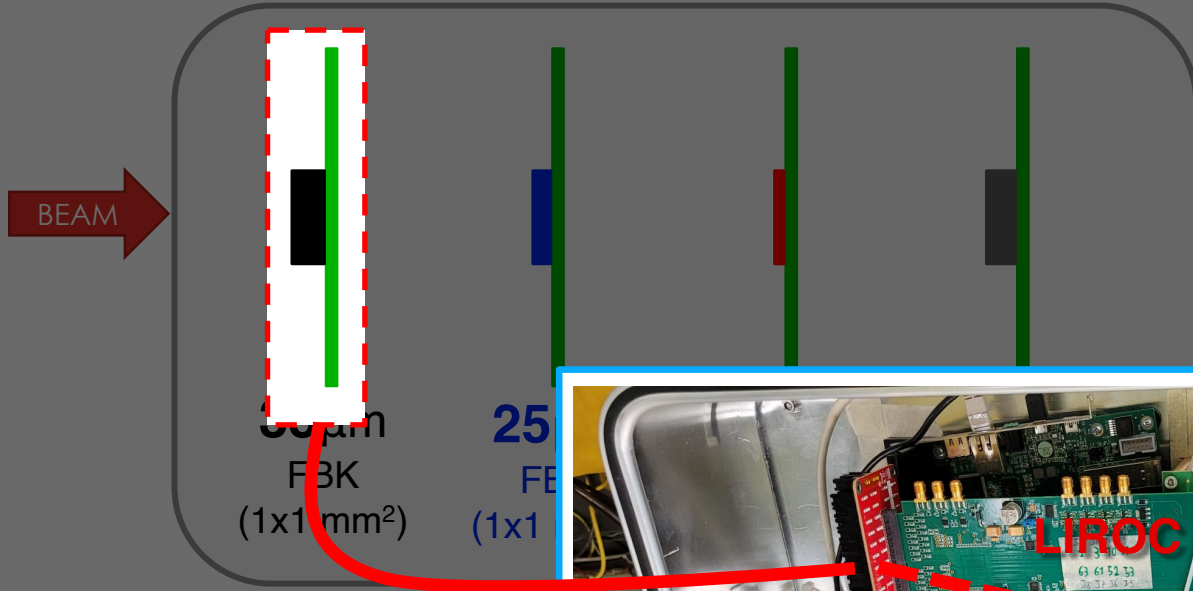


Comparison of the
of sensors
the different
electronics

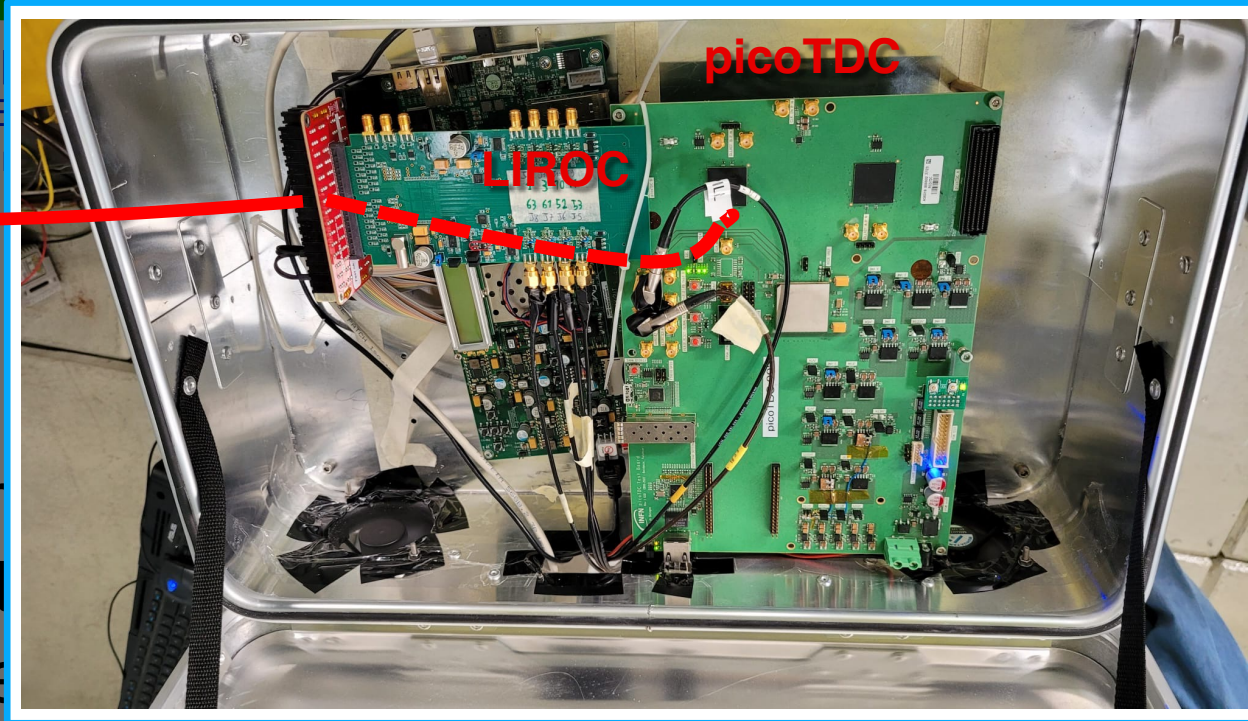
- Different number
- Different voltages
- Different thresholds

OSCILLOSCOPE

LGADS



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LGADS

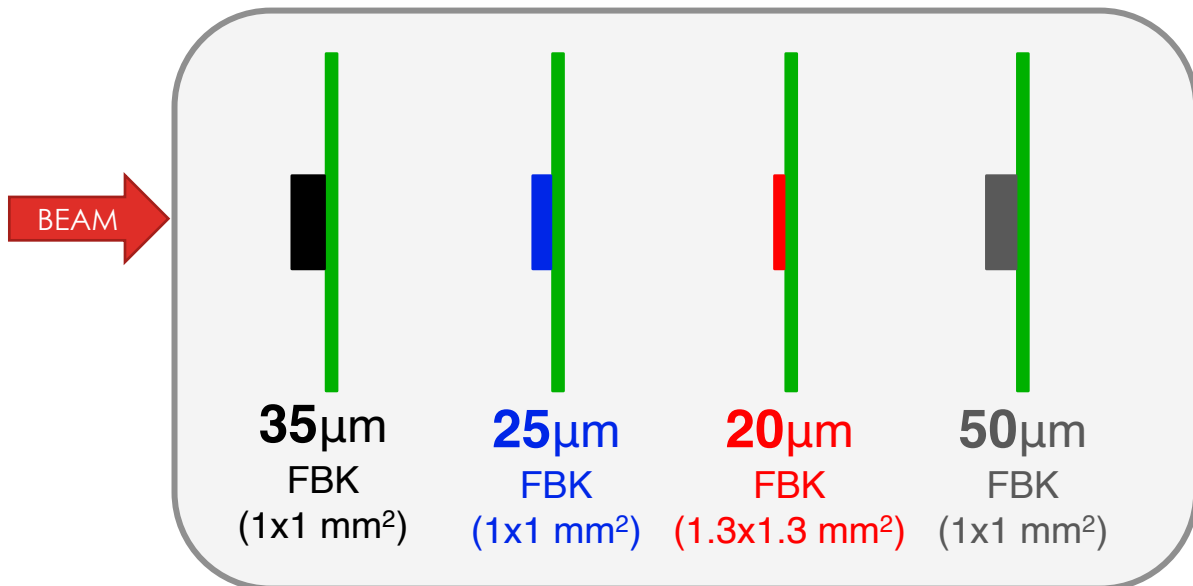
**DAQ
at work**

hits per spill
(both leading
& trailing edges)

Per spill
Since SOR

```
----- PicoTDC Board Readout Status --- @ 30/04/2024-03:43:55
Run # 104 WAIT SPILL SOR: 30/04/2024-03:31:45 EOR: 01/01/1970-01:00:00
Events | 01188689 | # triggers since SOR | Buffers 00068390 | Ev/Buffer 17.3
Spill | Uptime: 158.4 (s) | OFF | Off->On 066 | On->Off 066 |
Memory | Max FPGA buffer size 00001814 | Max hits/event 00000030
-- LAST Spill Stat --- Spill # 066 --- LGAD4 triggers (in the spill) -----
Duration 2.40 (sec) Events: 18140 Ev. rate 2.400000 [KHz] |
PCI MEM 00243078 | FPGA MEM 000024 | Hit 0
[00] 00004193 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[08] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[16] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[24] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[32] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[40] 00000000 00000000 00000000 00000000 00000000 00000000 00009477 00000000
[48] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[56] 00000000 00000000 00000000 00000000 00011728 00000000 00000000 00000000
-- All Run stat ----- LGAD3 -----
[00] 00273108 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[08] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[16] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[24] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[32] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[40] 00000000 00000000 00000000 00000000 00000000 00000000 00616410 00000000
[48] 00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
[56] 00000000 00000000 00000000 00000000 00770940 00000000 00000000 00000000
MULT: 0 1 2 3 4 5 6 7 8 9 10
      61424 36475 16085 48840 00000 00000 00000 00000 00000 00000 00000
```

events when
0, 1, 2, etc
channels fired

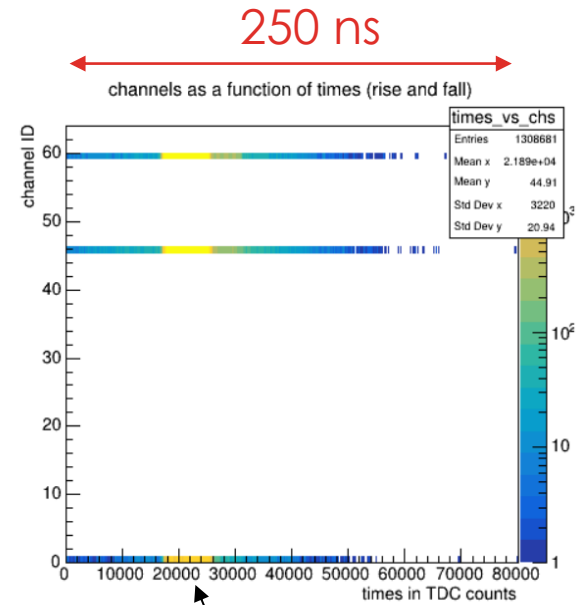
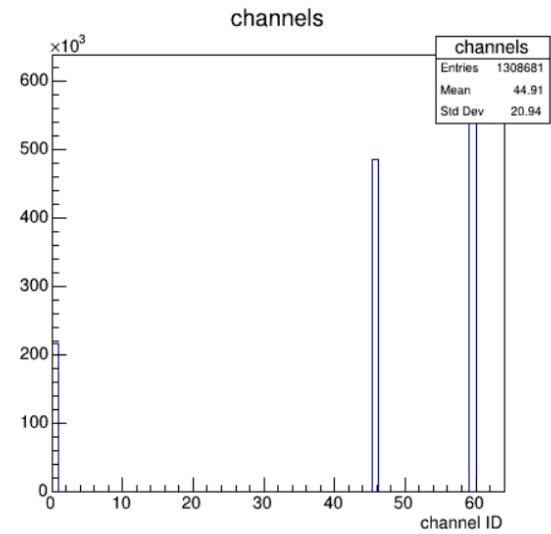
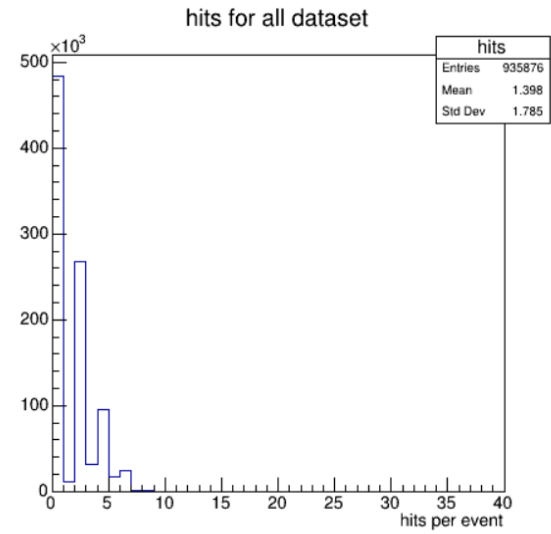


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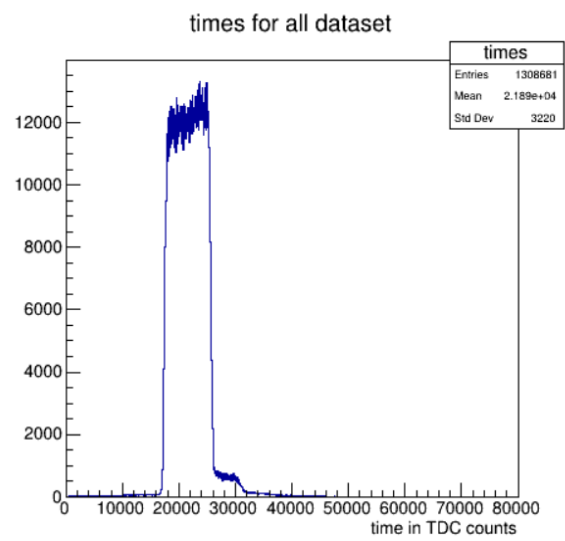
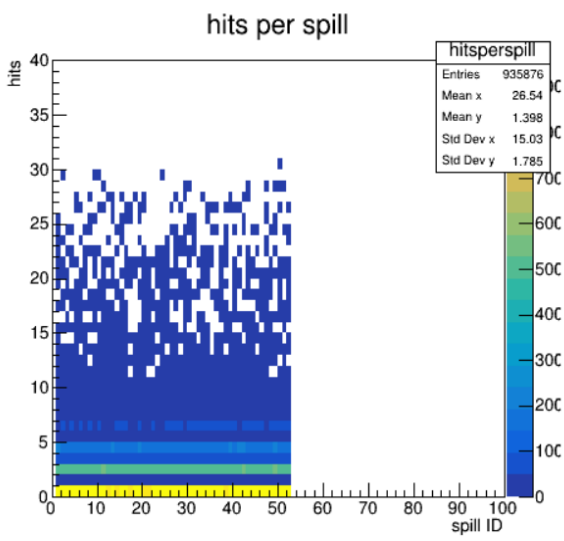
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FAST QA ANALYSIS



1 TDC count = 3 ps

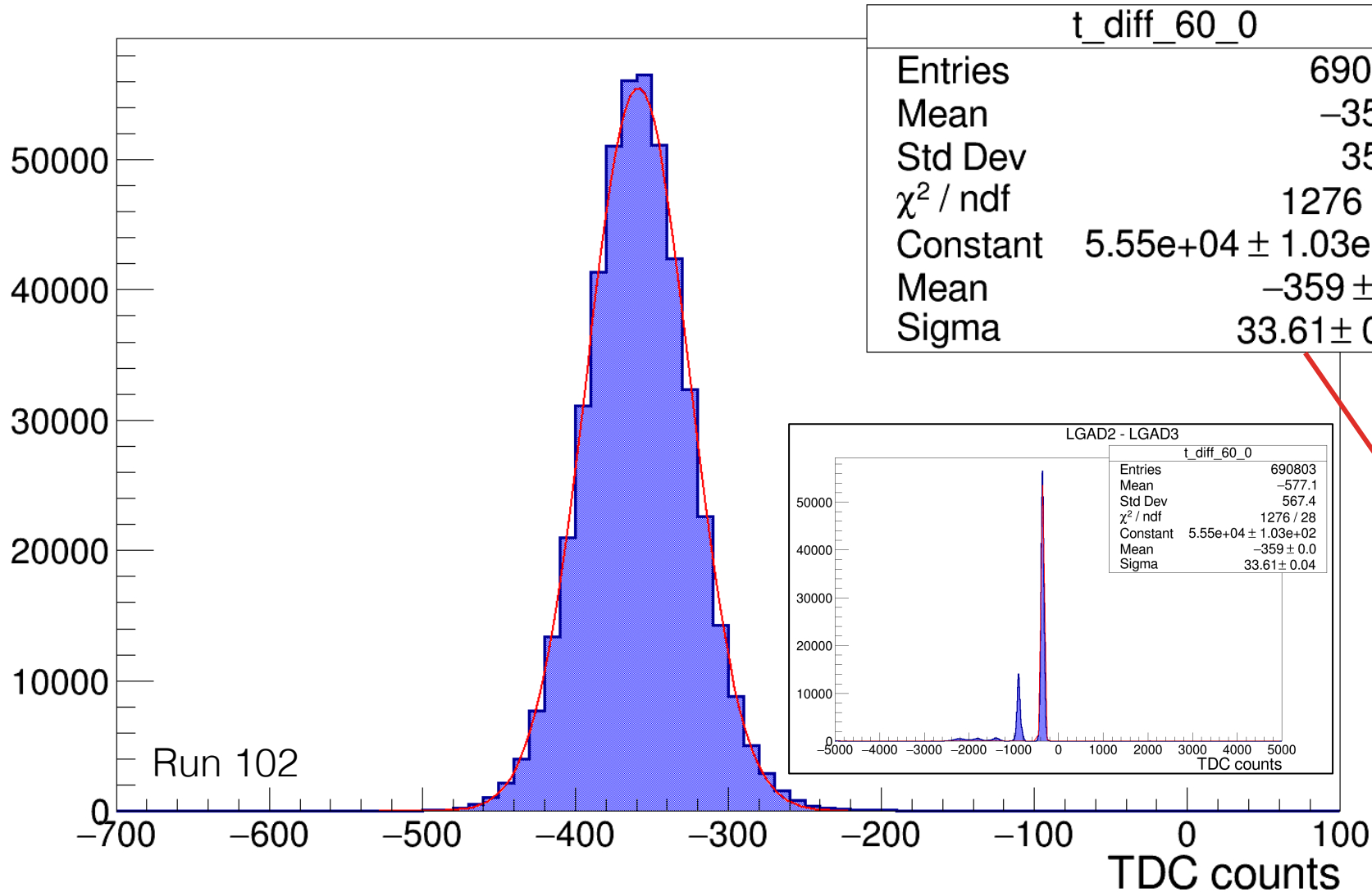


LGAD signals within the readout window and well discriminated (**OK**)

To be included:
hit multiplicity vs channel

FAST QA ANALYSIS

LGAD2 - LGAD3



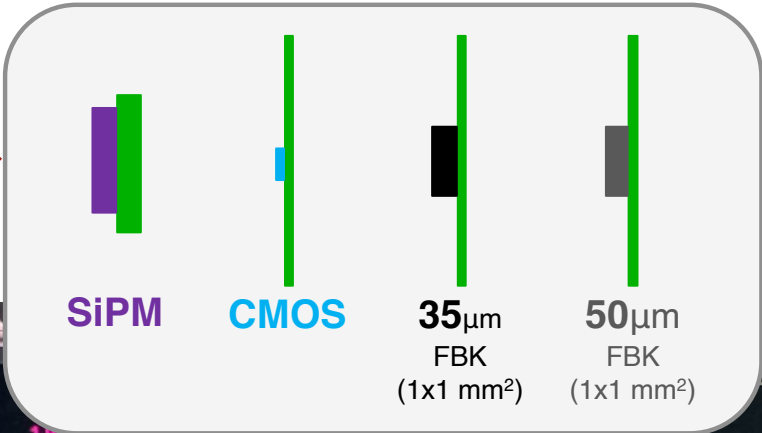
All contributions enter here (!)

- Sensor
- Amplification
- Discrimination (LIROC)
- Digitization (picoTDC)

The one of LIROC is substantial, picoTDC is few ps (*See Pietro slides*)

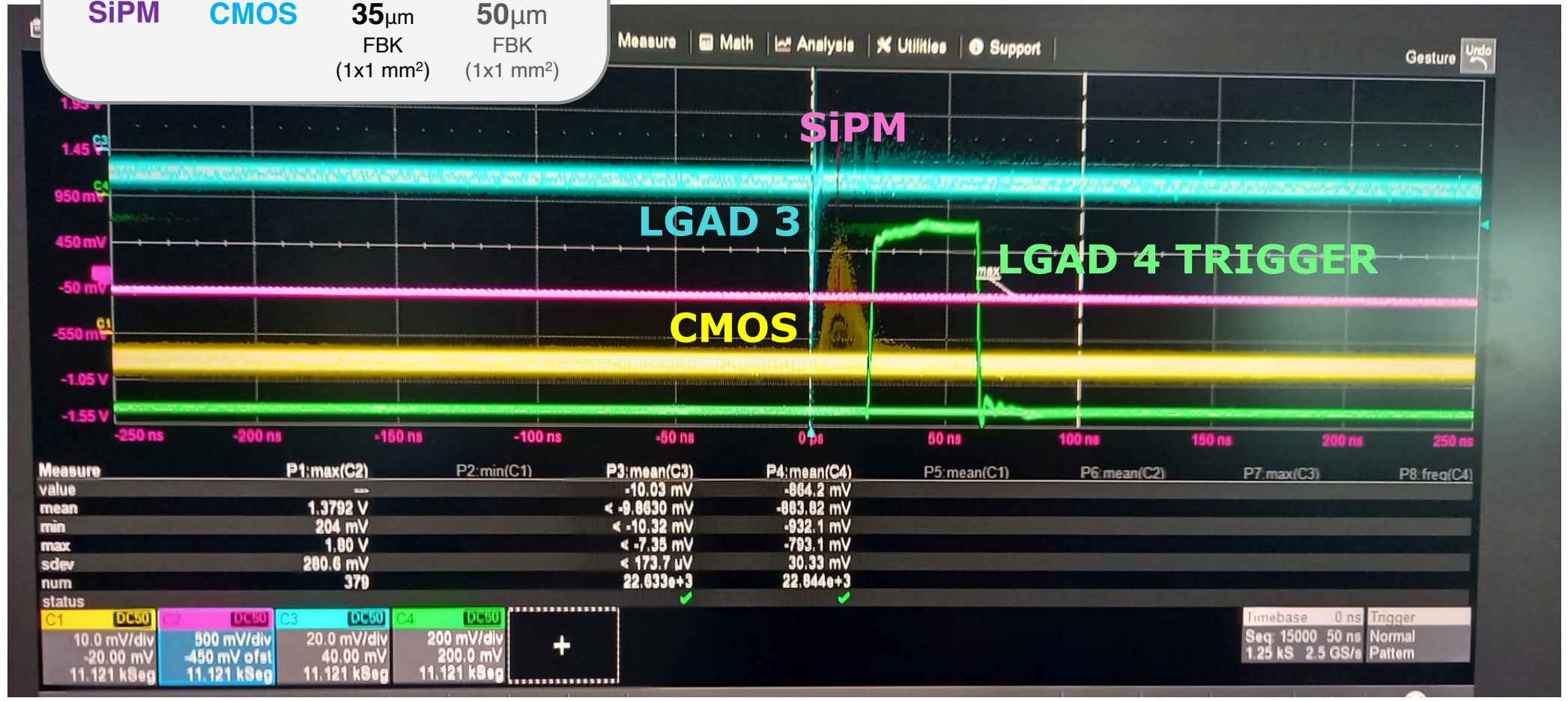
$$\sigma = 33 \times 3 = 99 \text{ ps}$$

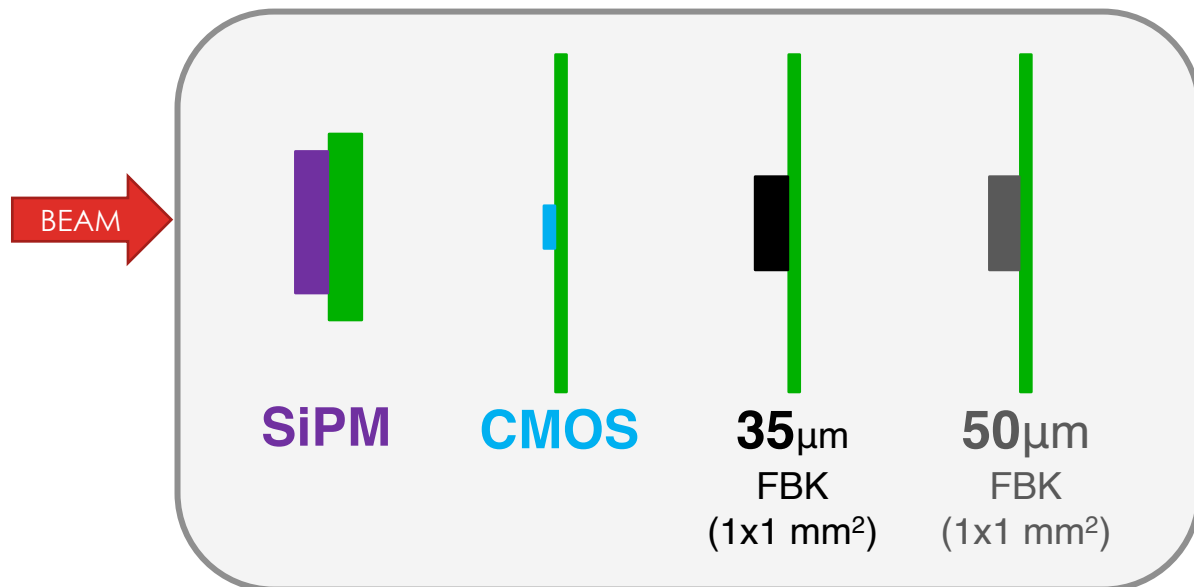
$$\rightarrow \sigma_{\text{DUT}} = 99/\sqrt{2} = 70 \text{ ps}$$



CMOS matrix 1a flavor A1

- Different top and bottom voltages





- SR1 (1 mm resin) Single
- SR1 (1 mm resin) Matrix
- SR3 (3 mm resin) Single

→ **Comparison**

- Different resins
- Matrix VS single

- Different voltages
- Different thresholds on picoTDC
- Different PA_Gain

OUTLOOK



- **Readout** with picoTDC extremely **stable** (thanks to the picoTeam!)
- **Fast QA analysis very helpful** → additional checks for the next beam test to be implemented
- Not easy to discriminate **positive** (CMOS, SiPMs) **and negative** (LGAD) signals on the same LIROC board → possibility of 2 LIROCs?
- **Data** to be analyzed, moved on:
`/eos/project/a/alice3timing/testbeams/2024_04`
- Other data included those of crosstalk effects still stored locally, including LIROC runs

Next Beam Test:

- *26 June – 10 July (already approved)*
- *16 October – 30 October (draft)*

Always main users without parasitics

Backup slides



ALICE



LGAD2 - LGAD3

