The Upgrade of the CMS tracker
Status and plans

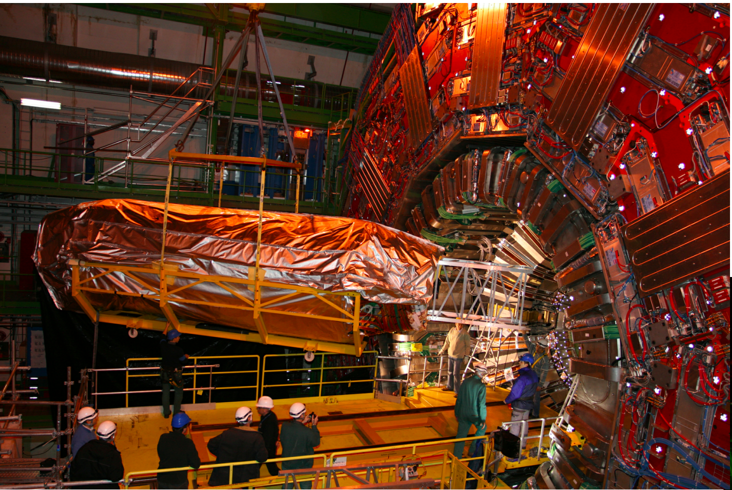
G. Bolla

PURDUE UNIVERSITY

bolla@cern.ch

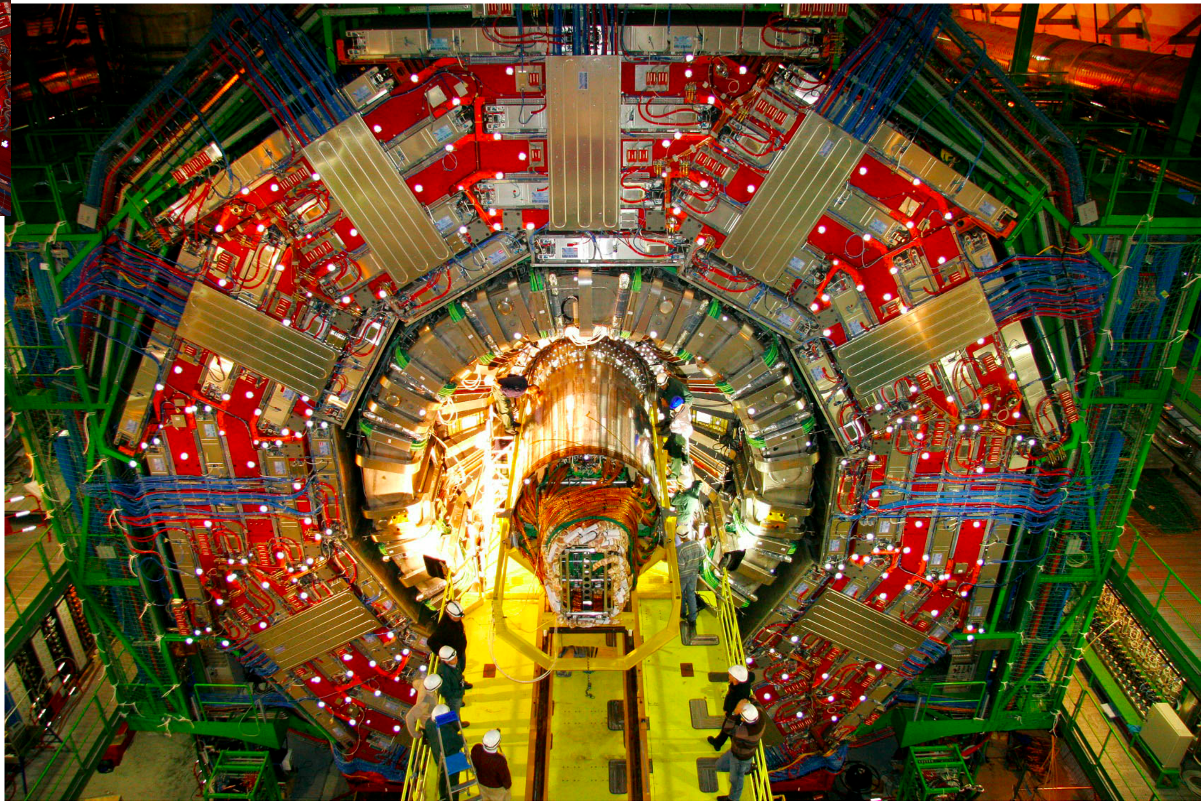
Let’s start from Xmas 2007

Not even 5 years ago in the CERN bulletin



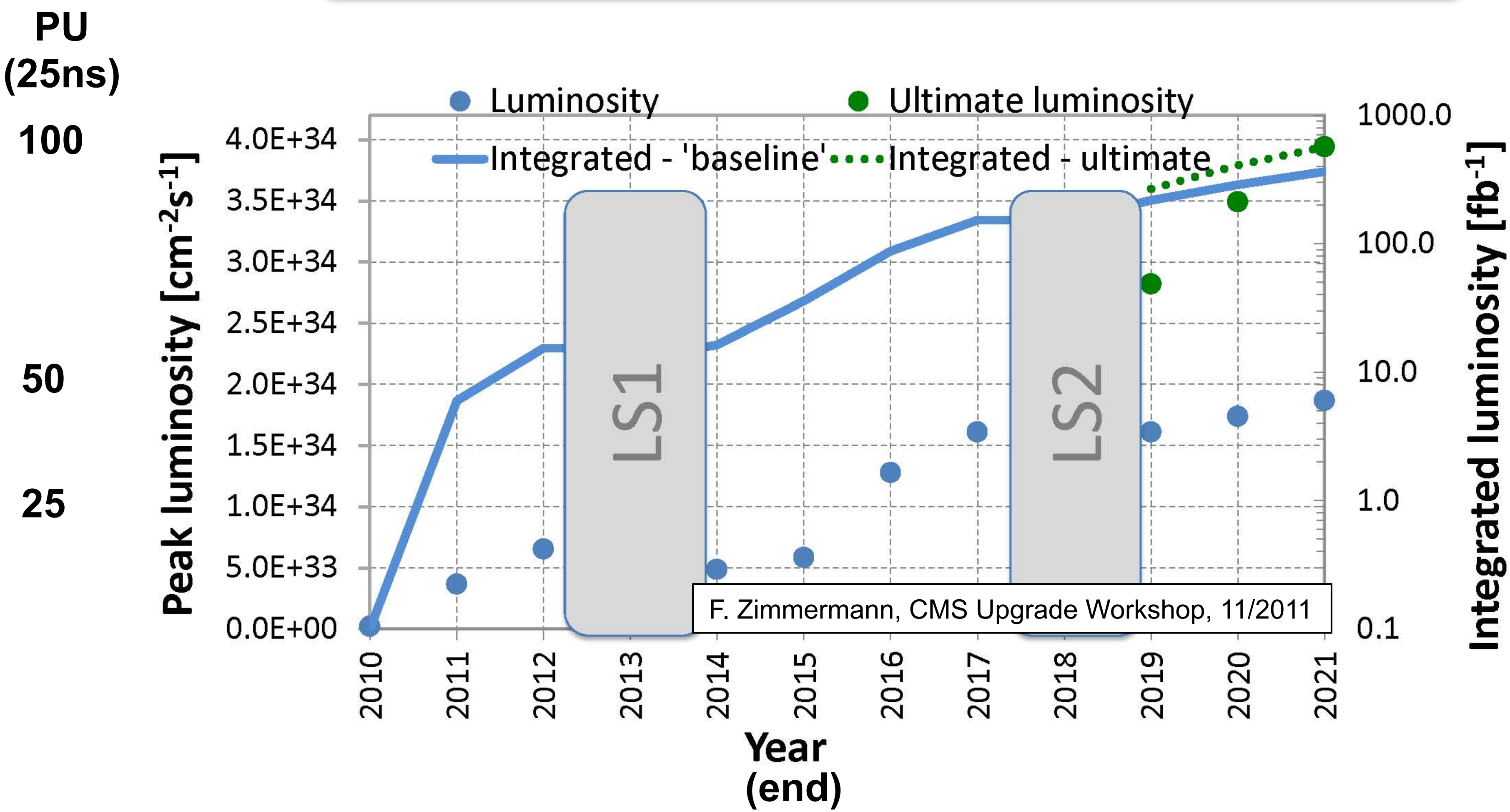
A silicon tracker for Christmas

The CMS experiment installed the world’s largest silicon tracker just before Christmas.



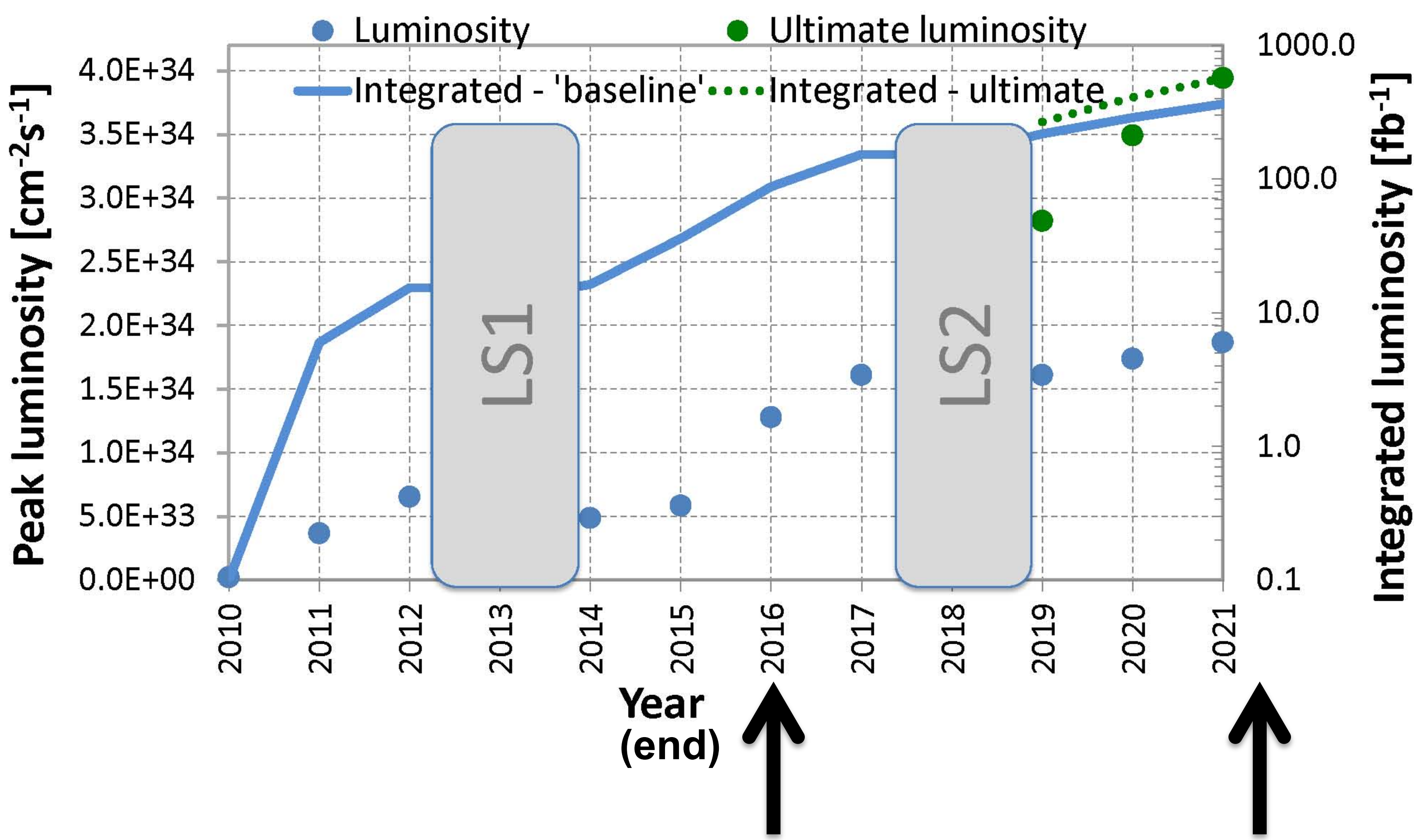
As of today the CMS tracker has integrated ~10 fb^{-1} of the ~500 it was built for.
The performance are excellent (see **poster** by P. Merkel) but the luminosity forecast of the LHC drives an upgrade plan to be deployed in the next decade.

LHC schedule for the next decade



The third Long Shutdown LS3 is not yet on the map. It is assumed to happen in 2022.

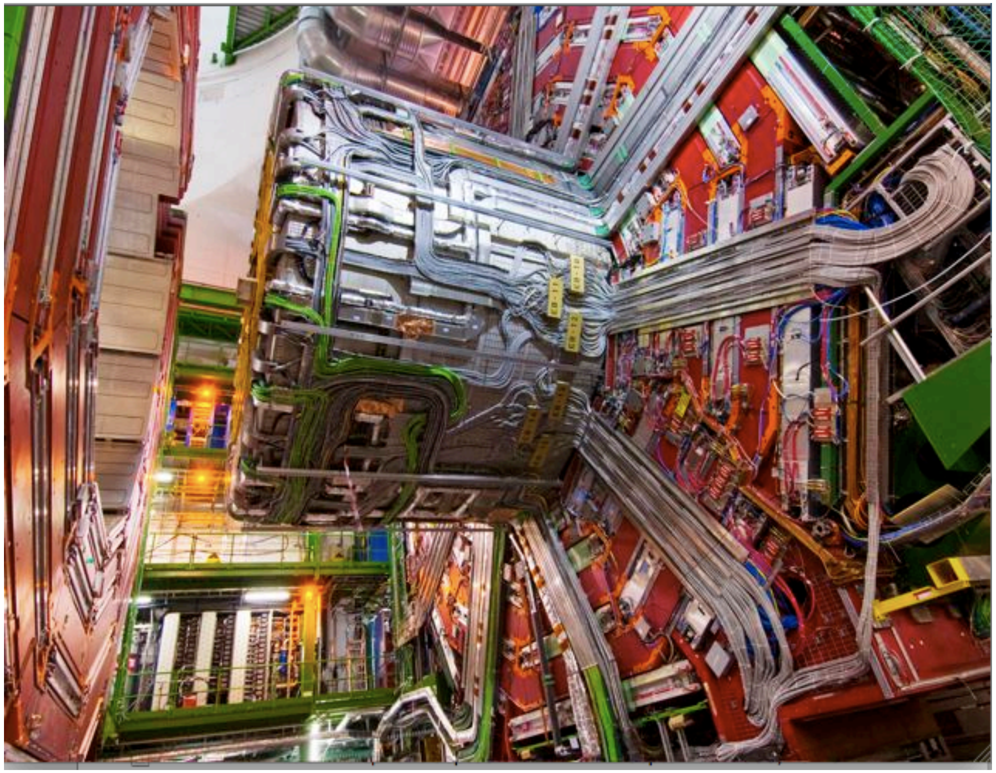
CMS Tracker plans for the next decade



At the end of 2016 we plan to replace the CMS Pixel Detector (**Phase 1**)
During LS3 (2022 onward) we plan to replace the wholes CMS Tracker (**Phase 2**).

Important boundary conditions

- The upgrade plan needs to develop within an important boundary condition
  - Must re-use services from balconies to detector "PP1" patch panel
  - Cooling pipes
  - Power cabling
  - Optical cabling
- Pixels and Tracker cables and pipes buried under ECAL/HCAL services



It is not trivial to increase the granularity by an order of magnitude maintaining the same power consumption and the same number of readout fibers.

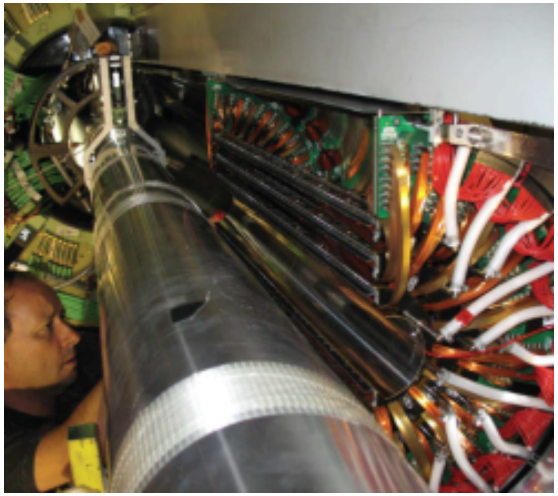
First Challenge: $\mathcal{L}$ > 1E34 cm^{-2}s^{-1} → Phase1

The **readout** of the present pixel system was designed for nominal LHC conditions of

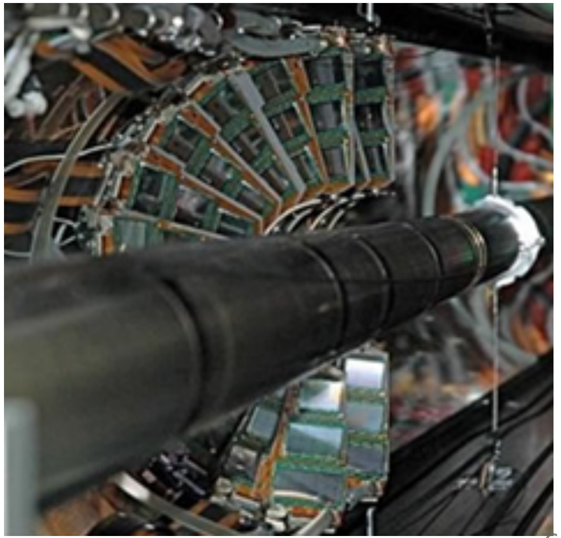
$\mathcal{L} = 1 \bullet 10^{34}$ cm^{-2}s^{-1} and 25ns bunch spacing

We expect **unacceptable data losses** for higher instantaneous luminosity:

- $\mathcal{L} = 2 \bullet 10^{34}$ cm^{-2}s^{-1} and 25 ns → ~16% **data loss** for BPIX layer-1
- $\mathcal{L} = 2 \bullet 10^{34}$ cm^{-2}s^{-1} and 50 ns → 50% data loss in BPIX-L1, and large losses for L2 and L3 also



Pixel seeded tracking and vertexing are essential for almost all physics analysis. Significant deterioration is physics reach without an upgrade of the pixel system.

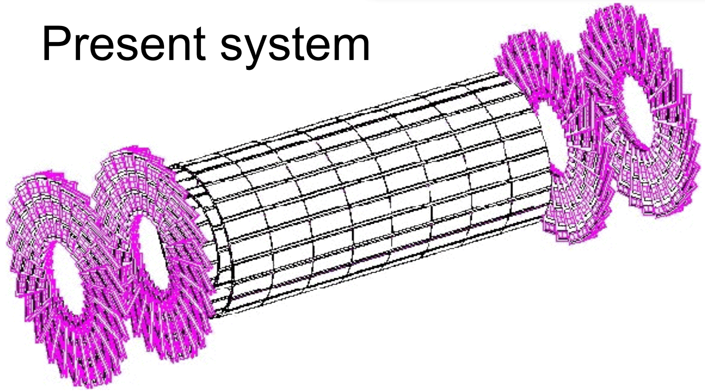


Further improvements:

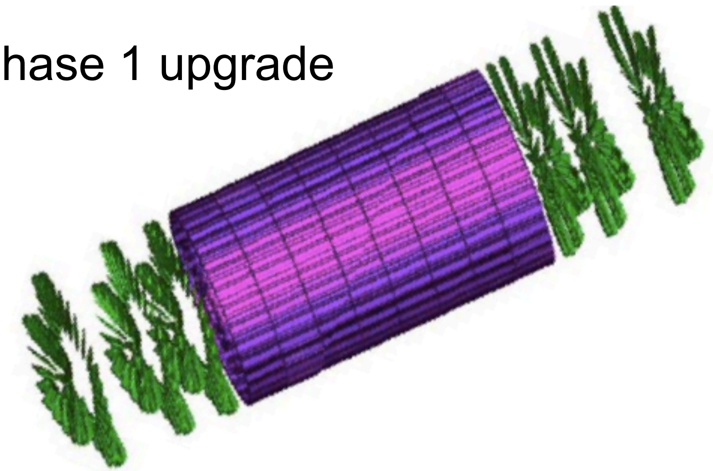
- Minimize material budget
  - New 2-phase cooling system
- Add a 4th layer
  - Move the innermost one closer to the new beam pipe

The proposed Phase 1 Pixel Upgrade

Present system



Phase 1 upgrade



Pixel size remain the same 100x150 μm

Barrel:

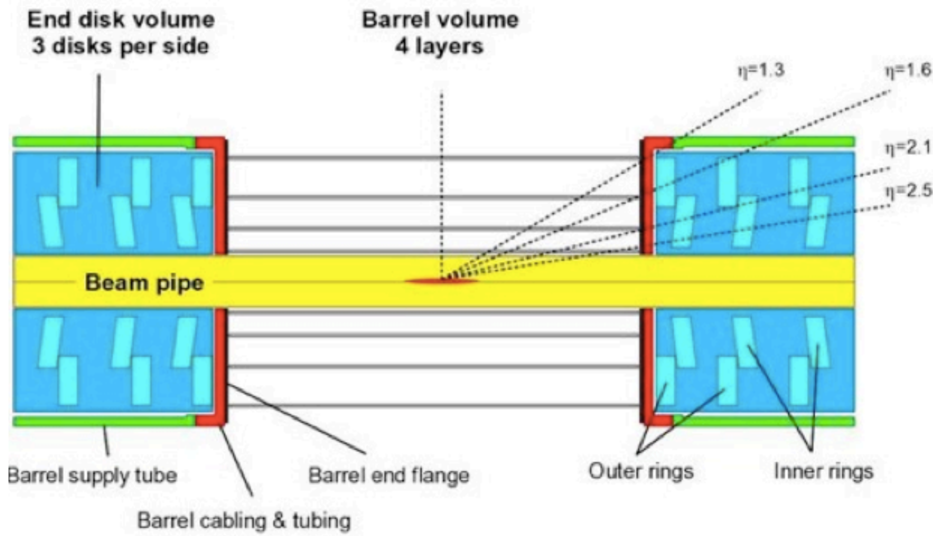
- from 3 to 4 layers
- 48 Mpix → 80Mpix

Endcap

- from 2 to 3 disks
- 18 Mpix → 44 Mpix

Overall: 66 Mpix → 124 Mpix

Obvious benefits of additional hits but 2 times the number of pixel with double the rates to be powered/readout/cooled with the same services.



The project need a New Readout Chip

<u>Higher rate capability</u>

- Larger L1 latency buffers with denser layout to reduce trigger latency related data losses.

- Additional readout buffer stage to lower readout related data losses

<u>Increase readout bandwidth</u>

- Change readout to digital scheme

<u>Increased radiation tolerance of the system</u>

- Lowering operational signal threshold
    - Lower threshold translates directly into longer lifetime of detector (as radiation damage decrease the charge from the silicon sensor)

<u>Miscellaneous</u>

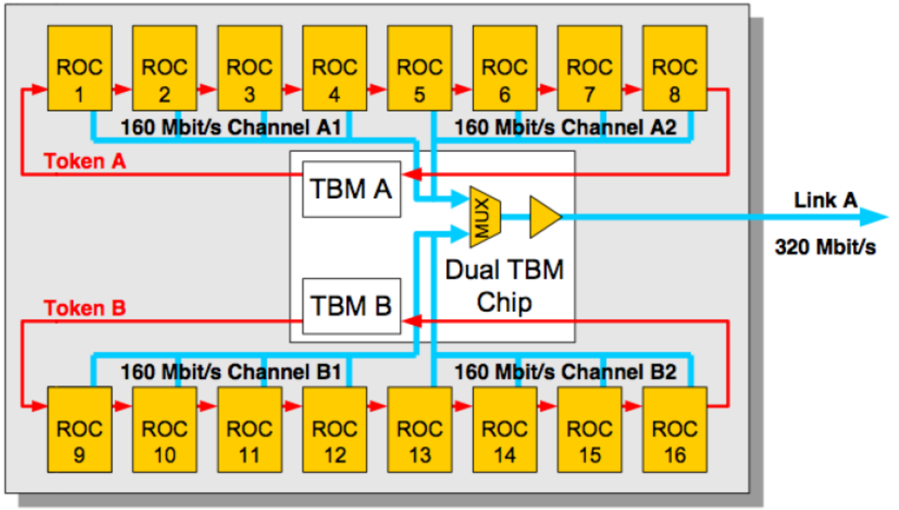
- Operational improvements
- Further optimization of current consumption

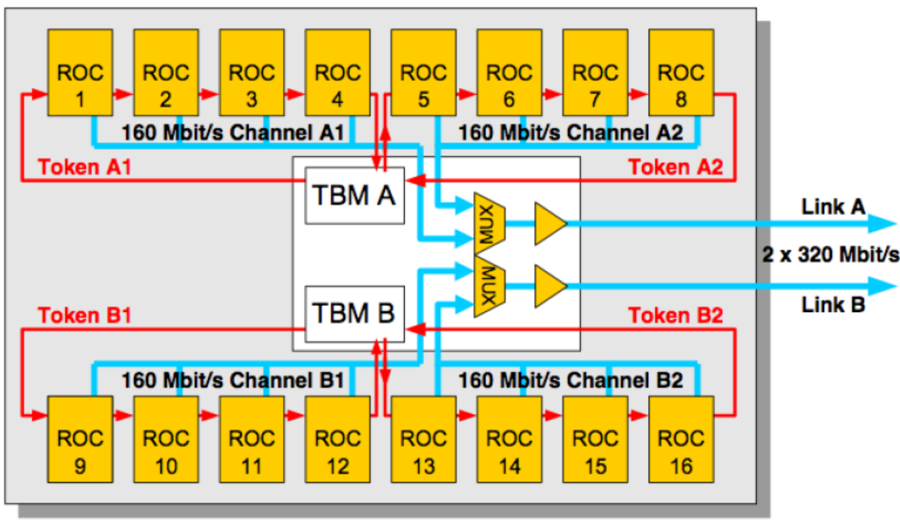
New digital data transfer

- Limited number of fibres in system.
  - Need faster optical links
    - Have to drop present analogue readout

- Two different readout schemes of a new module.
  - Standard scheme (upper) has one data link. Two ROC readouts (A and B) run in parallel.
  - For higher data rate in the innermost layer a module has two data links (lower). Four groups of four ROCs each can be read out in parallel.

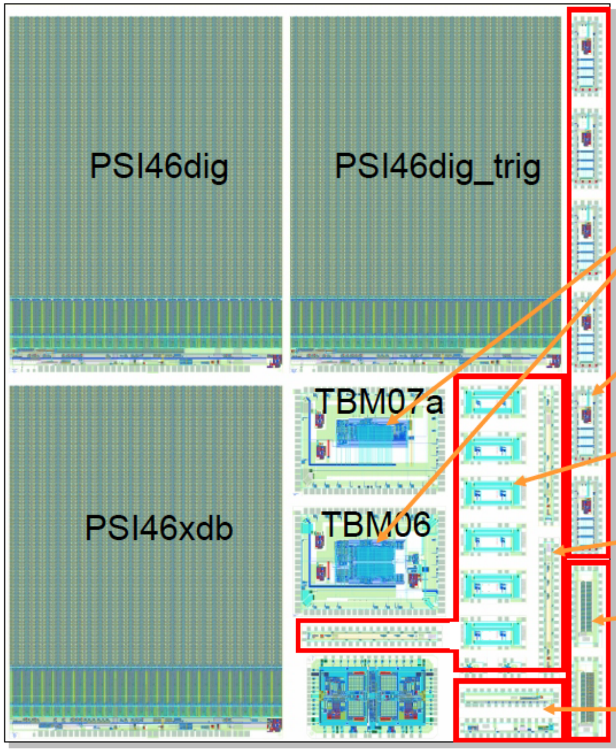
- Besides new digital ROC, several other new ASICs and boards needed for digital readout:
  - new Token Bit Manager (TBM)
    - Controls and reads out modules
  - Digital Level Translator (DLT)
    - To interface to POH
  - new Pixel Optohybrid (POH)
    - Laser carrier with laser driver.
  - new (or modified) Front-end driver (FED)
    - Off detector data receiver and processing board





A new chip is now in hand

- Two step development under way at PSI Villigen
  - 2011/12:'PSI-46dig'
  - Modifying periphery of existing analogue ROC
    - Bigger buffers
    - Digital readout: 8bit ADC, 160MHz
    - Other improvements, 5 metal layers to 6
      - improved x-talk
      - threshold reduction
- 2012/13 next iteration
  - Aiming for even better efficiency
    - Deeper re-design, touching also column-drain architecture



Size: 17.4 mm x 21.2 mm

3 new ROC versions (PSI)

2 new TBM versions
Ed Bartz, Rudgers

LCDS cable drivers with bug fixed in read back (PSI)

Digital Level Translator DTL to replace the ALT chip (PSI)
Christoph Nägeli

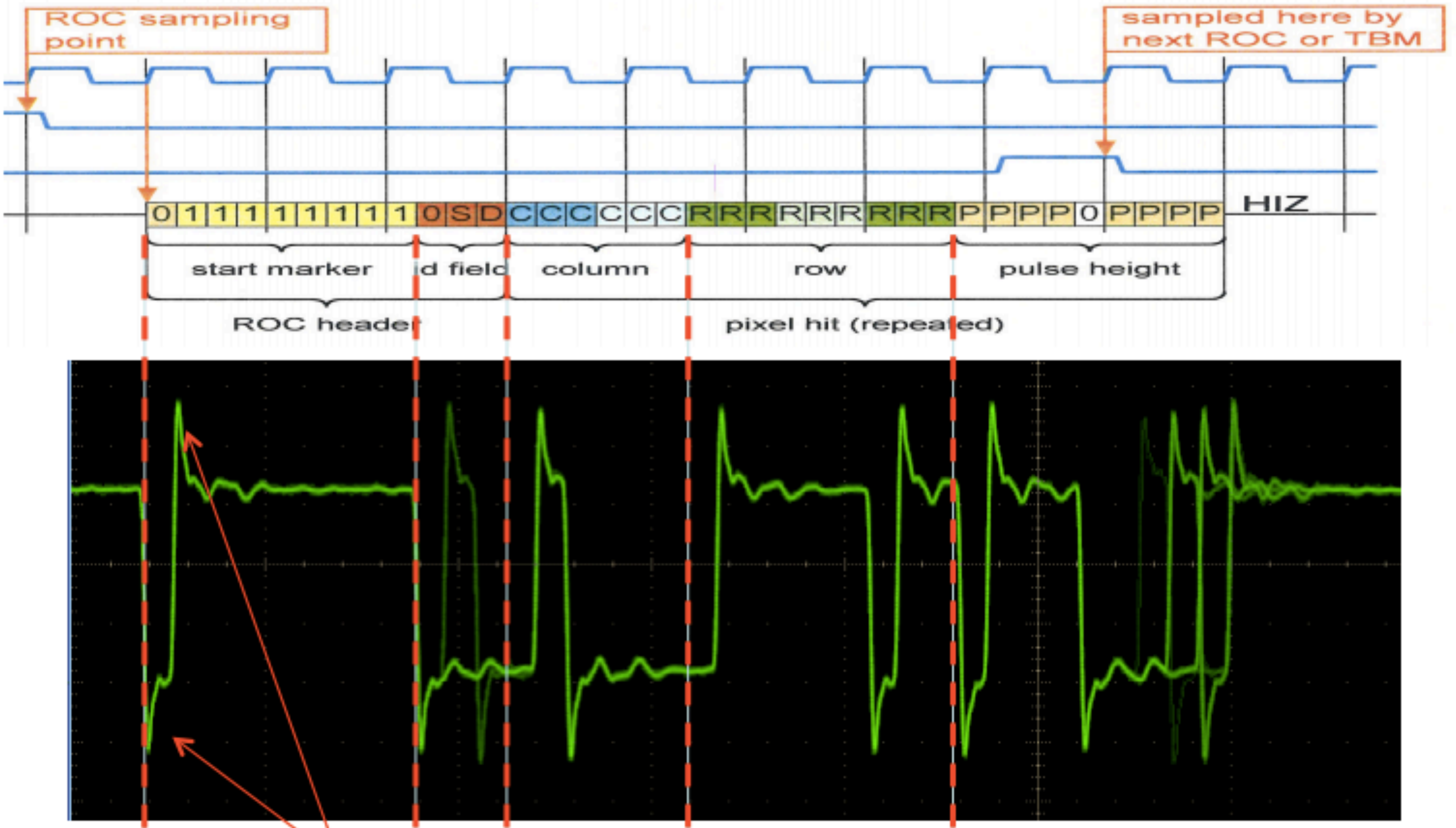
LCDS/LVDS converter for test setups (PSI)

SEU resistent register test structures (PSI)

ADC, PLL and oscillator test structures (PSI)

This reticule was received a few weeks ago and it works

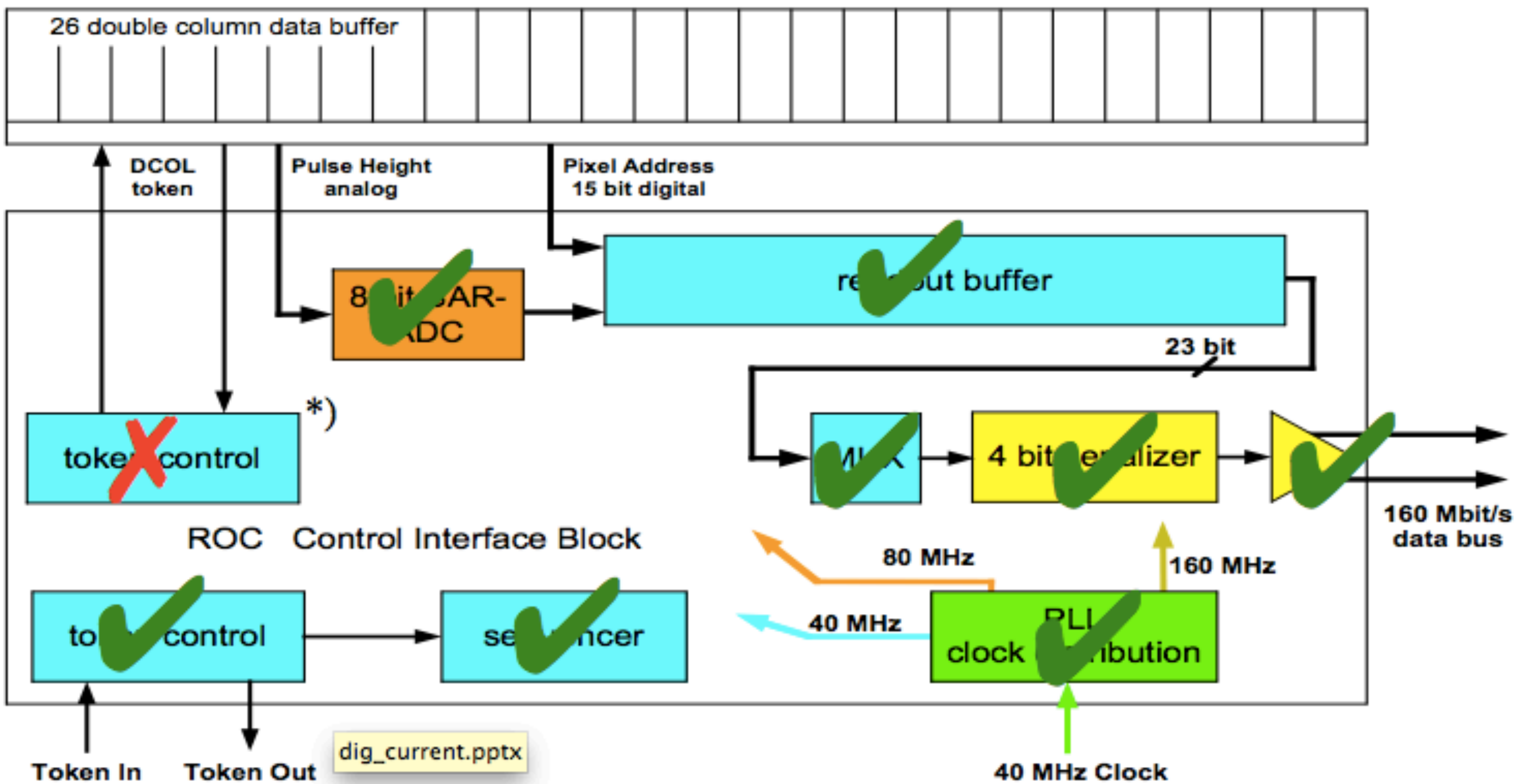
Digital data format



Spikes are artefact of non-ideal test setup

Scope picture

Modified circuitry in ROC periphery



Most of new logic blocks and new clock frequency domains work very good.

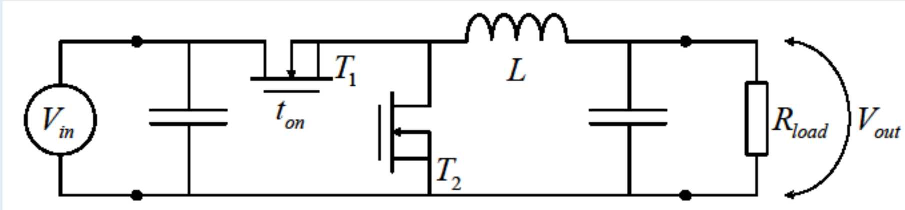
Power distribution

The readout chip power consumption of the new ROC is foreseen to be the same as the present one. With twice the number of pixel we need to bring in twice the power using the same cables.

Unsustainable voltage drops along the cables →

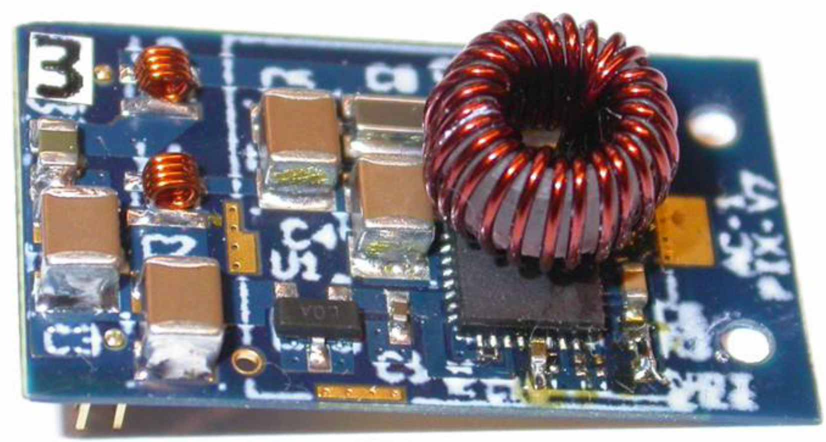
- Use DC-DC conversion to provide 2.5V and 3.3V to modules
  - Compatible with present powering/ safety system scheme
  - Can proceed with relatively small modification to existing power supplies
    - Raising LV output of CAEN A4603 to 12V
  - Will need eventually to replace power supplies to cover situation at highest luminosity and fluences

"Buck" converter



Idea: $P = U \cdot I = (rU) \cdot (I/r)$ with conversion ratio $r > 1$

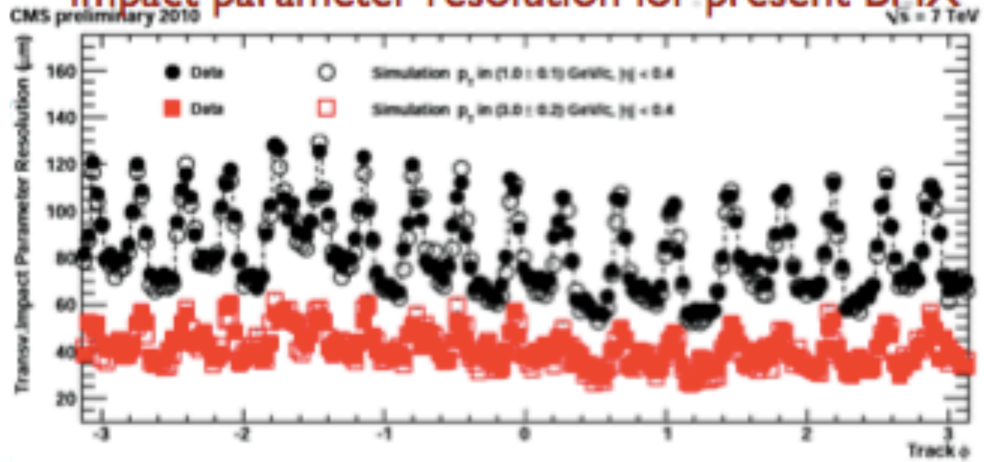
Duty cycle $D = t_{on}/T$; $1/D = I_{out}/I_{in} = V_{in}/V_{out} = r$



prototype converter with AMIS2 ASIC.
Efficiency: ~75% for V_{OUT}= 2.5 V, ~80% for V_{OUT}= 3.3 V

A new cooling system

Impact parameter resolution for present BPIX



Present Pixel uses mono-phase C6F14 cooling system that gives a sizeable contribution to the material budget that is quite visible in the impact parameter resolution versus the Phi of the track (peaks correspond to the location of the cooling pipes).

The upgrade will use two-phase CO_2 cooling (2PACL method = 2-Phase Accumulator Controlled Loop)

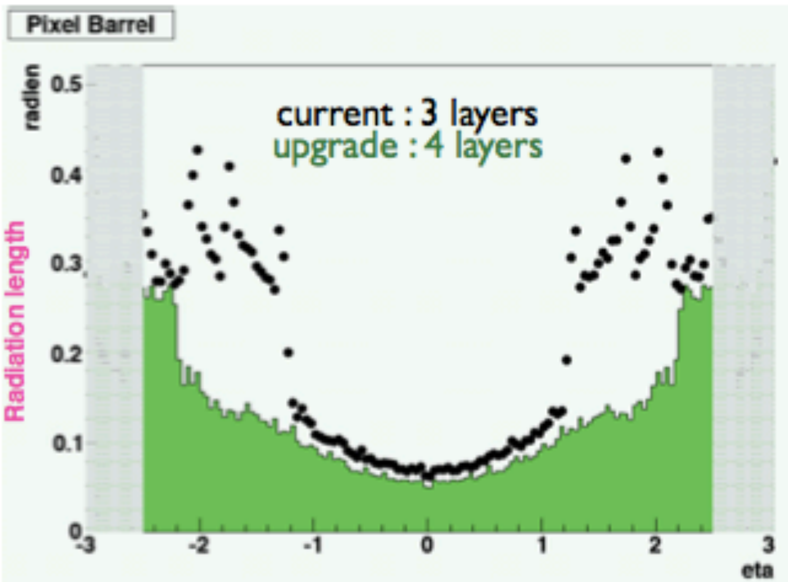
- High heat transfer coefficient;
- More heat load per channel
- Smaller cooling pipe (1.6/1.8 mm ∅)
- But higher pressure operation (up to 70 Bar)
    - Present pipes from balconies to tracker volume are adequate.

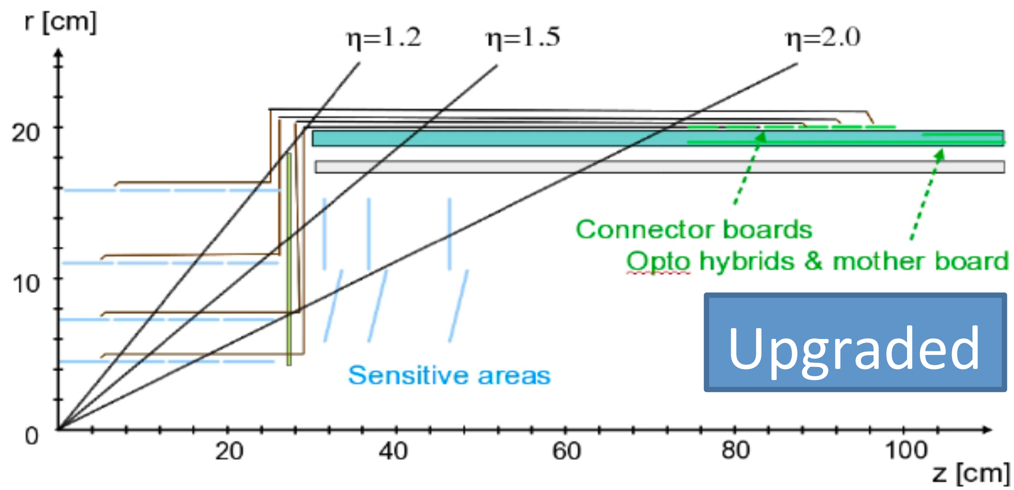
Weight Layer1 51g + 11g

CO_2 → 40% of old first layer

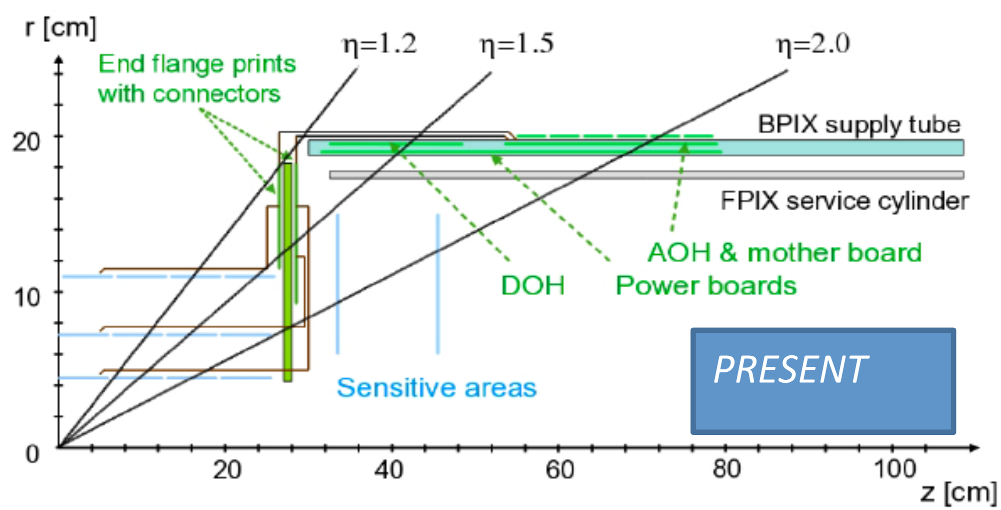
Phase 1 Pixel: material budget

- Lot of services material moved out of tracking region
- New ultra-light mechanics
- CO_2 cooling





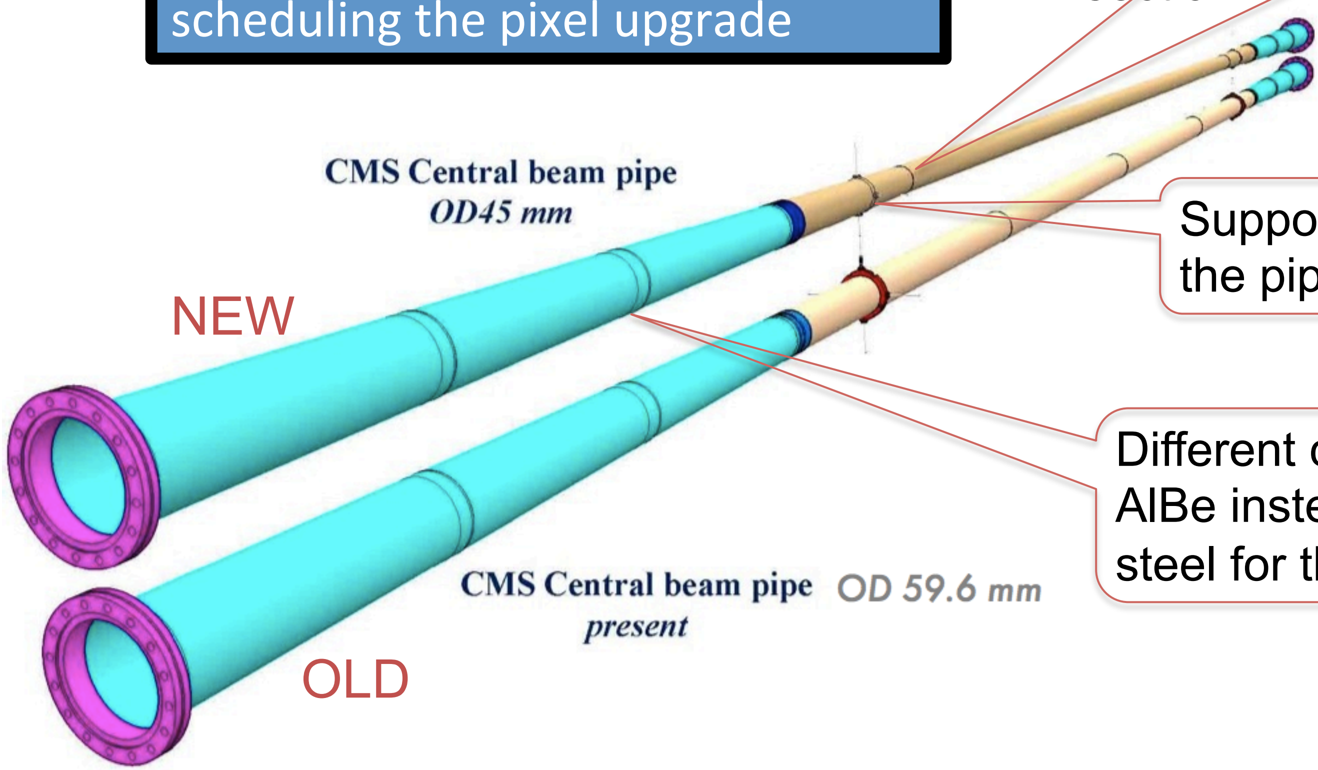
for illustration only - Now moving BPIX L1 to 30mm



2 times the number of pixel with less material (especially in the forward region)

From a new smaller beam pipe

Beam pipe installation foreseen in LS1 to allow most flexibility for scheduling the pixel upgrade



To a smaller radius for the innermost pixel layer

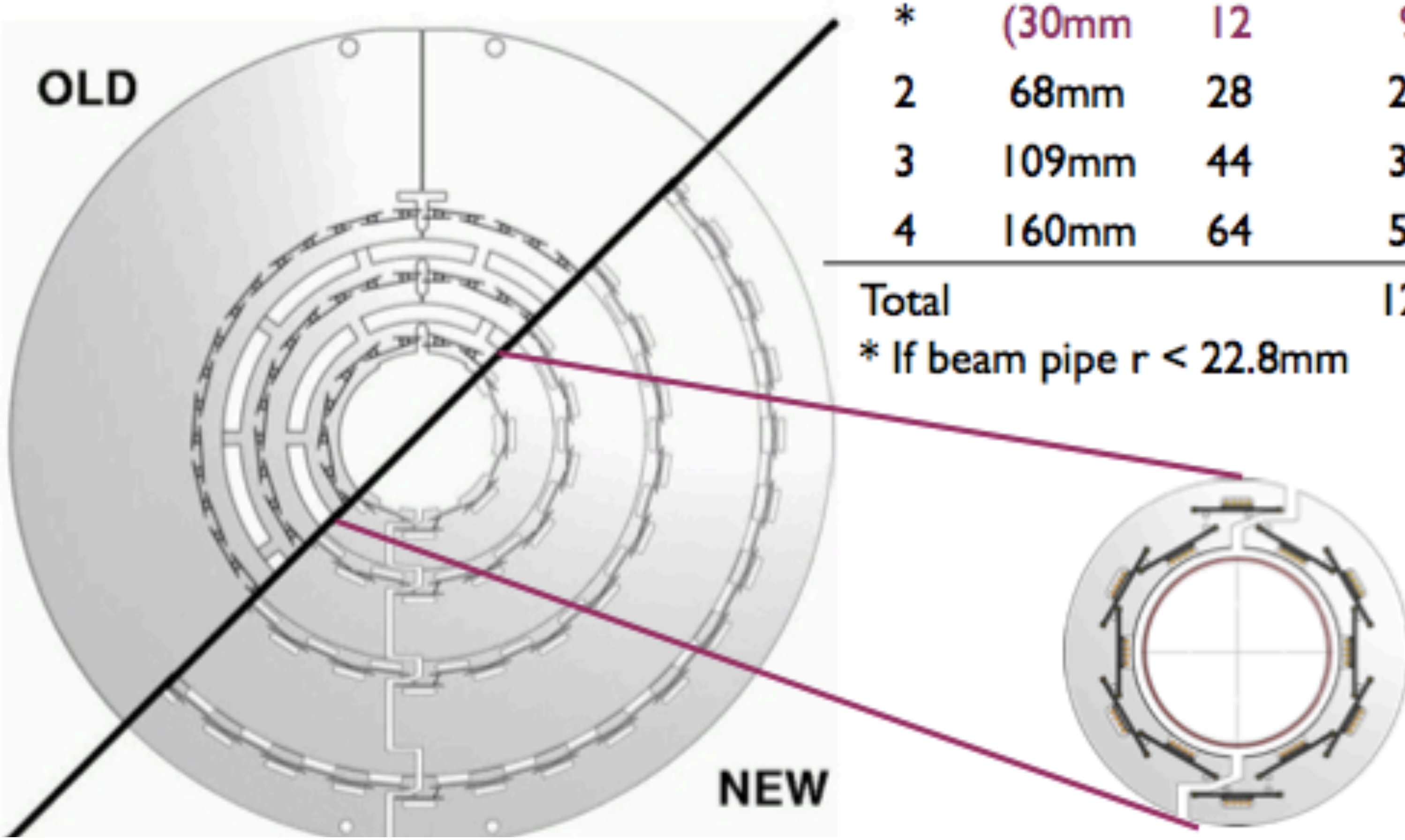
We are moving from a 18 faces 39 mm geometry to a 30 mm and 12 faces geometry with further improvements on b-tagging performances

- Two identical half shells with one type of module

Layer	radius	# faces	# modules	# ROCs
1	39mm	16	128	2048
*	(30mm	12	96	512)
2	68mm	28	224	3584
3	109mm	44	352	5632
4	160mm	64	512	8192
Total			1216	19456

* If beam pipe r < 22.8mm

19456 → ~81M pixels

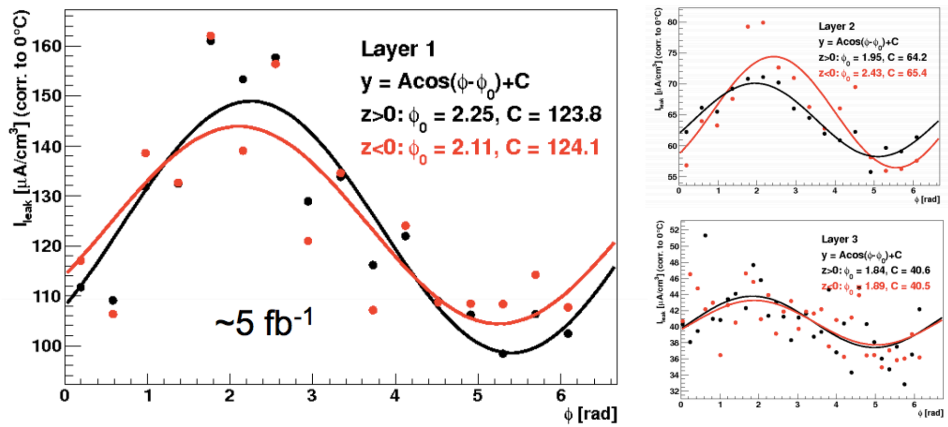


A new insertion tool

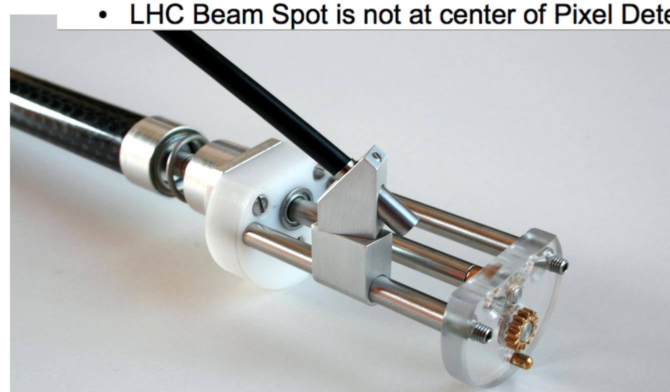
Smaller radius imply smaller tolerances for alignment

- Radiation exposure is strongly dependent on beam-pixel alignment.
- BPIX clearance around beam-pipe only 2mm
  - Also beam pipe off-centred
  - Needs a precisely adjustable insertion mechanism

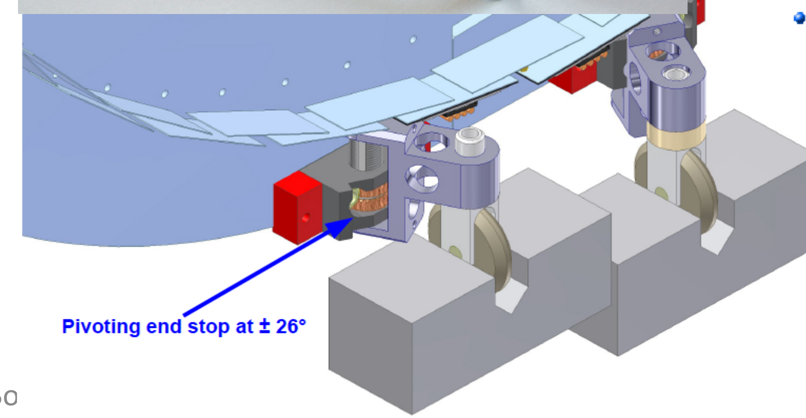
- Dedicated tooling developed
  - Wheels with worm gear adjustment run in insertion rails
  - Adjustment rod with in-built camera for engaging worm gear



- LHC Beam Spot is not at center of Pixel Detector!



- Note: Lower wheel set has two worm gears.
- One for lifting/lowering of the BPIX and one for moving towards/away from beam pipe



What is next ~2021 onward

Bla bla

Phase 2: $\mathcal{L}=10^{35}cm^2s^{-1}$

Full Tracker Upgrade

A new CMS tracker: Phase 2

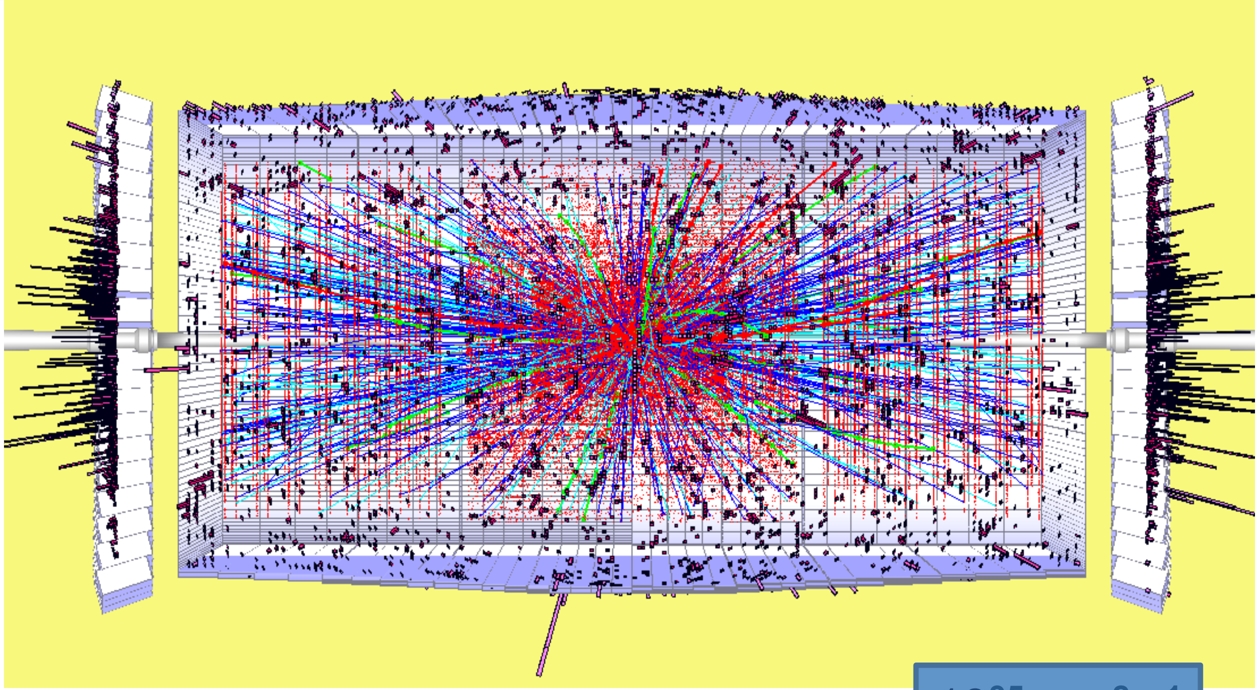
Hundreds of collisions per bunch crossing.

10 times the radiation flux

Require higher granularity to maintain occupancy at the % level and in general the tracking performance of the present detector in the more dense environment.

Still has to be serviced by the same pipes, cables and fibers as the present one.

And…
It will be an important tool to keep the trigger rates at L1 below 100 kHz.



10^{35} $cm^{-2}s^{-1}$

An excellent detector will be essential……
…..even better than current Tracker!
The layout is not yet final but there is clear progress on developing building blocks for a new tracker.

Title here Phase 2

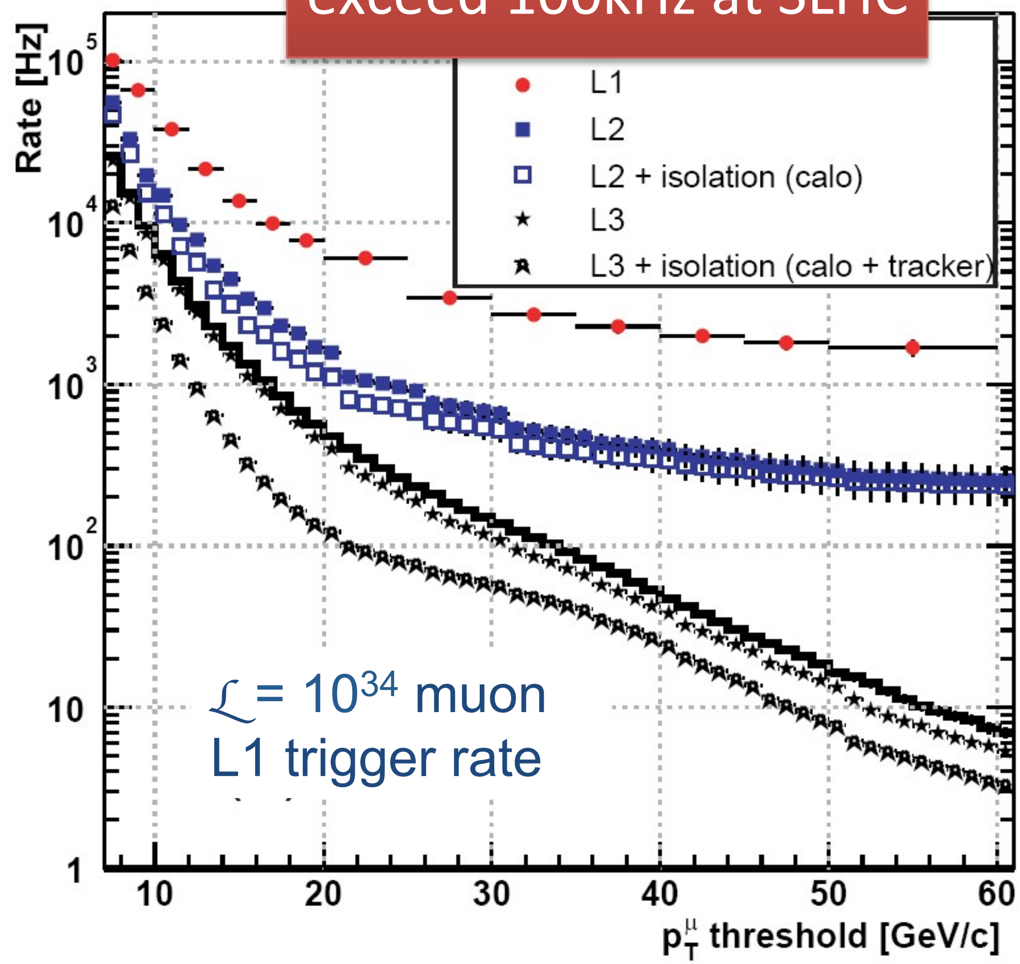
Single *μ, e and jet* L1 trigger rates will greatly exceed 100kHz

- Tracker data appears to be only extra info capable of improving selectivity
  - can increase latency, to 6.4μs, but must maintain 100kHz for compatibility

Impossible to transfer all data off-detector for decision logic

- on-detector data reduction (or selective readout) essential
  - eg ~0.5% occupancy at R ≈ 25cm at $10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ in 2.5mm x 100μm pixels
  - => ~20Mpix x 24bits => ~96,000 Gb/s
- Large fraction of low p_T tracks
  - not useful for trigger
  - conceptually simple to measure
- Trigger functions must not degrade tracking – material, power

μ, e and jet rates exceed 100kHz at SLHC

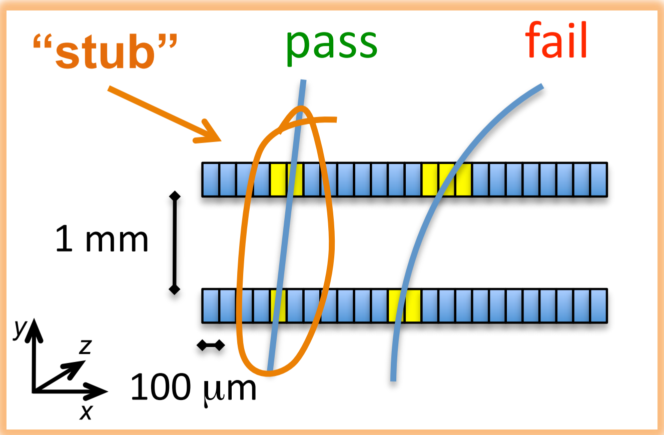


General concept

- Silicon modules provide at the same time “Level-1 data” (@ 40 MHZ), and “readout data” (@ 100 kHz, upon Level-1 trigger)
- Level-1 data require local rejection of low-p_T tracks
- Design modules with p_T discrimination (“p_T modules”)
  - Correlate signals in two closely-spaced sensors (exploit the strong magnetic field of CMS)

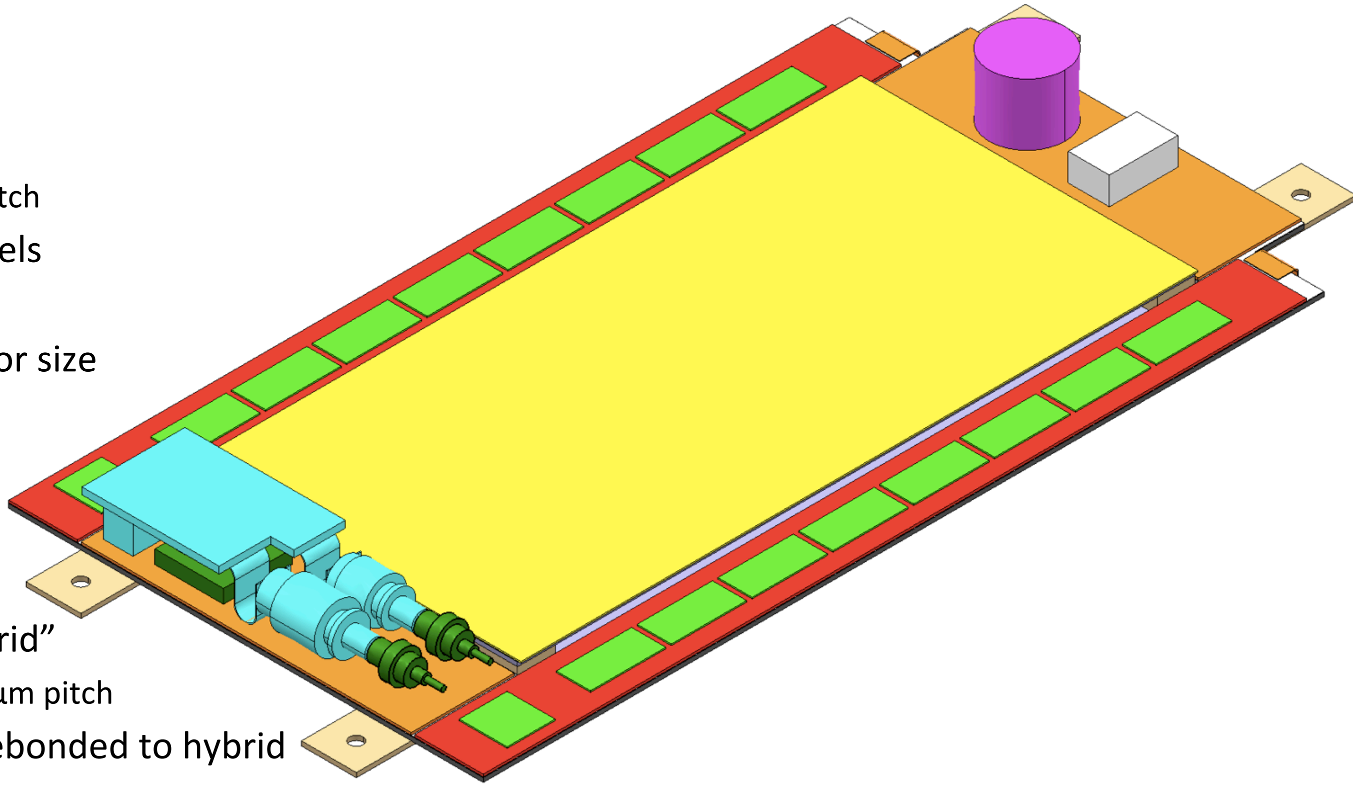
Infrastructure:

- Take advantage of the technologies already used in the phase 1 upgrade for the services:
  - Low mass CO2 cooling
    - With associated mass reduction.
  - DC-DC converters for power distribution.
- Data readout
  - Fast optical links developed at CERN.
    - g



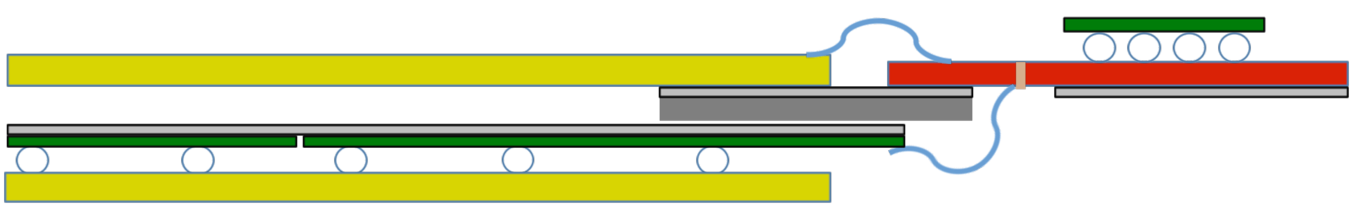
A possible (pixel strip) module

- Sensors:
  - Top sensor: strips
    - 2×25 mm, 100 µm pitch
  - Bottom sensor: long pixels
    - 100 µm × 1500 µm
  - ≈ 5x10 cm^2 overall sensor size



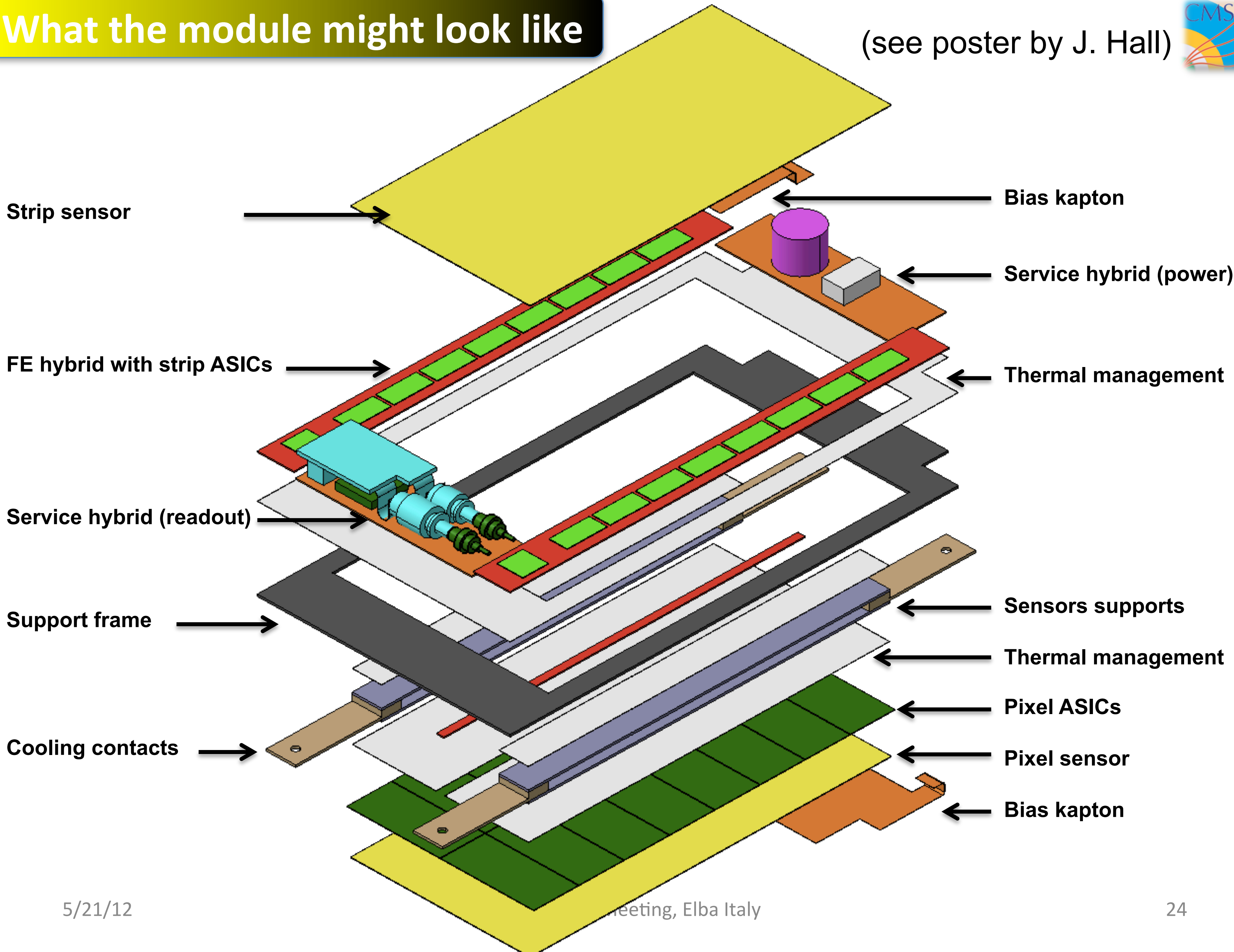
- Readout:
  - Top: wirebonds to "hybrid"
    - 1 wire per strip, 100 µm pitch
  - Bottom: pixel chips wirebonded to hybrid
    - 2 wires per pixel row, 50µm pitch
  - Correlation logic in the pixel chips
  - C4 bump-bonding

Different approaches exist see **poster** by J Hall on the CBC ASIC



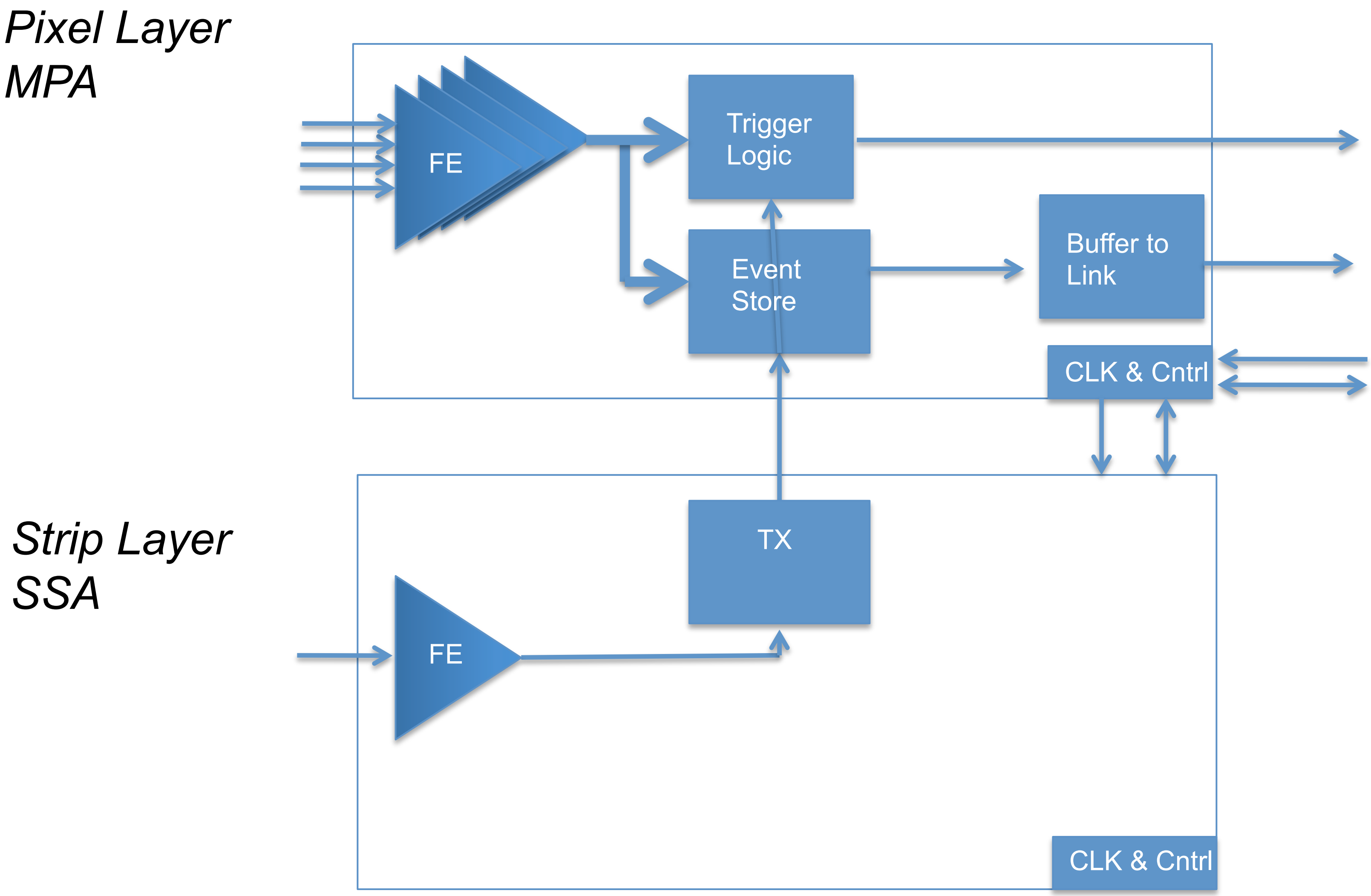
What the module might look like

(see poster by J. Hall)



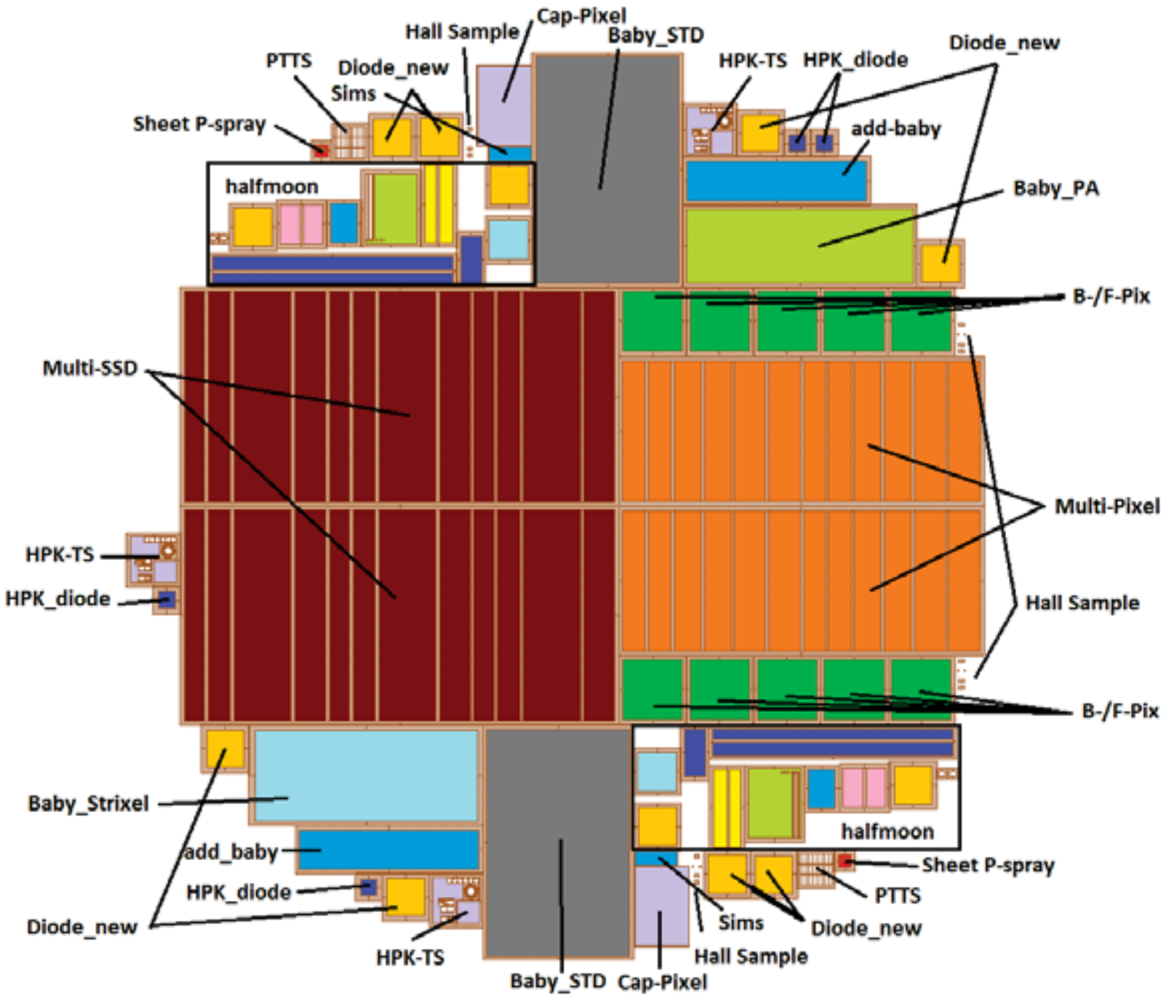
Module functional block diagram

- Coincidence and data handling in the pixel ASIC



Phase 2 sensor development

Extensive work on development of sensor in the last two years via a 6 inch production with HPK.



Substrate types:
FloatZone (FZ),
Magnetic-Czochralski (M)
Epitaxial (E).

p-in-n (N-type)
n-in-p (p-stop) (P-type)
n-in-p (p-spray) (Y-type)

p-in-n (double metal)
n-in-p (p-stop; double metal)
n-in-p (p-spray; double metal)

Different silicon thickness being explored

Phase 2 data links

Whenever possible take advantage of common efforts.
http://cdsweb.cern.ch/record/1235836/

Article

Title	**The GBT Project**
Author(s)	Moreira, P (CERN) ; Ballabriga, R (CERN) ; Baron, S (CERN) ; Bonacini, S (CERN) ; Cobanoglu, O (CERN) ; Faccio, F (CERN) ; Fedorov, T (Southern Methodist U.) ; Francisco, R (CERN) ; Gui, P (Southern Methodist U.) ; Hartin, P (Southern Methodist U.) *Show all 17 authors*
In:	TWEPP-09: Topical Workshop on Electronics for Particle Physics, Paris, France, 21 - 25 Sep 2009, pp.342-346
Subject category	Engineering
Abstract	The GigaBit Transceiver (GBT) architecture and transmission protocol has been proposed for data transmission in the physics experiments of the future upgrade of the LHC accelerator, the SLHC. Due to the high beam luminosity planned for the SLHC, the experiments will require high data rate links and electronic components capable of sustaining high radiation doses. The GBT ASICs address this issue implementing a radiation-hard bi-directional 4.8 Gb/s optical fibre link between the counting room and the experiments. The paper describes in detail the GBT-SERDES architecture and presents an overview of the various components that constitute the GBT chipset.

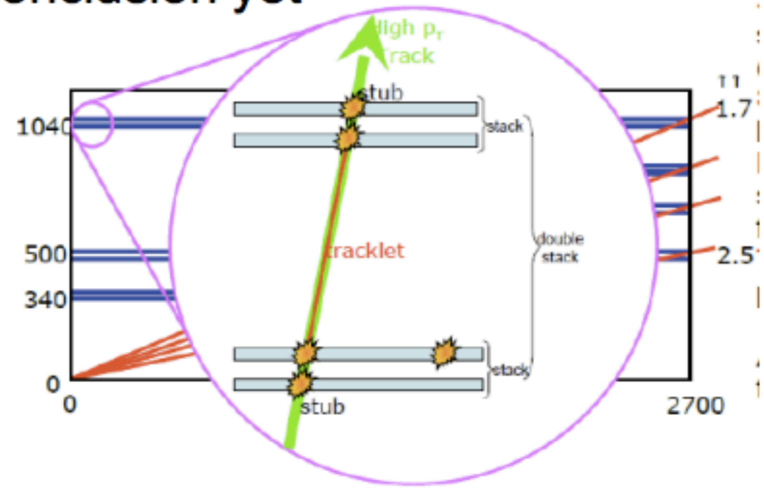
Record created 2010-01-28, last modified 2012-02-16 Similar records

The GBT project is a clear example of where common R&D can be very effective for several experiments.

Tracker layout

Several tracker layouts under study – no conclusion yet

Track finding for level 1 trigger:
+ Combine pairs of stubs from double layers (seperated order few cm) → „tracklets“
+ Processing using FPGAs

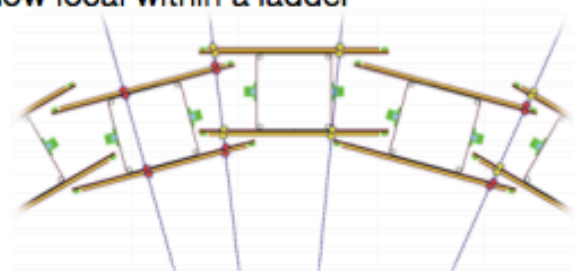


In the layout studies a compromise is sought between trigger requirements (number of trigger layers) and physics performance of the final tracker and **material budget**.

→ use of dedicated software package to study different layouts

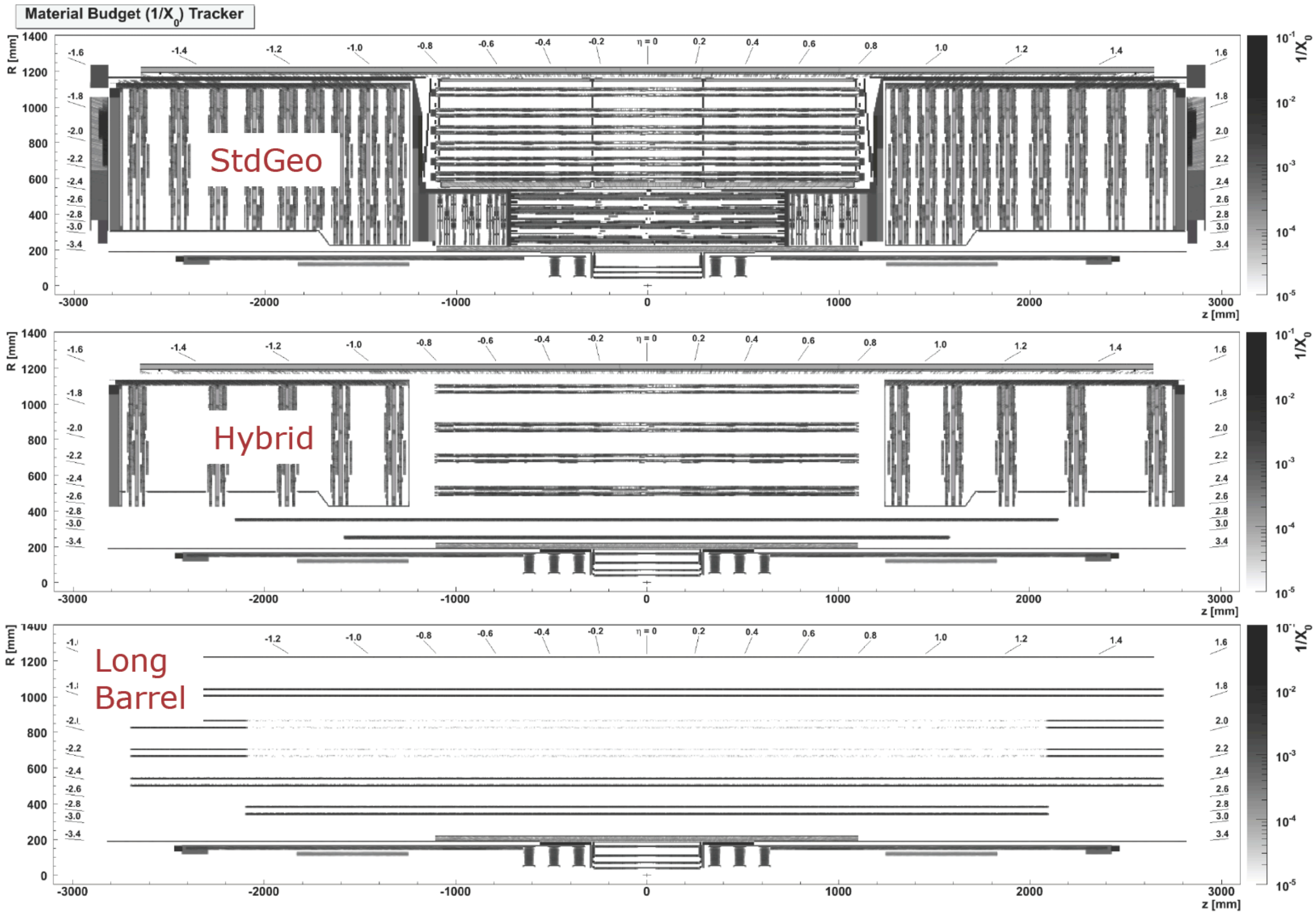
→ study feasibility of track trigger concept and implementation in CMS combined triggers

- Hermetic azimuthal coverage to keep data flow local within a ladder



Possible layouts into simulations

- Large effort in developing SLHC tracking simulations
- Started from tools hard-wired to current CMS TK geometry
- Now working with similar geometries to layout possible layouts



Final remarks

While installing the present tracker the CMS experiment was developing a plan to upgrade the silicon detector for the future.

Such plan is now split into a two phase upgrade.

We have seen today that there is a mature plan for replacing the present pixel detector in ~5 years from now (phase 1). Such a detector should guarantee adequate performance until the end of the decade.

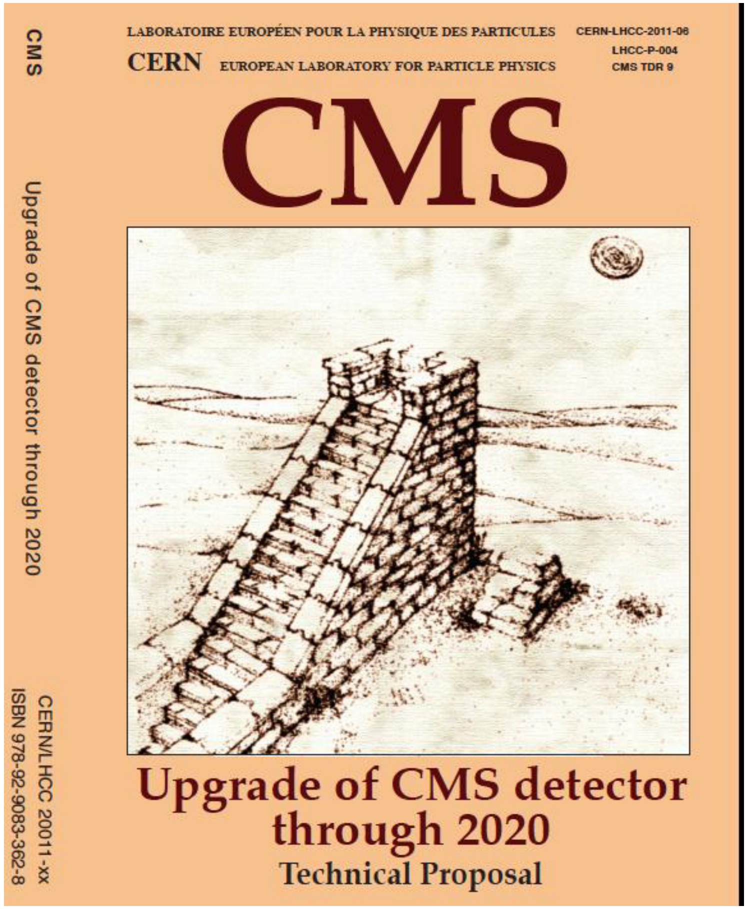
For HL-LHC the CMS tracker community is deeply committed to R&D (phase 2). Such R&D is now approaching a phase where prototypes of the various building blocks are becoming available for bench tests and testbeams.

Thank you all for your attention.

Spare slides

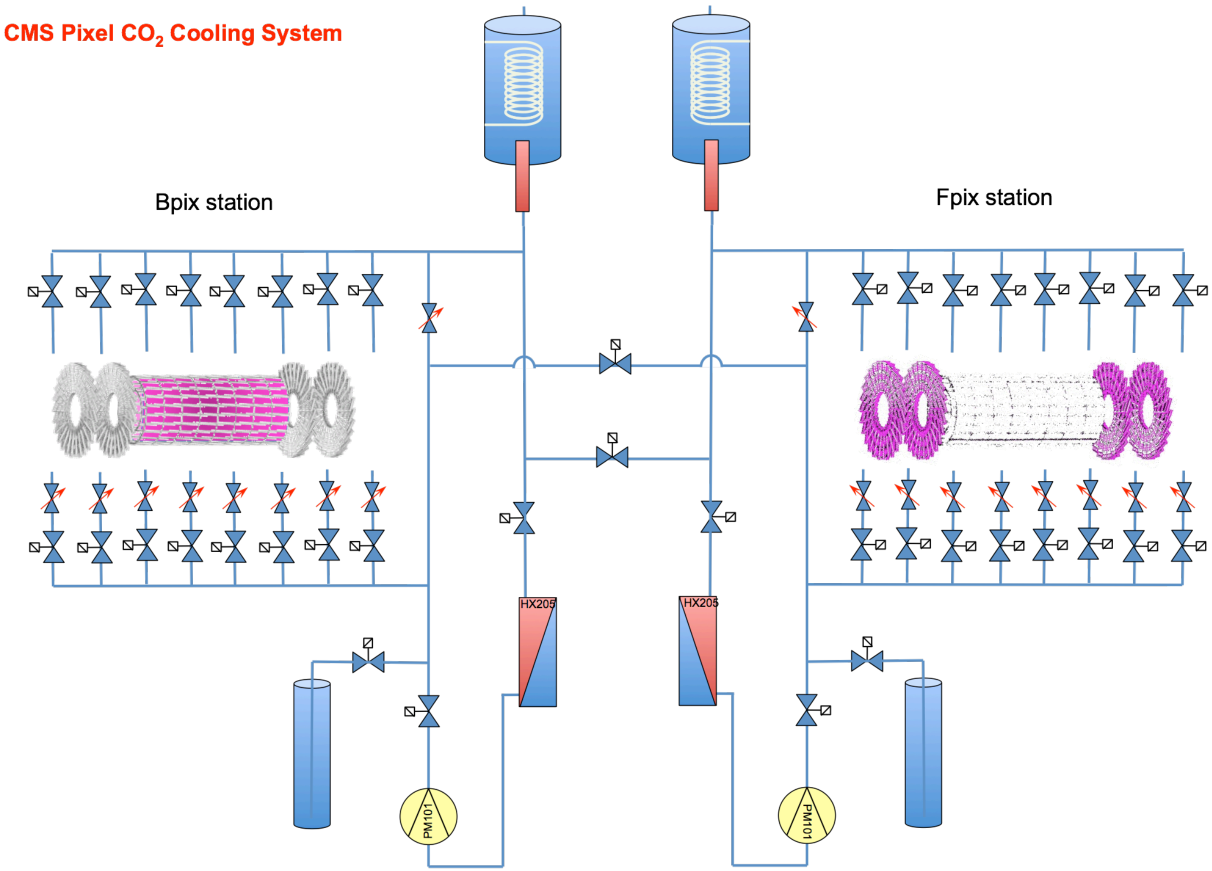
Main references

- CMS Present detector
  - 2008 *JINST* **3** S08004
  - Also www.cern.ch/icms
- Upgraded CMS detector
  - CMS Technical Proposal
    - CERN-LHCC-2011-006
- There will be a Technical Design Report (TDR) by the end of 2012 for the Pixel Phase 1 Upgrade.

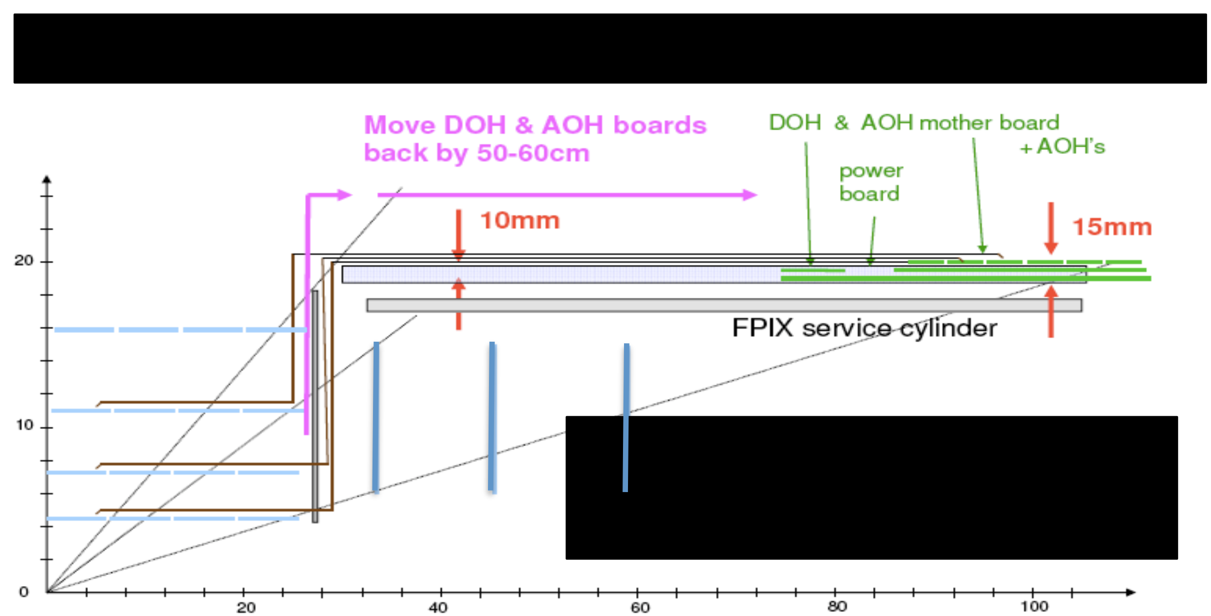


Cooling system details

- Two systems will be installed, 1 FPIX, 1 BPIX
- Different temperatures possible for FPIX and BPIX
  - **range -20C/+15C**
- Redundancy: BPIX and FPIX can both be run on either one of the two cooling plants

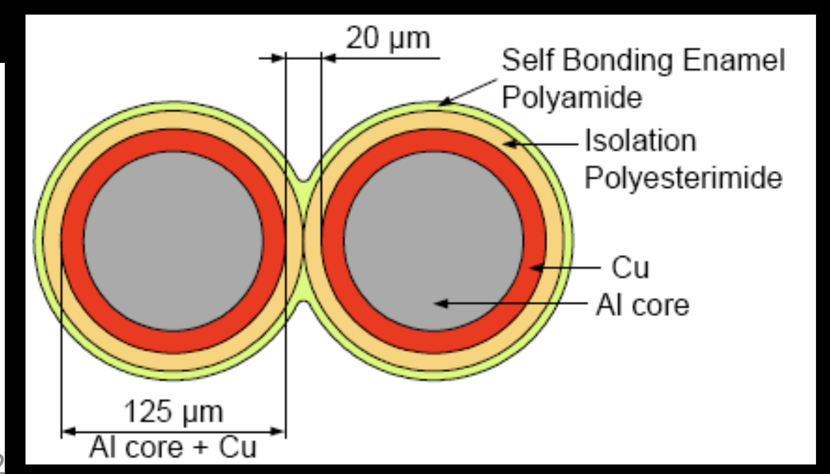


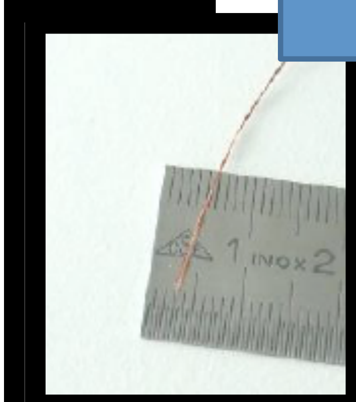
Micro-twisted-pairs



- Move BPIX optoelectronics further out

- Use micro-twisted wire cables instead of flex-cables





Cooling system details

Installing a new pixel system during a xmas break

CMS pixel has been built for fast extraction/insertion.

The initial plan (late 90s) implied a (possible) bake-out of the beam pipe during every winter shutdown.
The pixel system needs to be extracted for beam-pipe bake-out.

At present it is evident that beam-pipe bakeout is not necessary at such short intervals still CMS is compatible with extracting and reinserting the pixel system within 3 months.

We have a detailed procedure (hour by hour) of the activities needed.

Such a procedure was fully tested in 2009 when the forward pixel system was extracted for maintenance.

The time estimate associated with the removal of the present system and the installation of the phase 1 pixel detector are very solid.
Most of the work on the infrastructure for the new detector can be done while CMS is opening and most of the commissioning of the new system can be done while CMS is closing and vaccum is pumped on the beampipe.

Foreseen timeline of LS-1.5

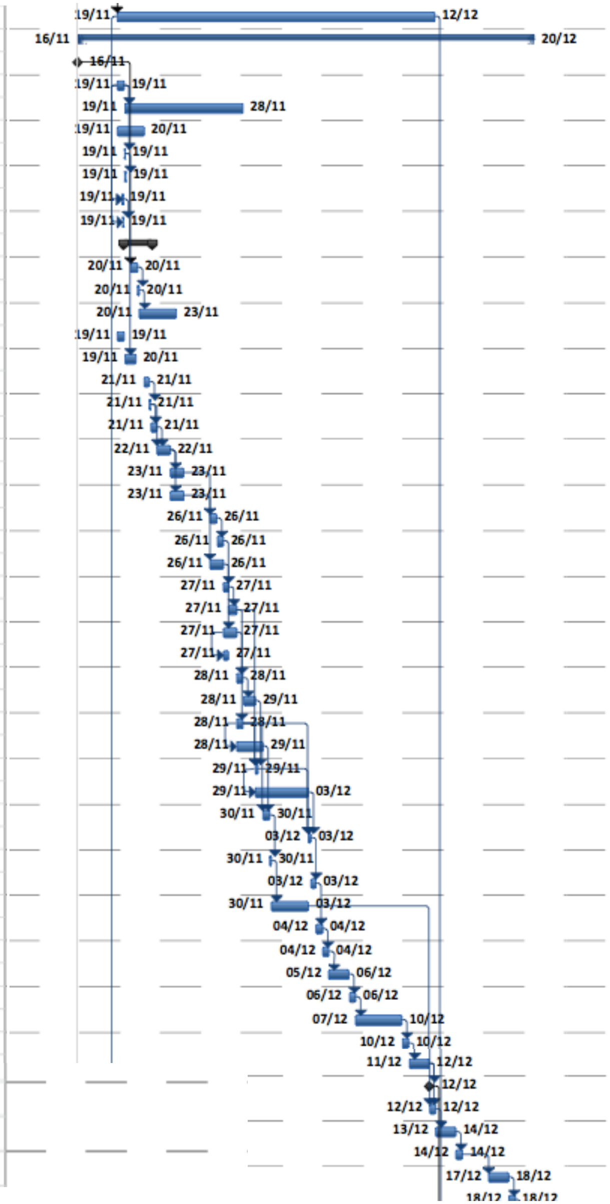
The table below shows the major activities needed during Xmas break in which we will install the Phase 1 pixel detector (xmas 2016). Units are working days.

Description	Min duration	Max duration	Int. Duration
Opening CMS	18	18	18
Installation of infrastructure (PX specific)	6	6	24
Extraction of present system	3	6	27-30
Work on cooling pipes and fibers	7	10	34-40
Insertion of BPIX and checkout of connections	4	7	38-47
Insertion of FPIX and checkout of connections	2	5	40-52
Insertion of BCM/PLT and closure of the pixel volume	3	4	43-56
Close CMS	20	20	61-76
Commission and calibrate PX	15	30	61-86 (par)

The process in total should take between 12 and 15 working week to get CMS closed.
There are 21 consecutive days to be added to “CMS Closed” for pumping down vacuum on BP.

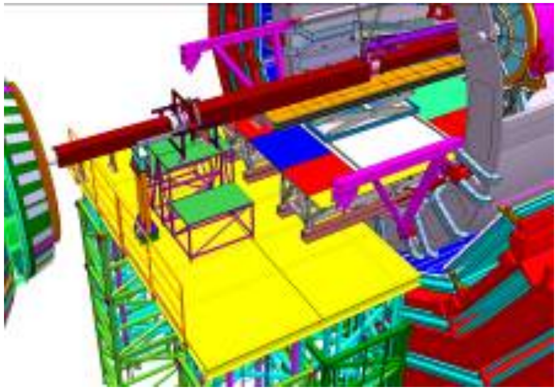
Opening of CMS.

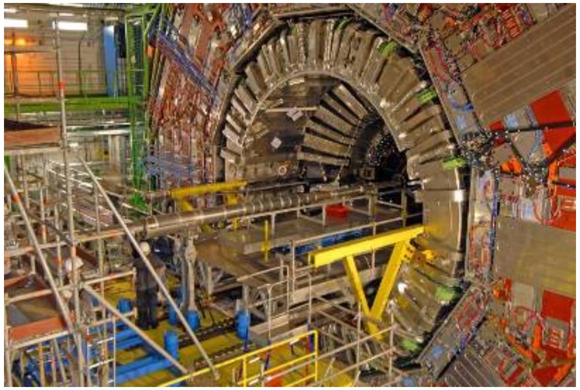
22	Bring CMS to full open config.	18 days
23	**Bring CMS to full open config.**	**24.5 days**
24	Beam Off at 18:00	0 days
25	Perform a full RP sweep	4 hrs
26	Install HFs traction system upgrade	7 days
27	Replace YE-3 hydrolics panel	2 days
28	Open PX56 Plug	1 hr
29	Switch ventilation to shutdown mode	1 hr
30	Restart crane	1 hr
31	Remove shielding around GIS	1 hr
32	**Bring CMS BP to atm pressure**	**2.38 days**
39	Open TX54	4 hrs
40	Open PM54	3 hrs
41	Remove all hand rails on balconies	20 hrs
42	Remove HF strain sensor fibres	4 hrs
43	Lower 4CPs and 2SLifts	4 hrs
44	Remove shims between collar and RSs	2 hrs
45	Open Rotating Shielding -/+Z	2 hrs
46	Open Collars	4 hrs
47	AUG tests (Cavern off limits)	1 day
48	Open HF+, T2, BSC, PLT	1 day
49	Open CASTOR	1 day
50	Remove blocking system for I beams	4 hrs
51	Prepare + Lower HF+ on 3 risers	4 hrs
52	Remove CASTOR	1 day
53	Lower HF+ on 2 risers	2 hrs
54	Install +Z extention beam + load transfer	6 hrs
55	Open HF-, T2, BSC + prepare for lowering	1 day
56	Remove PLT	1 hr
57	Lower HF- on 2 risers	4 hrs
58	Install-Z extension beam + load transfer	6 hrs
59	Extract T1+Z	4 hrs
60	Remove bellow between CT2-FWD + FWD module +Zend	2 days
61	Extract T1-Z	4 hrs
62	Remove bellow between CT2-FWD + FWD module -Zend	2 days
63	Lower HF+ to ground level	4 hrs
64	Lower HF- to ground level	4 hrs
65	Remove collars+Z	2 hrs
66	Remove collars-Z	2 hrs
67	Move HF+ in garage	4 hrs
68	Move HF- in garage	4 hrs
69	Install monorail for YE-3	0.5 days
70	Open YE-3 + VSL training	1.5 days
71	Install monorail for YE-2	0.5 days
72	Open YE-2 + VSL training	1.5 days
73	Install monorail for YE-1	0.5 days
74	Open YE-1 + VSL training	1.5 days
75	EC-Z full open configuration	0 days
76	Install monorail for YE+3	0.5 days
77	Open YE+3 + VSL training	1.5 days



Installation of pixel specific infrastructure

Lower the GASPROM platform
Installation of pixel platform and pixel scissor table.

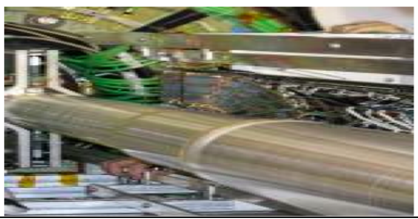




The end-goal of this process is to reach the configuration shown on the right picture and be ready to extract the present pixel system.

Extraction of present pixel system

The sequence and timing of this activity is well understood.

	Activity	End	
1	Disconnect cooling pipes and electrical/optical cables. 	Minus	½ shift
2	Setup and Extract FPIX	Minus	1 shift
3	Disconnect cooling pipes and electrical/optical connection 	Plus	½ shift
4	Setup and Extract FPIX	Plus	1 shift
5	Setup and Extract BPIX	Minus	1 shift
6	Pack and crane all removed objects to the surface for storage in the RP area 	Both	Irrelevant

The uncertainty on the time it takes (3-6 days) is associated with the capabilities of tech-coord to bring both ends open within three days from each other.

From PIX Installation to CMS close

Taken from LS1

290	Install and connect BPIX	2 days	28/03	01/04
291	Check BPIX connections	2 days	01/04	03/04
292	Install and connect FPIX	2 days	03/04	07/04
293	Check FPIX connections	2 days	07/04	09/04
294	Install BCM/PLT -Z + survey/alignment	2 days	09/04	11/04
295	Install BCM/PLT +Z + survey/alignment	2 days	11/04	15/04
296	Install Aring and connect electrics on -Z end	4 hrs	11/04	14/04
297	Install Aring and connect electrics on +Z end	4 hrs	15/04	16/04
298	Install Thermal screen -Z	1 hr	14/04	14/04
299	Install Thermal screen +Z	1 hr	16/04	16/04
300	Remove Scissor table -Z	0.5 days	14/04	14/04
301	Remove Scissor table +Z	0.5 days	16/04	16/04
302	Seal PIX volume + push test	2 days	16/04	18/04
303	Remove PIX platforms -Z	1 day	18/04	21/04
304	Remove PIX platforms +Z	1 day	21/04	22/04
305	Remove link beams to VacTank -Z	4 hrs	22/04	23/04
306	Remove link beams to VacTank +Z	4 hrs	23/04	23/04
307	Remove 20t platform -Z	1 day	23/04	24/04
308	Remove 20t platform +Z	1 day	24/04	25/04
309	Remove gasprom structure -Z	1 day	25/04	28/04
310	Remove gasprom structure +Z	1 day	28/04	29/04
311	Close CMS without T1-Z	16 days		
312	**Close CMS without T1-Z**	**8 days**		
313	Close and lock YE-1234	3 days	28/04	01/05
314	Close and lock YE+1234	3 days	01/05	06/05
315	Move HF-Z on 2 risers	1 day	06/05	07/05
316	Move HF+Z on 2 risers	1 day	07/05	08/05

14 days between starting to insert and exiting the vactank

Go to nominal temperature (COLD) and begin commissioning)

~20 days for commissioning between going COLD and CMS fully closed

Cooling system details