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# Low resources FPGA-based TDC for HET detectors of KLOE-2 experiment at DAΦNE

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Time to Digital Converters (TCDs) are very common devices in particles physics experiments. A lot of "off-the-shelf"TDCs can be employed but the necessity of a custom data acquisition system makes desirable the implementation of TDCs on the FPGAs. Most of the architectures developed so far are based on the tapped delay lines with resolutions down to 10 ps, obtained with high FPGA resources usage. Often such resolution is not needed and low resources occupancy TDC architectures are preferable. This makes possible the implementation on the same device of data processing systems and of other utilities. In order to reconstruct gamma-gamma physics events tagged in the KLOE-2 High Energy Tagger (HET), we need to measure the Time-Of-Flight (TOF) of the electrons and positrons from the KLOE-2 IP up to our tagging stations (11 m apart). A resolution better than the bunch spacing (2.7 ns) is required. We have developeded and implemented on a Xilinx Virtex-5 a 625 ps resolution TDC with embedded data acquisition systems and interface to the online FARM of KLOE-2.

## for the collaboration

KLOE-2

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