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A quadruple well CMOS MAPS prototype for the Layer0 of the SuperB SVT

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Apsel4well is a chip prototype intended for application to the Layer0 of the SuperB SVT. Physics studies set stringent requirements on the Layer0 design: radius of about 1.5 cm, high granularity (50 μm pixel pitch), fast readout techniques to comply with a high background rate, low material budget and an adequate radiation resistance. The considered approach is based on a planar 180 nm CMOS technology with an additional process step enabling the creation of a buried P-well layer. This deep-Pwell prevents the charge diffusing in the epitaxial layer from being collected by the parasitic Nwell diffusions where PMOS transistors of the readout channel are implemented. In this way, almost the whole amount of charge generated in the epitaxial layer is collected by the Nwell sensors. The ionizing radiation hardness of the device is guaranteed by the adoption of enclosed layout transistors. On the other hand, the use of a 12 μm thick high resistivity epitaxial layer is expected to increase the sensor tolerance to bulk damage. The pixel collecting electrode, consisting of four $1.5 \times 1.5 \mu\text{m}^2$ interconnected Nwell diodes, is read out by a classical channel for capacitive detectors. The Apsel4well chip consists of several test structures, including single channels, 3×3 pixel matrices and a 32×32 matrix with sparsified readout architecture and time stamping. In the final conference paper, the main design features of the chip and the results from physical device simulations will be presented.

for the collaboration

SuperB

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