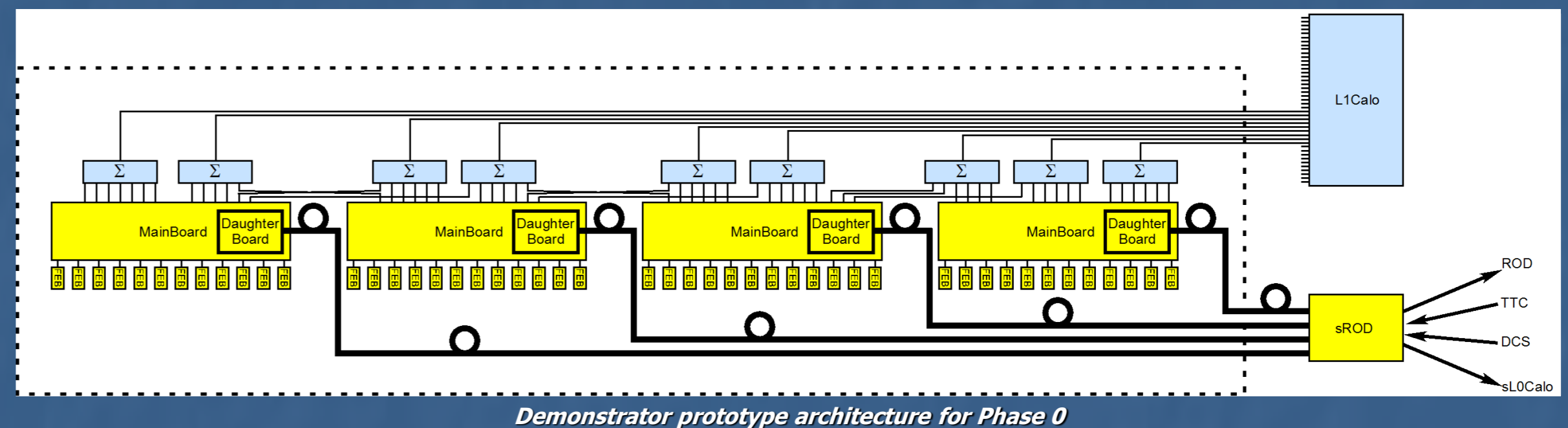
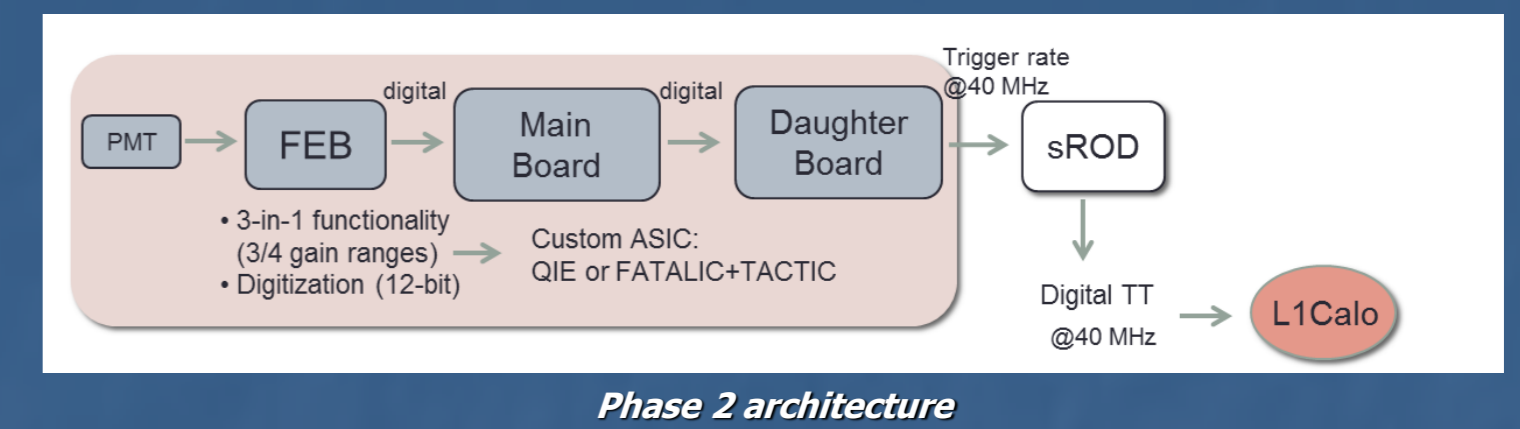
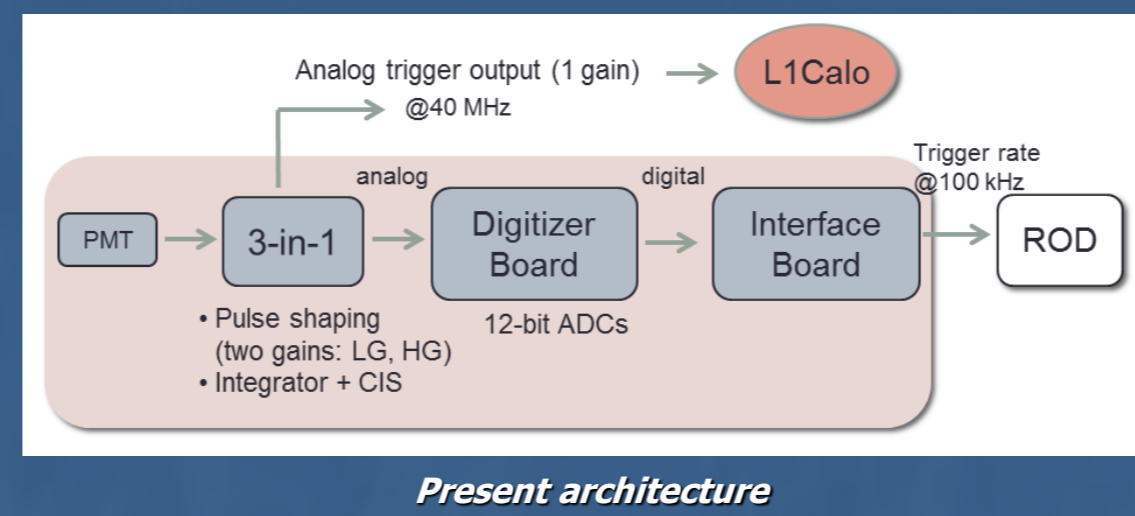


# Upgrade for the ATLAS Tile Calorimeter Readout Electronics at the High Luminosity LHC

F. Carrió<sup>1</sup> on behalf of the ATLAS Tile Calorimeter group  
<sup>1</sup>IFIC-UV

## Framework

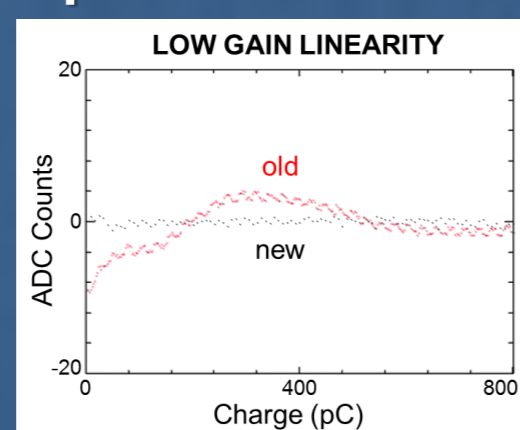
- The Tile Calorimeter is a segmented calorimeter of steel plates and plastic scintillator tiles which covers the most central region of the ATLAS experiment. It is divided in 3 sections along the beam direction, each of which is segmented azimuthally into 64 modules
- The light produced by a charged particle passing through a plastic scintillating tile is transmitted by wavelength shifting fibers to photomultiplier tubes (PMTs). These signals are read out using 10.000 electronic channels which, after digitization, which are transmitted through optical fibers to the Read Out Driver (ROD) modules
- The TileCal Phase II Upgrade is focused on replacement of most of the readout electronics by 2022. The new readout architecture will provide:
  - Full digital Level-1 trigger
  - Higher reliability and robustness
    - Redundant data links to the off-detector electronics
    - On-detector electronics will send all data to off-detector electronics every beam crossing
    - Redundant power supplies
    - Electronics design uses point of load voltage regulation
  - Higher radiation tolerance
- The Demonstrator Program for Phase 0 aims to test the new readout architecture:
  - Will be installed into detector at end of 2013 shutdown
  - Read out up to four adjacent drawers
  - Hybrid drawers compatible with the present system:
    - Complete new on-detector electronics
    - New off-detector electronics: super Read Out Driver modules (sROD)
    - Will provide both analog and digital trigger signals



## Alternatives for Front-End Boards

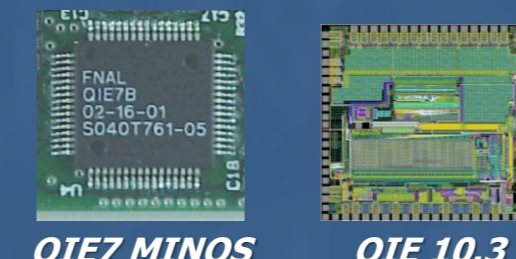
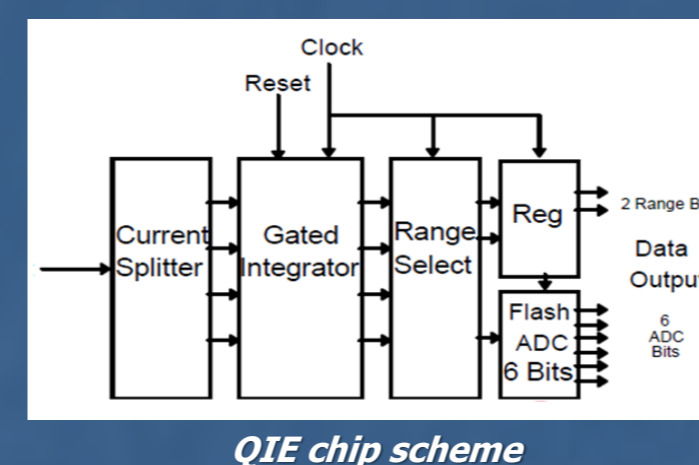
### Modified 3-in-1

- University of Chicago
- Design based on the original 3-in-1 cards
  - Compatible with the present readout system
- Main features:
  - Reception and shaping of PMT signals
    - Fast signal processing
      - 7-pole LC shape: 50ns FWHM shaping time
      - Bi-gain readout: gain ratio of 16
      - Digitization in MainBoards using 12 bit ADC
    - Slow signal processing
      - Integrator to read out Cesium calibration data
  - Charge injection calibration and controls
  - Better linearity and lower noise than previous version
- Project status:
  - Prototype tested using COTS components
  - Passed radiation tests



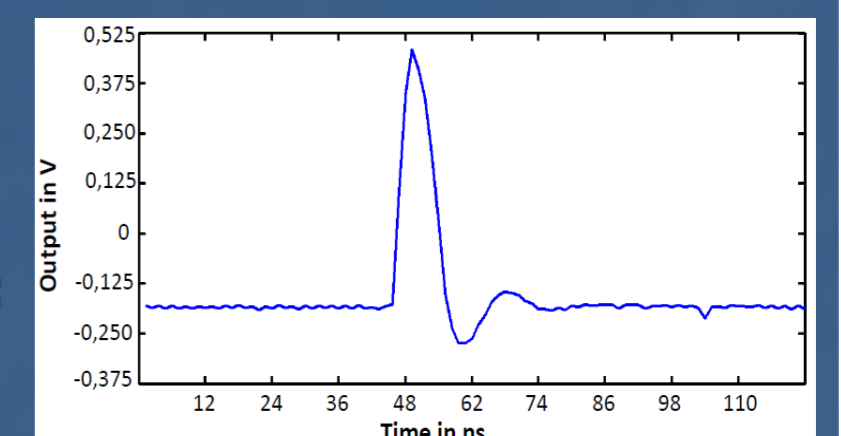
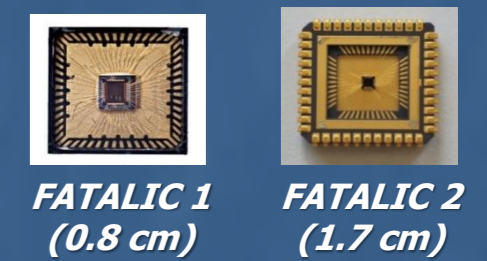
### QIE

- Argonne National Laboratory (ANL)
- Development in collaboration with FNAL and CMS HCAL
- Design based on the QIE chip (Fermilab)
- Main features:
  - Current splitter with multiple ranges and gated integrator
  - On-board flash ADC
  - 4 different gain ranges
  - 40 MHz operation
  - 16-bit dynamic range
  - Dead-timeless digitization
  - Pipelined operation
  - Charge injection for calibration
  - Integrator for calibration with source
- Project status:
  - 2 prototypes tested
  - Final version: QIE v10.4
  - Submission by November 2012



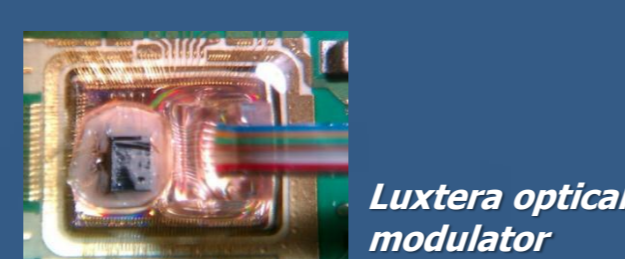
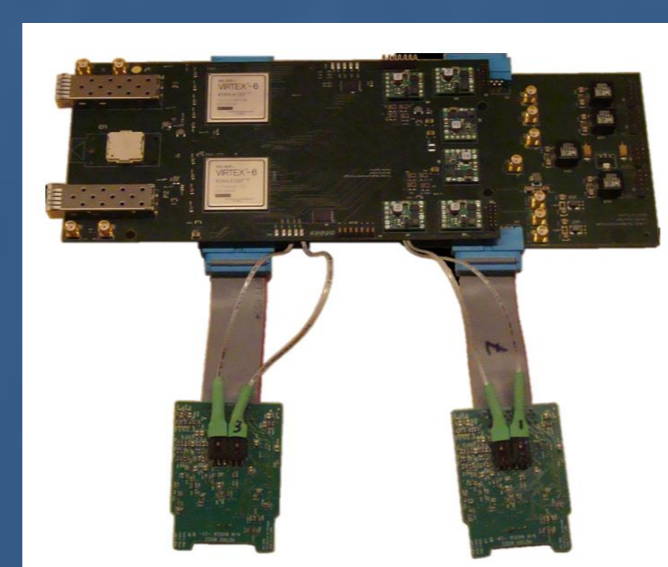
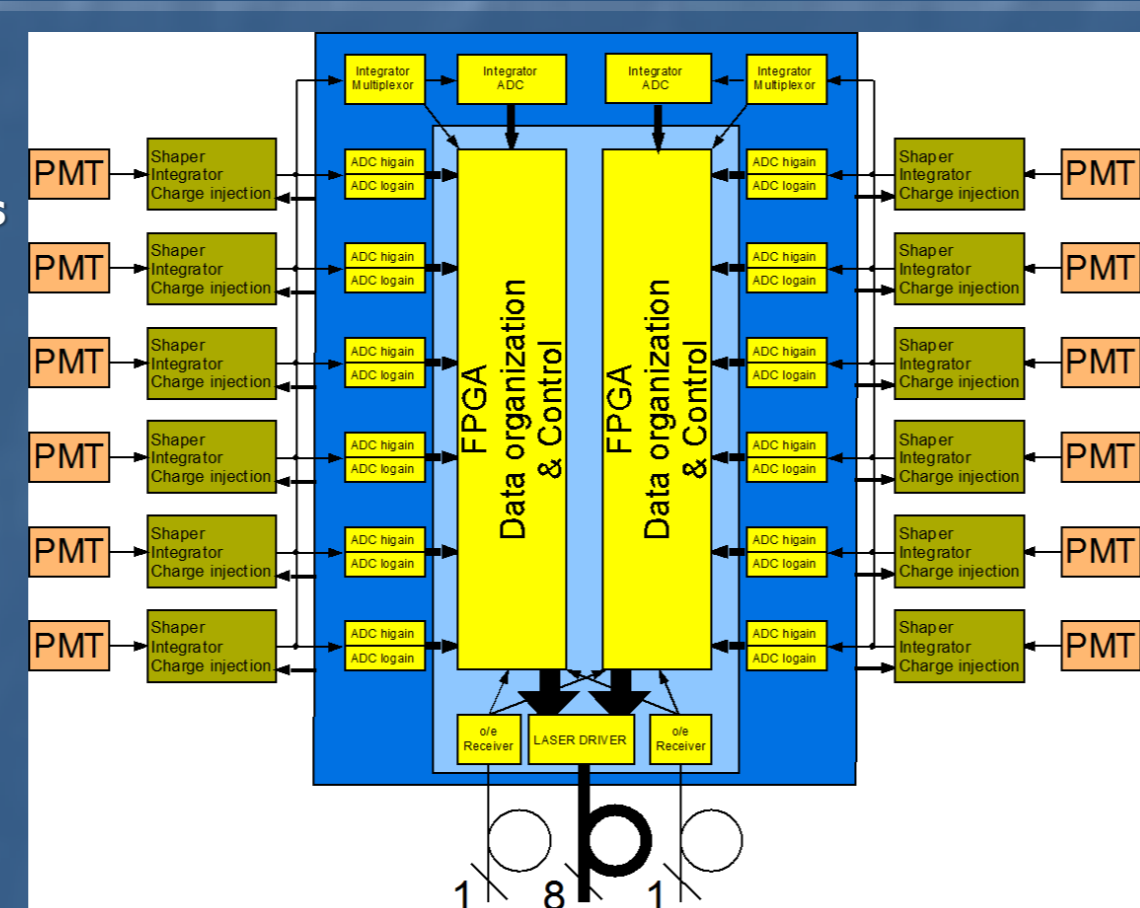
### FE-ASIC

- Clermont-Ferrand (LPC)
- Combined ASIC solution: FATALIC 3 + TACTIC
  - FATALIC 4 will include both ASICs
- IBM CMOS 130 nm technology
- FATALIC 3 main features:
  - Current conveyor
  - Shaping stage
  - 3 different gain ranges (1, 8, 64)
  - 80MHz operation
- TACTIC main features:
  - 12-bits pipeline ADC
  - 40MHz operation
- Project status:
  - First prototypes of FATALIC 1 and 2 validated
  - New version FATALIC 3 delivered March 2012:
    - Circuit corrections + integrator amplifier
    - Reduced parasitic self effects
  - TACTIC:
    - Designing the amplifier block
    - Ordered by beginning of August



## MainBoard and DaughterBoard

- University of Chicago & University of Stockholm
- MainBoard:
  - Digitizes signals coming from 4 modified 3-in-1 cards
    - Readout of 12 PMTs
    - Four 12-bit ADCs working at 40 MHz (LTC2264-12)
  - Sends digitized data to the DaughterBoard
    - 400-pin FMC connector
  - Performs AD conversion of data and digital control of the FE boards
  - Maintains compatibility with other Front-End Board alternatives
- DaughterBoard
  - Data processing unit
    - Two Xilinx Kintex-7 FPGAs
  - High speed communication between on and off-detector electronics (sROD)
    - Two SFP+ connectors for the down link
    - One SNAP12 connector for data transmission to sROD
    - 4-fold redundancy
      - All fibers are duplicated
      - 2 channels per cell
  - Clock, trigger and control obtained from GBT protocol
- Project status:
  - MainBoard and DaughterBoard prototypes tested
  - Final version design ongoing
  - Evaluating optical modulators for data transmission
    - Based on Luxtera QSFP connector (ANL)



## Super Read Out Driver (sROD)

- IFIC-Valencia, LIP & University of Stockholm
- sROD demonstrator board:
  - Data reception and processing from one new drawer
    - 4 RX Avago MiniPOD connectors – GBT protocol
    - Xilinx Virtex 7 FPGA
    - Pipeline and derandomizer memories
  - Timing, Trigger and Control (TTC) and Detector Control System (DCS) management and transmission to MainBoards
    - 1 TX Avago MiniPOD connector
  - Data reconstruction and transmission to Read Out Subsystem (ROS)
    - SFP connector – G-Link protocol
  - Data preprocessing and transmission to L1Calo
    - Xilinx Kintex 7 FPGA
    - FMC boards for expansion
      - Clock unit management
      - Communication with L1Calo
  - Double mid-size AMC board
    - Radisy's ATCA – 1200 carrier
- Project status:
  - Optical Link Card prototype tested
    - RX and TX SNAP12 connectors – GBT protocol
  - Altera Stratix II GX
  - ATCA test bench deployed and being evaluated
  - sROD demonstrator design ongoing
  - First prototypes by November 2012

