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64-Channel, 5 GSPS ADC Module with Switched Capacitor Arrays

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We present a 5 GSPS ADC/Data processing Module with up to 64 channels and 2,048 cells per channel, designed for fast-sampling, front-end applications. This is a 6U VME board, that incorporates 16 pieces DRS4 switched capacitor array chips developed at Paul Scherrer Institut, Switzerland. The 16 DRS 4 chips are grouped in four independent input blocks. A block, with a geometric size of 43 by 120 mm, has 4 pieces DRS 4 chips, 4 pieces AD9222 converters, and one Altera Stratix III FPGA. Each DRS 4 chip has 8 channels and each channel has 1024 sampling cells, which can be daisy-chained for larger sampling depth. This feature allows for a great level of flexibility in choosing the number of channels relative to capacitor array size, for a particular application. The first prototype PCB was designed for a sampling depth of 2,048 cells and 16 channels for a 42mm wide block, i.e. 64 channels for the 6U VME board. This compact form factor allows for these input blocks to be used as front-end electronics for the Cherenkov Telescope Array (CTA) cameras. In this VME board, the four blocks are fully independent and can run each in different modes without any conflict. A global FPGA, also a Stratix III device, provides control and interfacing. The module can run with a local oscillator or with input system clocks in the range of 20MHz to 550MHz. The front panel is fitted with a 2.5Gbps serial link transceiver. The full design and test results will be described.

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