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# The Front-End Chip of the SuperB SVT Detector

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The asymmetric e+e- collider SuperB is designed to deliver a high luminosity with moderate beam currents and a reduced center of mass boost with respect to earlier B-Factories. The innermost detector is the Silicon Vertex Tracker which is made of 5 layers of double sided silicon strip sensors plus a Layer0 that can be equipped with short striplets detectors in a first phase of the experiment. In order to achieve an overall track reconstruction efficiency above 98% it is crucial to optimize both analog and digital readout circuits. The readout architecture being developed for the Front-End chips will be able to cope the very high rates expected in the first layers (up to 2 MHit/s per strip in the Layer0) and can potentially accommodate higher rates with a proper tuning of the buffer depth. The readout is based on a triggered architecture where each of the 128 strip channel is provided with a dedicated digital buffer storing a 4-bit TOT in conjunction with the related time stamp. The buffers are dimensioned considering the expected trigger latency and hit rate including suitable safety margins. A dedicated circuit handles the trigger logic and conveys the parallel streams of hits to the common chip output port. This architecture has been modeled by HDL language and investigated with a Montecarlo hit generator emulating the analog front-end behavior. Simulations showed that efficiency of the digital readout remained above 99.8% even for the stressing conditions of layer 0.

## Optional extended abstract

The asymmetric e+e- collider SuperB is designed to deliver a high luminosity, greater than 10^36cm-2s-1, with moderate beam currents and a reduced center of mass boost with respect to earlier B-Factories. The innermost detector is the Silicon Vertex Tracker which is made of 5 layers of double sided silicon strip sensors plus a Layer0, that can be equipped with short striplets detectors in a first phase of the experiment. In order to achieve an overall track reconstruction efficiency above 98% it is crucial to optimize both analog and digital readout circuits. The readout architecture being developed for the Front-End chips will be able to cope the very high rates expected in the first layers (up to 2 MHit/s per strip in the Layer0) and can potentially accommodate higher rates with a proper tuning of the buffer depth. The readout is based on a triggered architecture where each of the 128 strip channel is provided with a dedicated digital buffer. Each buffer collects the digitized charge information by means of a 4-bit TOT, storing it in conjunction with the related time stamp. The buffers depth was dimensioned considering the expected trigger latency and hit rate including suitable safety margins. Every buffer is connected to a highly parallelized circuit handling the trigger logic, rejecting expired data in the buffers and channeling the parallel stream of triggered hits to the common output of the chip. The presented architecture has been modeled by HDL language and investigated with a Montecarlo hit generator emulating the analog front-end behavior. The simulations showed that even applying the highest stressing conditions of layer 0, about 256 Mhit/s, the efficiency of the digital readout remained above 99.8%.

## for the collaboration

SVT-SuperB Group

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