The front-end chip of the SuperB SVT detector

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On behalf of the SuperB SVT collaboration

Outline

• The SuperB project
• The Silicon Vertex Tracker
• The Strip / Stripllet readout chip
  – Analog front-end
  – Digital readout architecture
• Conclusions
The SuperB accelerator project

- Flavour physics promises sensitivity to New Physics ... but **large statistics is needed** (50-100 ab⁻¹)
- An upgrade to the first generation of B-Factories (PEP-II and KEKB) of ~2 orders of magnitude in \( \mathcal{L} \) is needed to get 50 ab⁻¹.
- The **SuperB** factory is an Italian e⁺ e⁻ accelerator concept that allows to reach \( \mathcal{L}=10^{36} \text{ cm}^{-2} \text{ s}^{-1} \) with **moderate beam current** (2A) using **very small beam size** (~1/100 of present B-Factories beams).
- **2007**: Conceptual Design Report published
- **2010**: Approved by the Italian Government (250 ME allocated for the Infrastructures)
- **2011**: Established site: Roma Tor Vergata
- **Management** under **Cabibbo Lab** consortium (INFN, Uni Tor Vergata, IIT).

Now closing the Technical Design Report
The SuperB Silicon Vertex Tracker

Design based on the 5-layer Babar SVT

1) Due to reduced beam energy asymmetry (7x4 GeV vs. 9x3.1 GeV) required an improved vertex resolution (~factor 2)
   - EXTRA Layer0 very close to IP (@1.5 cm) with low material budget (<1% $X_0$) and fine granularity (50 μm pitch)
   - Layer0 area 100 cm²

2) Bkg levels depend steeply on radius
   - Layer0 needs to be fast and rad hard (>20x5 MHz/cm², >3x5 M Rad/yr)

BUT

R>3 cm, Double-sided Si strip sensors.
Low-mass design. ($P_t < 2.7$ GeV)
Stand-alone tracking for slow particles.
SVT Detectors

• Baseline
  – 5 layers of silicon strip modules (ext. coverage w.r.t BaBar) for the outer layers
  – Striplets for layer0 @ R~1.5 cm.
  – Need to develop 2 new FE chips for strips: existent chips do not match all the requirements: analog info needed, high rates in inner Layers (up to 1.4 MHz/strip in L0) & short shaping time (25-100ns), very long modules and long shaping time (0.5-1 us) in Layers 4-5.

• Layer0 upgrade for full luminosity run
  – SVT Mechanics will allow a quick access/removal of Layer0
  – Upgrading to thin pixel sensors.
    • More robust against background occupancy
    • Several options investigated:
      – CMOS MAPS
      – Hybrid Pixels
      – Vertical Integration... reliable and stable?
  – R&D continue in 2012 after TDR → pixel technology decision by 2013

Ref. talk G.Rizzo on Thursday, h 12.40:
Recent developments on CMOS MAPS for the SuperB Silicon Vertex Tracker
## Strip rates on the SVT Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Side</th>
<th>Average rate on area MHz/cm²</th>
<th>Average rate kHz/strip</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>u</td>
<td>122</td>
<td>1340</td>
</tr>
<tr>
<td>0</td>
<td>v</td>
<td>181</td>
<td>1340</td>
</tr>
<tr>
<td>1</td>
<td>φ</td>
<td>15.8</td>
<td>848</td>
</tr>
<tr>
<td>1</td>
<td>z</td>
<td>13.6</td>
<td>670</td>
</tr>
<tr>
<td>2</td>
<td>φ</td>
<td>10.3</td>
<td>668</td>
</tr>
<tr>
<td>2</td>
<td>z</td>
<td>9.56</td>
<td>667</td>
</tr>
<tr>
<td>3</td>
<td>φ</td>
<td>3.03</td>
<td>580</td>
</tr>
<tr>
<td>3</td>
<td>z</td>
<td>4.19</td>
<td>397</td>
</tr>
<tr>
<td>4</td>
<td>φ</td>
<td>0.429</td>
<td>125</td>
</tr>
<tr>
<td>4</td>
<td>z</td>
<td>0.285</td>
<td>67.1</td>
</tr>
<tr>
<td>5</td>
<td>φ</td>
<td>0.216</td>
<td>81.1</td>
</tr>
<tr>
<td>5</td>
<td>z</td>
<td>0.149</td>
<td>43.9</td>
</tr>
</tbody>
</table>

Safety Factor x5 included

45°-tilted striplets

z/φ microstrip

23/05/2012

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The Strip/Striptlet front-end Chip Diagram

128 input channels

Analog Front-End:
- Pre-amplification
- Discrimination
- A/D conversion

Analog / Digital boundary

Digital Hit buffers
- Time Stamp
- ToT

Trigger Selection

Digital Readout:
- Control logic
- Trigger handling
- Hit encoding
- Formatted output

Digital output / control pads

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Analog Front End

- **Charge sensitive amplifier** with gain selection (1 bit)
- **2nd order unipolar semi-Gaussian shaper** with polarity (1 bit for p/n strip sides) and peaking time (2 bits) selection.
- **Symmetric baseline restorer** for baseline drift suppression (1 bit)
- **Threshold generator and discriminator**
- **3-4 bit A to D conversion** with TOT technique or through a flash ADC

Ref. to L. Gaioni poster: *The design of fast analog channels for the readout of strip detectors in the inner layers of the SuperB SVT*

Ref to L. Bombelli poster: *Analog Front-end Electronics for the Outer Layers of the SuperB SVT: Design and Expected Performances*
Present performance

- **Charge sensitivity**: \( \sim 5.5 \text{ mV} \) (high gain configuration)
- **Power consumption**: \( \sim 1.3 \text{ mW} \) (not including the stages following the shaper)
- **Output dynamic range**: \( \sim 15 \text{ MIP} \) (240 ke- for layer 0, 360 ke- for layers 1 to 3)
- **Response linearity**: \( \sim 3\% \)
- **S/N**: \( > 20 \) for all the layers

**Peaking times and efficiencies**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Peaking Time (ns)</th>
<th>Efficiency (r-( \phi )/z) %</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>No SF</td>
</tr>
<tr>
<td>0</td>
<td>25</td>
<td>99/99</td>
</tr>
<tr>
<td>1</td>
<td>100</td>
<td>98/98</td>
</tr>
<tr>
<td>2</td>
<td>100</td>
<td>98/98</td>
</tr>
<tr>
<td>3</td>
<td>200</td>
<td>95/95</td>
</tr>
<tr>
<td>4</td>
<td>500</td>
<td>98/98</td>
</tr>
<tr>
<td>5</td>
<td>1000</td>
<td>98/98</td>
</tr>
</tbody>
</table>

Shorter peaking time gives:
- lower inefficiency due to analog dead time
- better hit time resolution and lower occupancy
The Digital Readout Architecture

A fast digital readout architecture was developed during the R&D on pixel sensors (SLIM5 - VIPIX - SuperB collaborations)

The latest version features:
- Sparsified readout
- Temporal/Spatial hit encoding
- Data compression
- Data-push and triggered working mode
- Designed to withstand 100 MHz/cm² hit rate on a 50k channel matrix

THIS ARCHITECTURE HAS BEEN CHOSEN FOR STRIP CHIP TOO (WITH PROPER MODIFICATIONS & ADDON)
Pixel Architecture Overview

- **In-pixel** time stamping / hit-latch
- **Selective** (only where there is need to) **Column-based** hit extraction (time ordered)
- **One column** in **ONE clock cycle** (independent on the column occupancy, 256 encoded hits)
- **4 Sparsifiers**: each encode up to 64 hits into 8 words
- **4 Barrels**: memory elements with **multiple write-access ports** (up to 8) and single output
- **Time ordered** hit flow. Smart concentrator **preserve hit temporal sorting**.
Pixel Architecture Simulated Performance

**Data Push Mode**

- Efficiency vs Bunch Crossing clock

<table>
<thead>
<tr>
<th>Read Clock</th>
<th>10 ns</th>
<th>12 ns</th>
<th>15 ns</th>
<th>18 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>100.0</td>
<td>99.9</td>
<td>99.8</td>
<td>99.7</td>
</tr>
</tbody>
</table>

- 100 MHz/cm² hit rate. (tot 130 MHz)

**Triggered Mode**

- Efficiency vs trigger latency

- Expected working condition

<table>
<thead>
<tr>
<th>BC clock</th>
<th>100 ns</th>
<th>110 ns</th>
<th>120 ns</th>
<th>130 ns</th>
<th>140 ns</th>
<th>150 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>100.0</td>
<td>99.9</td>
<td>99.8</td>
<td>99.7</td>
<td>99.6</td>
<td>99.5</td>
</tr>
</tbody>
</table>

- 100 MHz/cm² hit rate. (tot 130 MHz)
- 192x256 matrix
- 50 MHz read clock
- 2.5 MHz trigger rate (stressed condition)
- 200k events per point

Efficiency slightly decreases (linear) as the trigger latency increase:

**NO pre-trigger front buffer** was foreseen in this pixel readout solution.

**Pixels latch as memory bit.**

- Higher granularity → lower occupancy
- Smoother efficiency drop w.r.t. strips

Simulations DO NOT take into account:
- Sensor Efficiency.
- Analog FE.
Strip Front-End Architecture Overview

- All hits of a triggered time-stamp processed at a time
- 4 Sparsifiers: each encode up to 8 channels into 8 words: (TS, Address, ToT ...)
- 4 Barrels: memory elements with multiple write-access ports (up to 8) and single output
- Time ordered hit flow. Smart concentrator preserve hit temporal sorting.

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Strip Front-End Architecture Overview

• Readout logic is replicated 4 Times
• Common final output stage

Round Robin

Common output stage

Data Serialized on 1 up to 6 lines per chip.

4 parallel Readout: 128 Channels

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## F.E. Chip Data Rates & Serial Links

<table>
<thead>
<tr>
<th>Layer</th>
<th>Side</th>
<th>Required Bandwidth Mbit/s</th>
<th>Lines at 60 MHz</th>
<th>Lines at 120 MHz</th>
<th>Lines at 180 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>u</td>
<td>250</td>
<td>6</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>0</td>
<td>v</td>
<td>250</td>
<td>6</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>φ</td>
<td>230</td>
<td>5</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>z</td>
<td>123</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>φ</td>
<td>170</td>
<td>4</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>z</td>
<td>130</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>φ</td>
<td>143</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>z</td>
<td>119</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>φ</td>
<td>120</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>z</td>
<td>118</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>φ</td>
<td>87.6</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>z</td>
<td>76.1</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

*Trigger 150 kHZ*

*15 % protocol overhead (on Layer0)*
Trigger handling

- External electronic boards process primary trigger signals.
- Pre-processed triggers are sent to front-end electronics.
  - Fixed trig. latency on chip → configured at start-up
  → Simpler on-chip trigger logic
  - Rely on re-configurable logic on external boards for more complicate algorithms.

- **One-wire trigger** to FE chips.

![Diagram showing trigger handling process](image_url)
Strip Chip Architecture Simulations

• GOALs:
  – Choose optimal front buffer dimensions (trade-off efficiency vs cells saving)
  – Measure ~ 100 % efficiency after pre-trigger buffer insertion
  – Verify functionality of the well-known digital core in the new environment.

• Efficiency evaluation: \( 1 - \frac{H_t - H_O}{H_t} \)
  
  \( H_t = \) Hits triggered in digital buffer
  \( H_O = \) Hits on output

• VHDL test bench and Monte Carlo generator

NB: Only digital readout efficiency taken into account
Results:
- ~**100 % efficiency** observed (digital only)
- Front buffers optimal depth: **32 hits**
  - Deeper front buffers → higher rates/trig. latency handled
- Logical verification of the architecture **OK**
Conclusions

SuperB strip FE chip development:
• **2 front-end chips** under development with different analog characteristics, same digital architecture
• **Analog channel simulated**: shaping time reduction for some layers under evaluation to mitigate background impact
• **Digital readout architecture** mostly inherited from pixel R&D
• Addition of **dedicated FIFOs** as hit buffers during trigger latency
• Whole digital readout architecture simulated (VHDL) with Monte Carlo hit generator: **100% digital efficiency** achievable even for high Layer0 rates: ~1.5 MHz/strip including SF x5.
• **Higher rates can be handled** increasing the **front buffer size**. (⇒ Higher throughput ⇒ higher number of lines and/or higher line-rate)
• FE chip **work completed for TDR**

Next steps
• First FE chip submission with IBM 130 nm - Nov. 2012
Thanks for your attention
Back Up Slides
The SuperB SVT Collaboration

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Silicon Vertex Tracker

- **B → π π decay mode**, βγ = 0.28, beam pipe X/X0 = 0.42%, hit resolution = 10 μm

### BaBar SVT
- 5 Layers of double-sided Si strip sensor
- Low-mass design. (Pt < 2.7 GeV)
- Stand-alone tracking for slow particles.
- 97% reconstruction efficiency
- Resolution ~15 μm at normal incidence

### Design based on the 5-layer Babar SVT (R>3cm)

**BUT:**
- Due to reduced beam energy asymmetry (7x4 GeV vs. 9x3.1 GeV) required an improved vertex resolution (~factor 2)
  - EXTRA Layer0 very close to IP (@1.5 cm) with low material budget (<1% X0) and fine granularity (50 μm pitch)
  - Layer0 area 100 cm²

- Bkg levels depend steeply on radius
  - Layer0 needs to be fast and rad hard (>20x5 MHz/cm², >3x5 MRad/yr)
Pixel digital architecture (PI)

Analog front-end

- Threshold comparator

Hit latch

TS latch

Comparator

Time counter

Reading Time Stamp

FAST-OR logic
Pixel digital architecture (PI)

Analog front-end

Threshold comparator

Hit latch

TS latch

Comparator

COL_ENABLE

PXL_DATA_BUS

Reading Time Stamp

Hit extraction logic

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Monte Carlo tuned to obtain 100 MHz/cm² hit rate on area

C++ Reports, efficiency check, analysis tools ...

MC hit extraction and application on the matrix model

Simulating hit extraction, encoding and sequencing

Generation of report files
Cluster SVTHit Z/Phi Multiplicity2 on Svt Layer 0

From Physical background simulations

Simulated architecture:
few clustered events read out
Simulation results

2 MHz/strip : Layer 0

<table>
<thead>
<tr>
<th>buffer size</th>
<th>16</th>
<th>32</th>
<th>64</th>
</tr>
</thead>
<tbody>
<tr>
<td>buffered hits</td>
<td>3.8 M</td>
<td>12.9 M</td>
<td>12.9 M</td>
</tr>
<tr>
<td>of which triggered</td>
<td>23363</td>
<td>76850</td>
<td>23363</td>
</tr>
<tr>
<td>output triggered hits</td>
<td>14679</td>
<td>76849</td>
<td>23363</td>
</tr>
<tr>
<td>triggered hit lost</td>
<td>8684</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Efficiency (%)</td>
<td>62.8</td>
<td>99.9987</td>
<td>100</td>
</tr>
</tbody>
</table>

760 kHz/strip : Layer 1

<table>
<thead>
<tr>
<th>buffer size</th>
<th>8</th>
<th>16</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>buffered hits</td>
<td>1.4 M</td>
<td>7 M</td>
<td>7 M</td>
</tr>
<tr>
<td>of which triggered</td>
<td>8748</td>
<td>28829</td>
<td>28829</td>
</tr>
<tr>
<td>output triggered hits</td>
<td>6788</td>
<td>28825</td>
<td>28829</td>
</tr>
<tr>
<td>triggered hit lost</td>
<td>1960</td>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>Efficiency (%)</td>
<td>77.6</td>
<td>99.986</td>
<td>100</td>
</tr>
</tbody>
</table>
TOT counter bit number

Shaper linearity over the full signal dynamic range (15 MIPs) is assumed.
Uncertainty in the estimation of $t_0$

$$t_0 = t_{th} - t_{walk}$$

<table>
<thead>
<tr>
<th>Layer</th>
<th>$t_p$ [ns]</th>
<th>$t_p/T_{CK,TOT}$</th>
<th>$f_{CK,TS}$ [MHz]</th>
<th>$\sigma_{walk}$ [ns]</th>
<th>$\sigma_{t0}$ [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>25</td>
<td>4</td>
<td>30</td>
<td>1.6</td>
<td>9.8</td>
</tr>
<tr>
<td>1</td>
<td>100</td>
<td>4</td>
<td>30</td>
<td>6.2</td>
<td>11.4</td>
</tr>
<tr>
<td>2</td>
<td>100</td>
<td>4</td>
<td>30</td>
<td>6.2</td>
<td>11.4</td>
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<td>3</td>
<td>200</td>
<td>4</td>
<td>30</td>
<td>12.5</td>
<td>15.8</td>
</tr>
<tr>
<td>4</td>
<td>500</td>
<td>4</td>
<td>30</td>
<td>31.2</td>
<td>32.6</td>
</tr>
<tr>
<td>5</td>
<td>1000</td>
<td>4</td>
<td>30</td>
<td>62.5</td>
<td>63.2</td>
</tr>
</tbody>
</table>

Actually $\sigma_{walk}$ gets smaller for larger values of TOT, so better estimation of $t_0$ could be obtained
<table>
<thead>
<tr>
<th>Layer</th>
<th>Hit rate/strip [kHz]</th>
<th>Peaking time [ns]</th>
<th>Efficiency - random waveform generation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>safety factor 5 included</td>
</tr>
<tr>
<td>0 - side 1</td>
<td>933</td>
<td>25</td>
<td>0.955</td>
</tr>
<tr>
<td>0 - side 2</td>
<td>937</td>
<td>25</td>
<td>0.967</td>
</tr>
<tr>
<td>1 - phi</td>
<td>853</td>
<td>50</td>
<td>0.943</td>
</tr>
<tr>
<td></td>
<td></td>
<td>75</td>
<td>0.917</td>
</tr>
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<td></td>
<td></td>
<td>100</td>
<td>0.889</td>
</tr>
<tr>
<td>1 - z</td>
<td>671</td>
<td>50</td>
<td>0.938</td>
</tr>
<tr>
<td></td>
<td></td>
<td>75</td>
<td>0.908</td>
</tr>
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