Frontier Detectors for Frontier Physics

12th Pisa meeting on advanced detectors

The front-end chip of the SuperB SVT detector

F. Giorgi INFN and University of Bologna, Italy

On behalf of the SuperB SVT collaboration

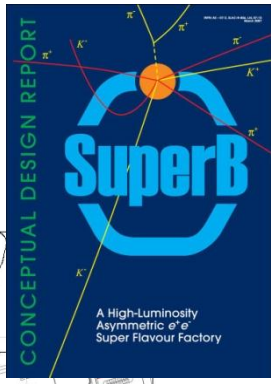
C. Avanzini, G. Batignani, S. Bettarini, F. Bosi, G. Calderini, G. Casarosa, M. Ceccanti, R. Cenci, A. Cervelli, F. Crescioli, M. Dell'Orso, F. Forti, P. Giannetti, M.A. Giorgi, A.Lusiani, S. Gregucci, P. Mammini, G. Marchiori, M. Massa, F. Morsani, N. Neri, E. Paoloni, M. Piendibene, A. Profeti, G. Rizzo, L. Sartori, J. Walsh, E. Yurtsev, M. Manghisoni, V. Re, G. Traversi, M. Bruschi, R. Di Sipio, B. Giacobbe, A. Gabrielli, F. Giorgi, G. Pellegrini, C. Sbarra, N. Semprini, R. Spighi, S. Valentinetti, M. Villa, A. Zoccoli, M. Citterio, V. Liberali, A. Stabile, F. Palombo, L. Gaioni, A. Manazza, L. Ratti, V. Speziali, S. Zucca, D. Gamba , G. Giraudo , P. Mereu , G.F. Dalla Betta, G. Soncini, G. Fontana, M. Bomben, L. Bosisio, P. Cristaudo, D. Jugovaz, L. Lanceri, I. Rashevskaya, L. Vitale, G. Venier

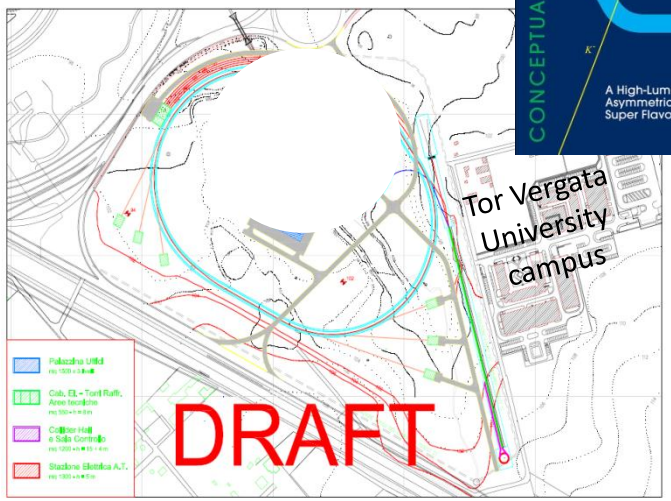
Outline

- The SuperB project
- The Silicon Vertex Tracker
- The Strip / Striplet readout chip
  - Analog front-end
  - Digital readout architecture
- Conclusions

The SuperB accelerator project

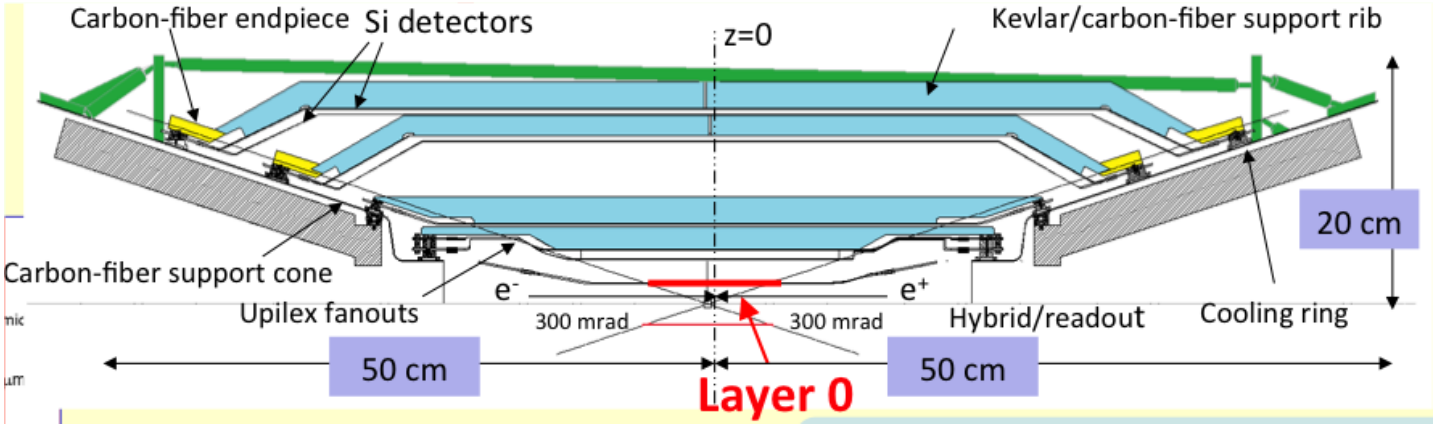
- Flavour physics promises sensitivity to New Physics ... but **large statistics is needed** (50-100 ab^{-1})
- An upgrade to the first generation of B-Factories (PEP-II and KEKB) of **~2 orders of magnitude** in $\mathscr{L}$ is needed to get **50 ab^{-1}**.
- The **SuperB** factory is an Italian e^+ e^- accelerator concept that allows to reach $\mathscr{L}$**=10^{36} cm^{-2} s^{-1}** with moderate beam current (2A) using very small beam size (~1/100 of present B-Factories beams).
- **2007** : **Conceptual Design Report published**
- **2010 : Approved** by the Italian Government (250 ME allocated for the Infrastructures)
- **2011** : **Established site: Roma Tor Vergata**
- **Management** under **Cabibbo Lab** consortium (INFN, Uni Tor Vergata, IIT).





Now closing the Technical Design Report

The SuperB Silicon Vertex Tracker



Design based on the 5-layer Babar SVT

R>3 cm, Double-sided Si strip sensors.
Low-mass design. (P_t < 2.7 GeV)
Stand-alone tracking for slow particles.

BUT

1) Due to reduced beam **energy asymmetry** (7x4 GeV vs. 9x3.1 GeV) required an **improved vertex resolution** (~factor 2)

- **EXTRA Layer0 very close to IP** (@**1.5 cm**)

with **low material budget** (<1% X_0) and **fine granularity** (50 μm pitch)

- Layer0 **area 100 cm²**

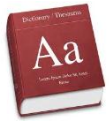
2) Bkg levels depend steeply on radius

- Layer0 needs to be **fast** and **rad hard**

(>20x5 MHz/cm², >3x5 MRad/yr)

SVT Detectors

- **Baseline**
  - 5 layers of **silicon strip** modules (ext. coverage w.r.t BaBar) for the outer layers
  - **Striplets** for layer0 @ R~1.5 cm.
  - Need to develop **2 new FE chips** for strips: existent chips do not match all the requirements: **analog info** needed, **high rates** in inner Layers (up to 1.4 MHz/strip in L0) & **short shaping time** (25-100ns), very long modules **and long shaping time** (0.5-1 us) in Layers 4-5.
- **Layer0 upgrade** for full luminosity run
  - SVT Mechanics will allow a **quick access/removal** of Layer0
  - Upgrading to thin **pixel sensors.**
    - **More robust** against background **occupancy**
    - Several options investigated:
      - **CMOS MAPS**
      - **Hybrid Pixels**
      - **Vertical Integration…** reliable and stable ?
  - R&D continue in 2012 after TDR → pixel technology decision by 2013



Ref. talk G.Rizzo on Thursday, h 12.40 :
Recent developments on CMOS MAPS for the SuperB Silicon Vertex Tracker

Strip rates on the SVT Layers

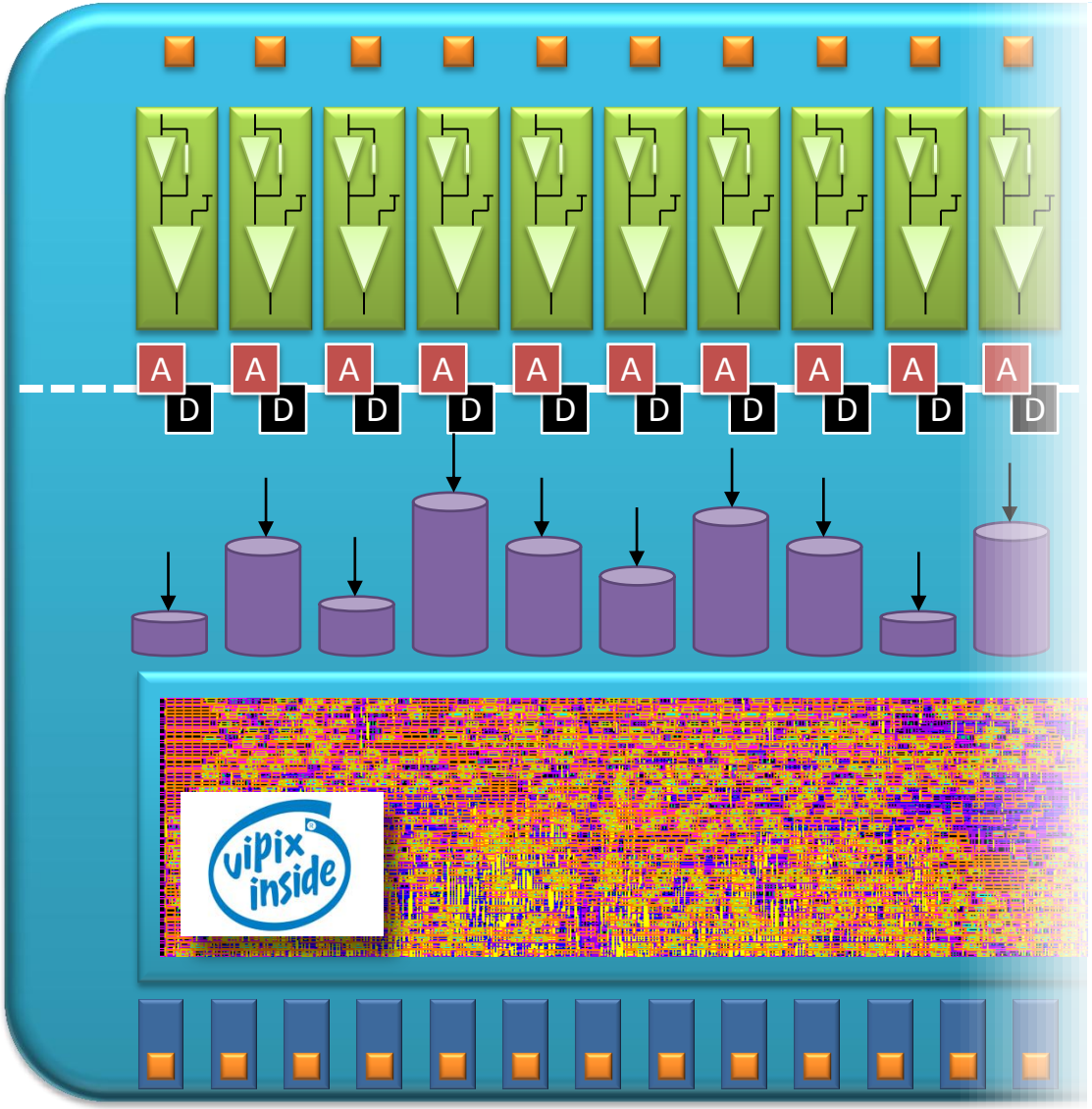
Safety Factor x5 included

45°-tilted striplets

z/ϕ microstrip

Layer	Side	Average rate on area MHz/cm^2	Average rate kHz/strip
0	u	122	1340
0	v	181	1340
1	ϕ	15.8	848
1	z	13.6	670
2	ϕ	10.3	668
2	z	9.56	667
3	ϕ	3.03	580
3	z	4.19	397
4	ϕ	0.429	125
4	z	0.285	67.1
5	ϕ	0.216	81.1
5	z	0.149	43.9

The Strip/Striplet front-end Chip Diagram



128 input channels

Analog Front-End:
- Pre-amplification
- Discrimination
- A/D conversion

Analog / Digital boundary

Digital Hit buffers
- Time Stamp
- ToT

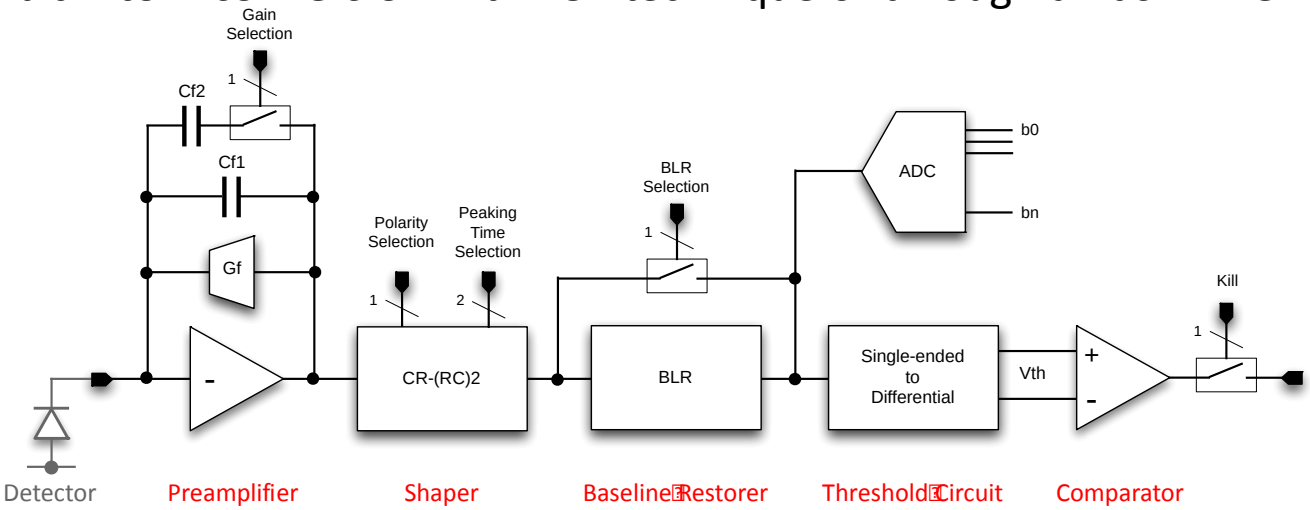
Trigger0 Selection

Digital Readout:
- Control logic
- Trigger handling
- Hit encoding
- Formatted output

Digital output / control pads

Analog Front End

- **Charge sensitive amplifier** with gain selection (1 bit)
- **2nd order unipolar semi-Gaussian shaper** with polarity (1 bit for p/n strip sides) and peaking time (2 bits) selection.
- **Symmetric baseline restorer** for baseline drift suppression (1 bit)
- **Threshold generator and discriminator**
- **3-4 bit A to D conversion** with TOT technique or through **a flash ADC**

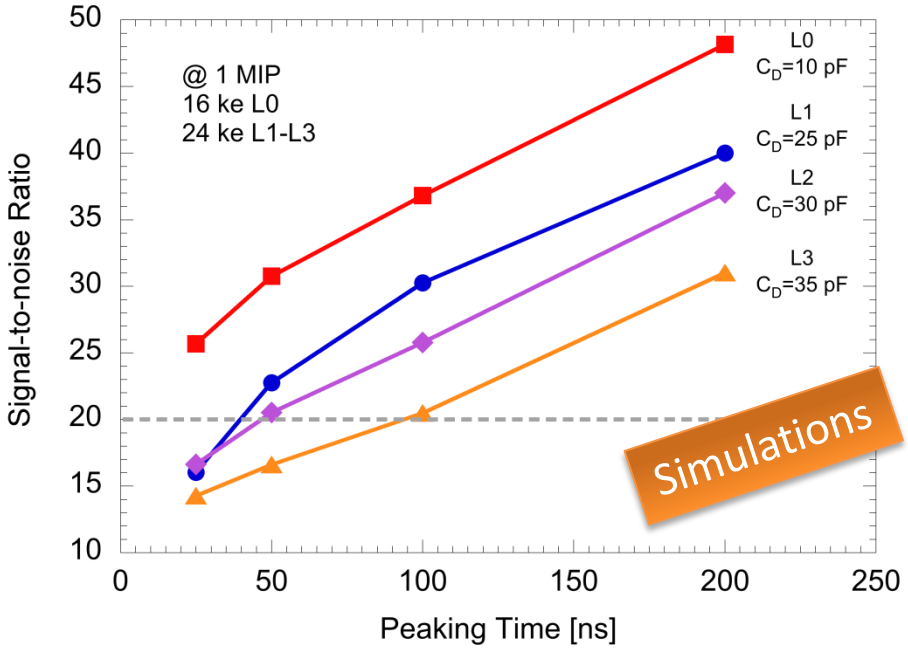


Ref. to L. Gaioni poster : The design of fast analog channels for the readout of strip detectors in the inner layers of the SuperB SVT

Ref to L. Bombelli poster : Analog Front-end Electronics for the Outer Layers of the SuperB SVT: Design and Expected Performances

Present performance

- **Charge sensitivity**: ~5.5 mV (high gain configuration)
- **Power consumption**: ~1.3 mW (not including the stages following the shaper)
- **Output dynamic range**: ~15 MIP (240 ke- for layer0, 360 ke- for layers 1 to 3)
- **Response linearity**: ~3%
- **S/N:** > 20 for all the layers



Peaking times and efficiencies

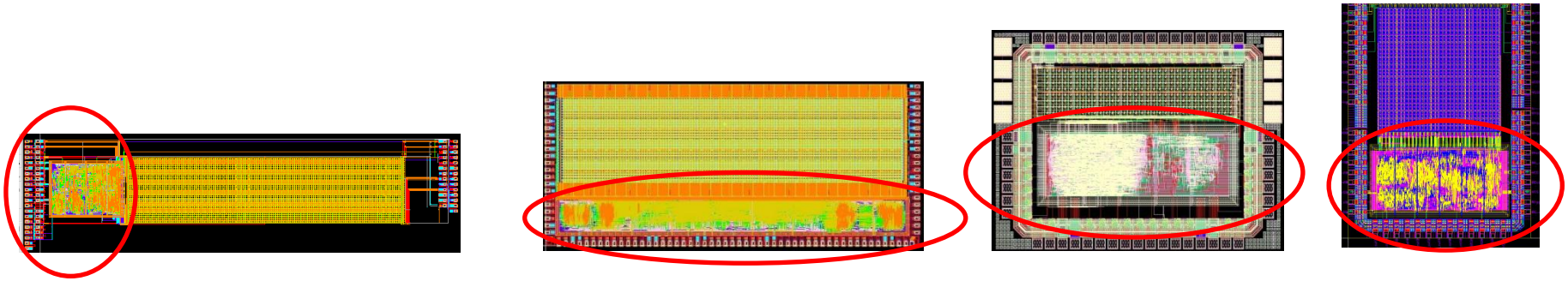
Layer	Peaking Time (ns)	Efficiency (r-ϕ/z) %	
		No SF	SF x5
0	25	99/99	96/96
1	100	98/98	88/89
2	100	98/98	89/89
3	200	95/95	77/86
4	500	98/98	89/93
5	1000	98/98	86/91

Shorter peaking time gives:

- *lower inefficiency due to analog dead time*
- *better hit time resolution and lower occupancy*

The Digital Readout Architecture

A **fast digital readout** architecture was developed during the R&D on **pixel** sensors (***SLIM5 - VIPIX - SuperB*** collaborations)

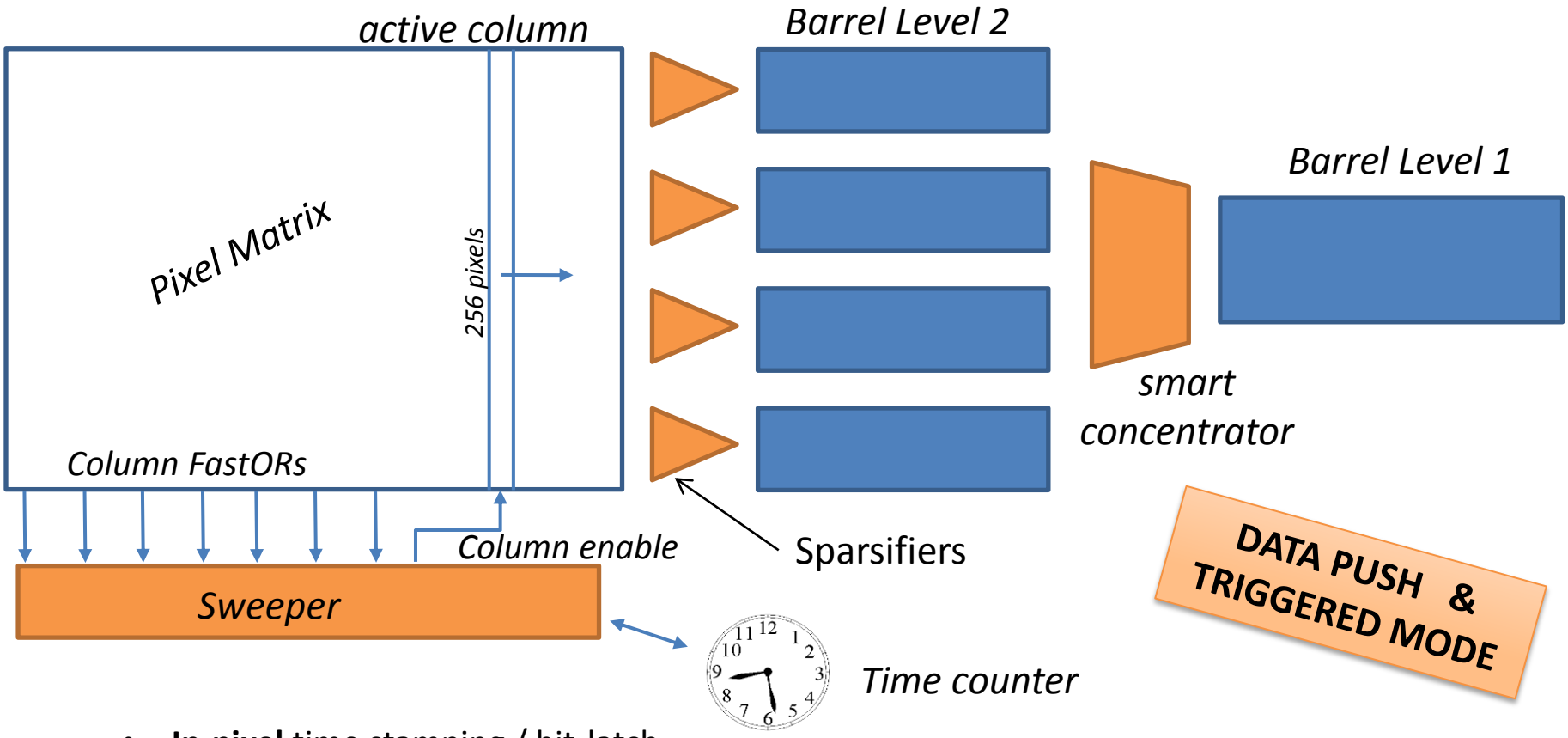


The latest version features:

- Sparsified readout
- Temporal/Spatial hit encoding
- Data compression
- Data-push and triggered working mode
- Designed to withstand **100 MHz/cm^2** hit rate on a 50k channel matrix

THIS ARCHITECTURE HAS BEEN CHOSEN **FOR STRIP CHIP** TOO
(WITH PROPER MODIFICATIONS & ADDON)

Pixel Architecture Overview

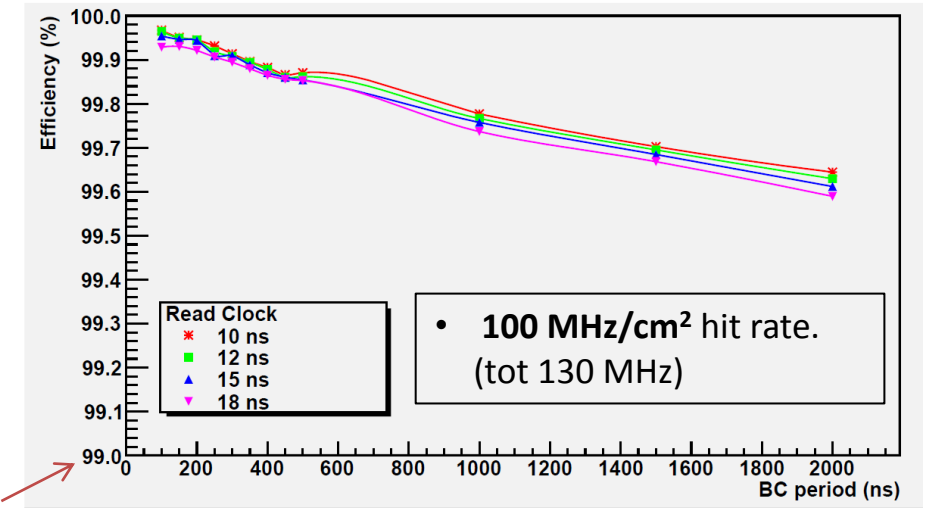


- **In-pixel** time stamping / hit-latch
- **Selective** (only where there is need to) **Column-based** hit extraction (time ordered)
- **One column** in **ONE clock cycle** (independent on the column occupancy, 256 encoded hits)
- **4 Sparsifiers**: each encode up to 64 hits into 8 words
- **4 Barrels**: memory elements with **multiple write-access ports** (up to 8) and single output
- **Time ordered** hit flow. Smart concentrator **preserve hit temporal sorting**.

Pixel Architecture Simulated Performance

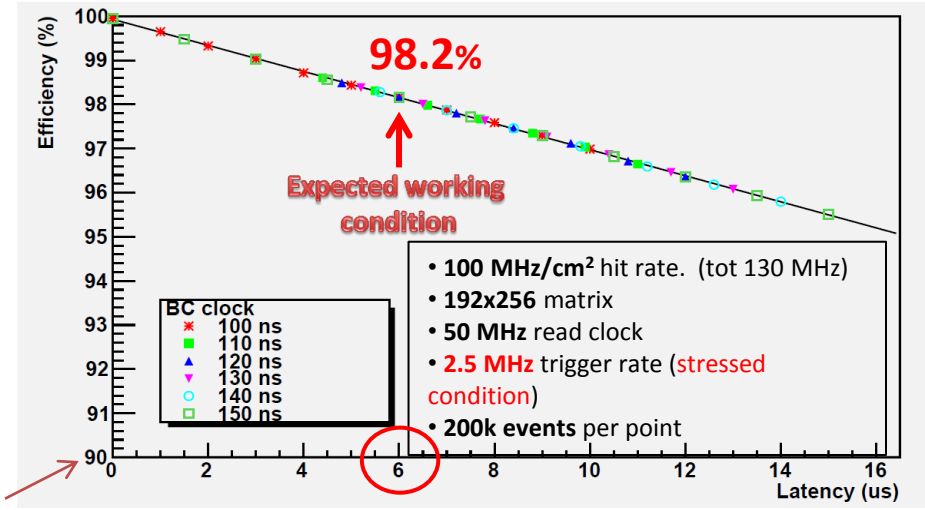
DATA PUSH MODE

Efficiency VS Bunch Crossing clock



TRIGGERED MODE

Efficiency VS trigger latency



Simulations DO NOT take into account:
- **Sensor Efficiency.**
- **Analog FE.**

Efficiency slightly decreases (**linear**) as the trigger latency increase:

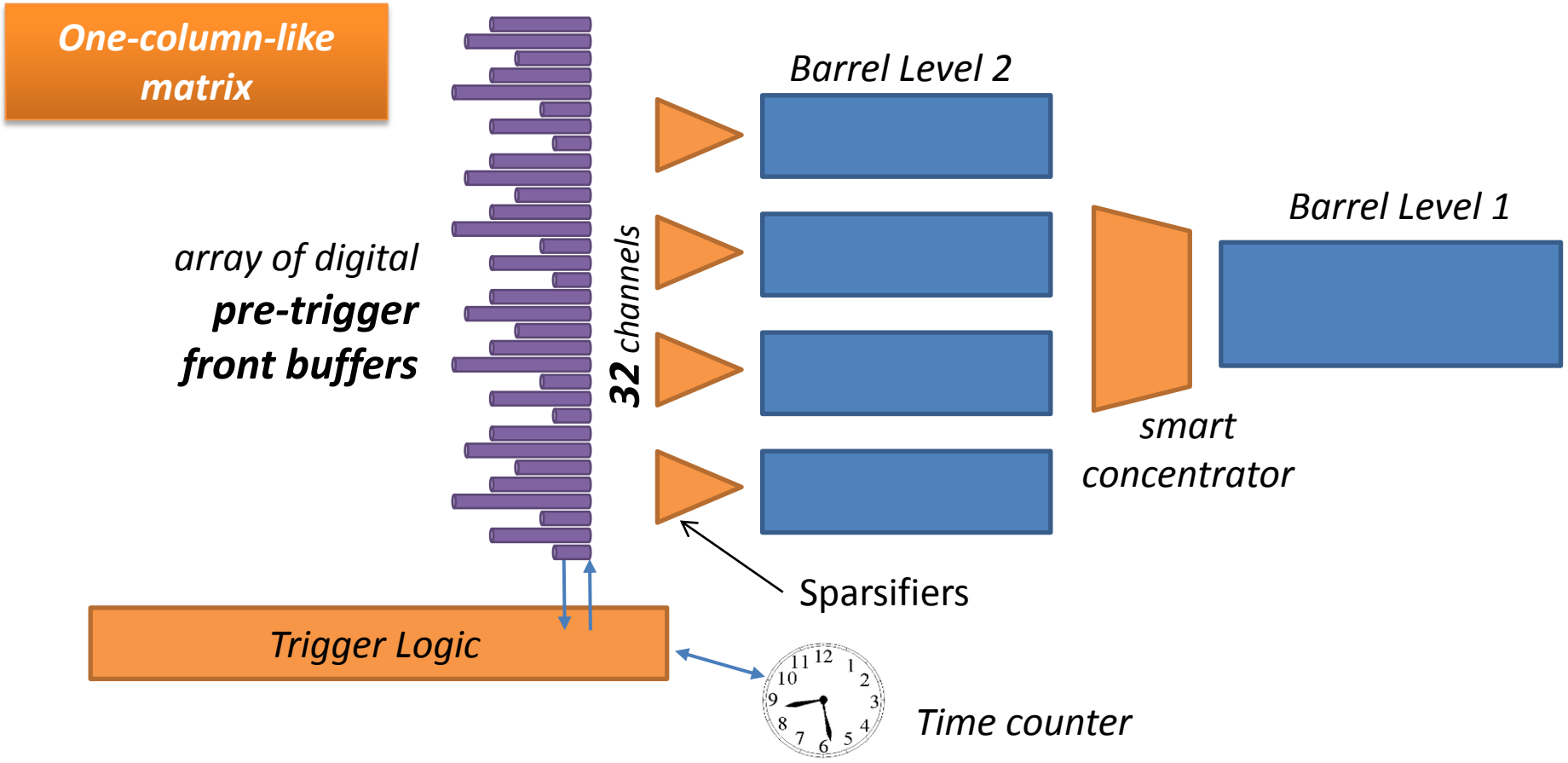
NO pre-trigger front buffer was foreseen in this pixel readout solution.

Pixels latch as **memory bit**.

Higher granularity → lower occupancy

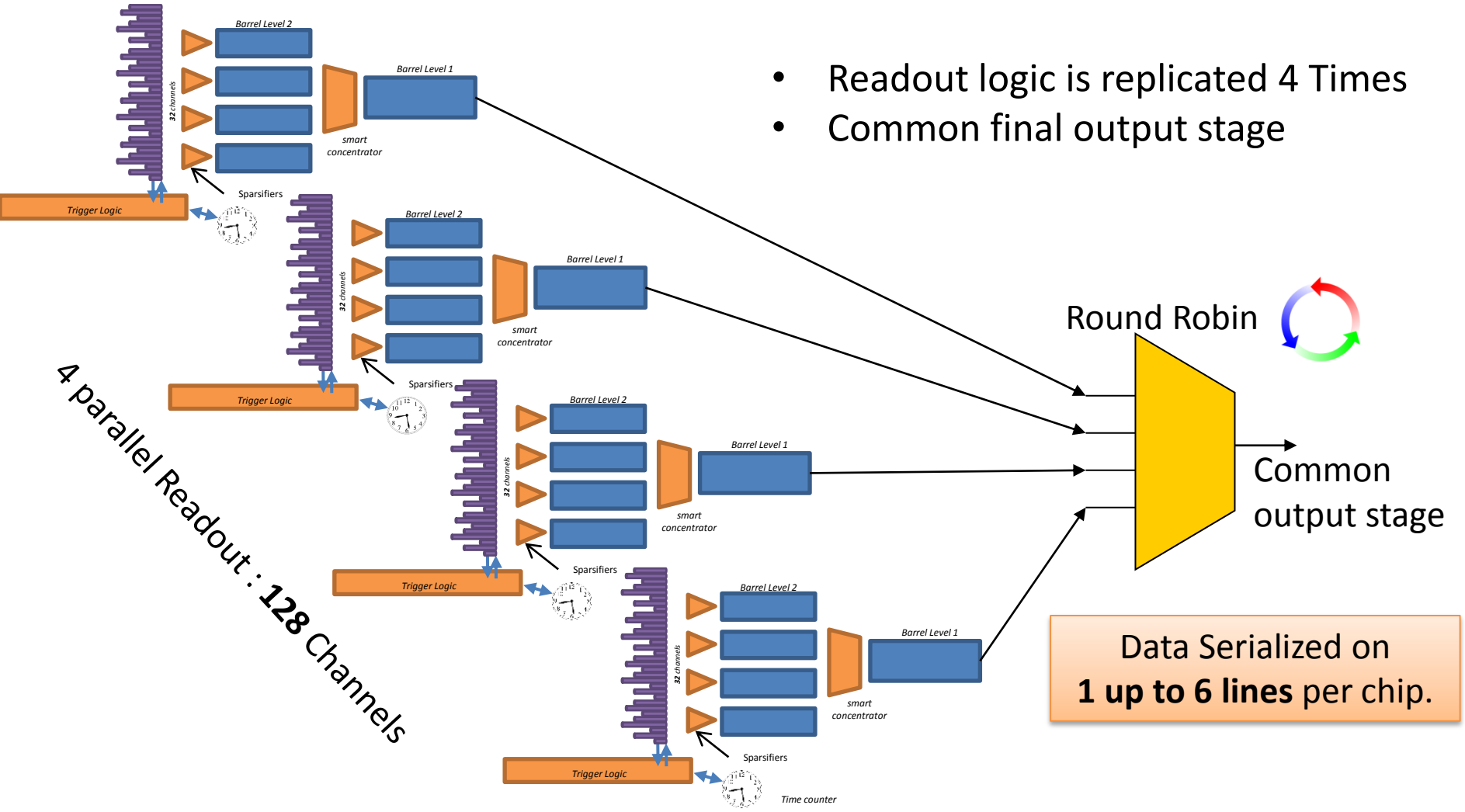
→ **Smoother efficiency drop** w.r.t. **strips**

Strip Front-End Architecture Overview



- **All hits of a triggered time-stamp processed** at a time
- **4 Sparsifiers**: **each** encode up to **8 channels** into 8 words: (TS, Address, ToT …)
- **4 Barrels**: memory elements with **multiple write-access ports** (up to 8) and single output
- **Time ordered** hit flow. Smart concentrator **preserve hit temporal sorting**.

Strip Front-End Architecture Overview



- Readout logic is replicated 4 Times
- Common final output stage

F.E. Chip Data Rates & Serial Links

Layer	Side	Required Bandwidth Mbit/s	Lines at 60 MHz	Lines at 120 MHz	Lines at 180 MHz
0	u	250	6	3	2
0	v	250	6	3	2
1	ϕ	230	5	3	2
1	z	123	3	2	1
2	ϕ	170	4	2	2
2	z	130	3	2	1
3	ϕ	143	3	2	1
3	z	119	3	2	1
4	ϕ	120	3	2	1
4	z	118	3	2	1
5	ϕ	87.6	2	1	1
5	z	76.1	2	1	1

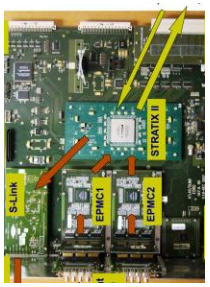
Trigger 150 kHZ

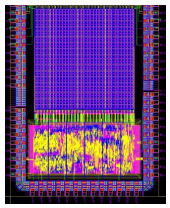
15 % protocol overhead (on Layer0)

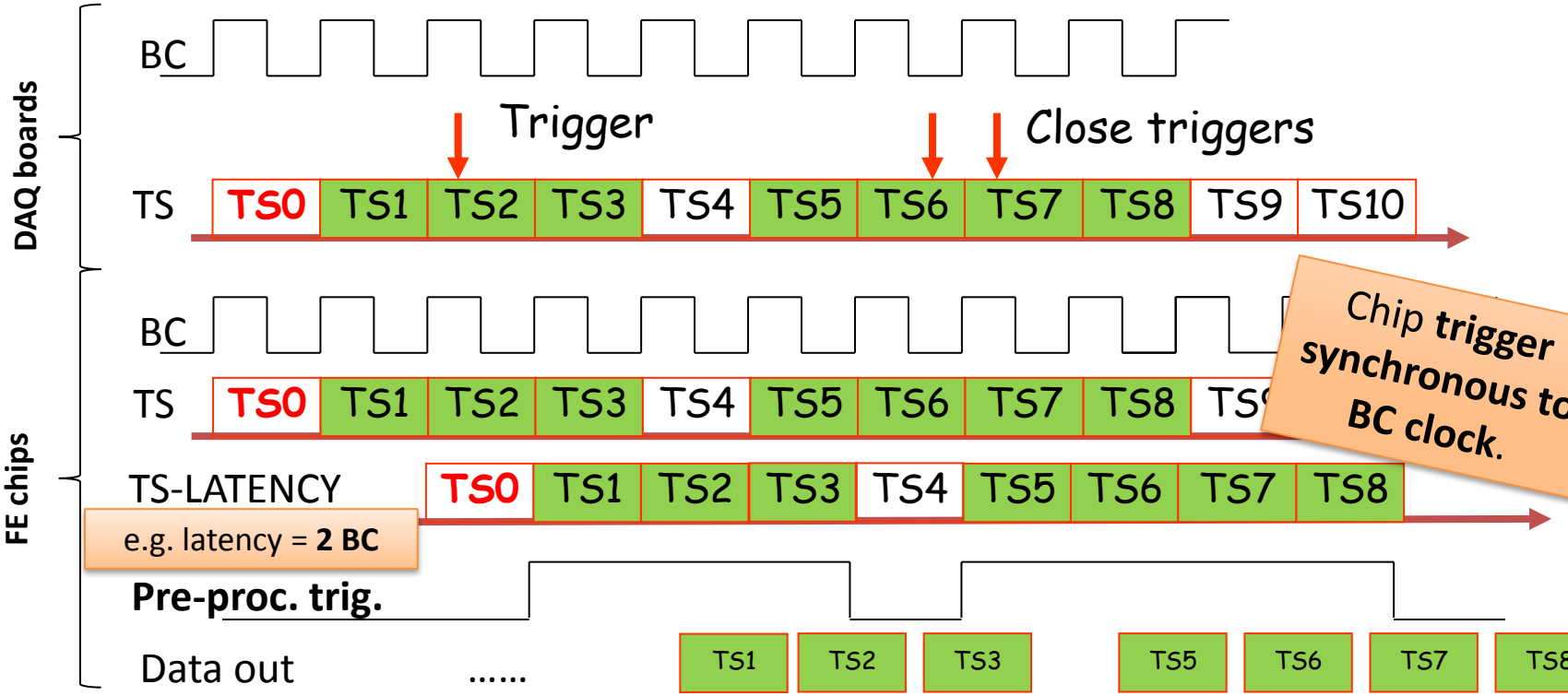
Trigger handling

- External electronic boards process primary trigger signals.
- Pre-processed triggers are sent to front-end electronics.
  - **Fixed trig. latency on chip → configured at start-up**

  → Simpler on-chip trigger logic
  - **Rely on re-configurable logic on external boards for more complicate algorithms.**
- **One-wire trigger** to FE chips.







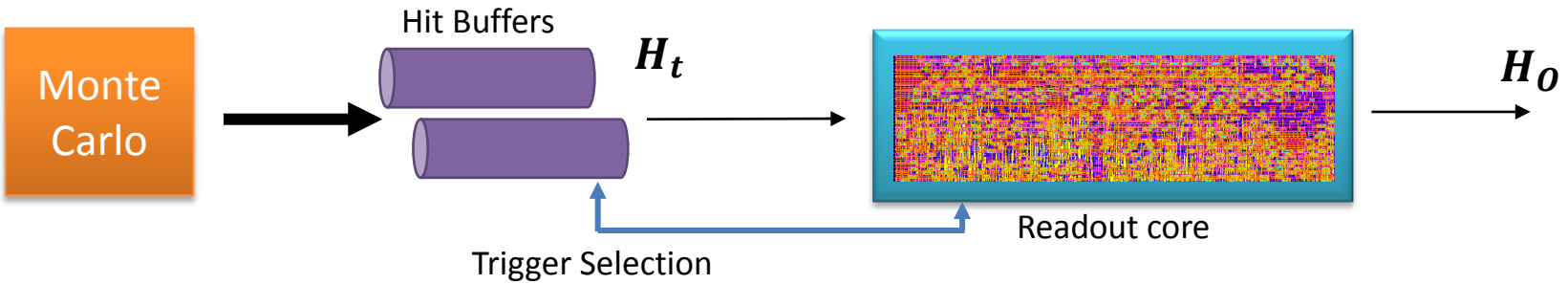
Strip Chip Architecture Simulations

NB: **Only digital readout efficiency taken into account**

- GOALs:
  - Choose optimal front buffer dimensions (trade-off efficiency vs cells saving)
  - Measure ~ 100 % efficiency after pre-trigger buffer insertion
  - Verify functionality of the well-known digital core in the new environment.

- Efficiency evaluation: $1 - \frac{H_t - H_O}{H_t}$

H_t = Hits triggered in digital buffer
H_O = Hits on output



- VHDL test bench and Monte Carlo generator

Strip Chip Architecture Simulations

Conditions:

- **Trigger latency** 6 us
- **Trigger rate** 200 kHz. (SuperB nominal: 150 kHz)
- **Statistics**: Tens of *ms* of operation simulated (→ millions of hits)
- MC hit rate trimmed to **Layer 0 expected rates** with **x5 S.F**.
- **Time stamp resolution**: 30 ns (33 MHz BC clock)

Results:

- **~ 100 % efficiency** observed (digital only)
- Front buffers optimal depth: **32 hits**
  - Deeper front buffers → higher rates/trig. latency handled
- Logical verification of the architecture **OK**

Conclusions

SuperB strip FE chip development:

- **2 front-end chips** under development with different analog characteristics, same digital architecture
- **Analog channel simulated**: shaping time reduction for some layers under evaluation to mitigate background impact
- **Digital readout architecture** mostly inherited from pixel R&D
- Addition of **dedicated FIFOs** as hit buffers during trigger latency
- Whole digital readout architecture simulated (VHDL) with Monte Carlo hit generator: **100% digital efficiency** achievable even for high Layer0 rates: **~1.5 MHz/strip including SF x5**.
- **Higher rates can be handled** increasing **the front buffer size**. (→Higher throughput→ higher number of lines and/or higher line-rate)
- FE chip **work completed for TDR**

Next steps

- First FE chip submission with IBM 130 nm - Nov. 2012

Thanks for your attention

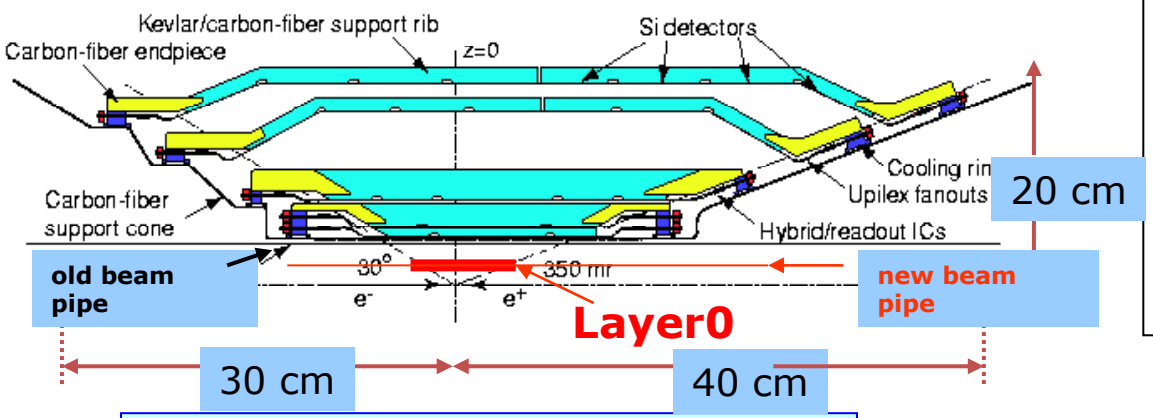
Back Up Slides

The SuperB SVT Collaboration

C. Avanzini[a], G. Batignani[a], S. Bettarini[a], F. Bosi[a], G. Calderini[a], G. Casarosa[a], M. Ceccanti[a], R. Cenci[a], A. Cervelli[a], F. Crescioli[a], M. Dell'Orso[a], F. Forti[a], P. Giannetti[a], M.A. Giorgi[a], A.Lusiani[b], S. Gregucci[a], P. Mammini[a], G. Marchiori[a], M. Massa[a], F. Morsani[a], N. Neri[a], E. Paoloni[a], M. Piendibene[a], A. Profeti[a], G. Rizzo[a], L. Sartori[a], J. Walsh[a], E. Yurtsev[a], M. Manghisoni[c], V. Re[c], G. Traversi[c], M. Bruschi[d], R. Di Sipio[d], B. Giacobbe[d], A. Gabrielli[d], F. Giorgi[d], G. Pellegrini[d], C. Sbarra[d], N. Semprini[d], R. Spighi[d], S. Valentinetti[d], M. Villa[d], A. Zoccoli[d], M. Citterio[e], V. Liberali[e], A. Stabile[e], F. Palombo[e], L. Gaioni[f], A. Manazza[f], L. Ratti[f], V. Speziali[f], S. Zucca[f], D. Gamba[g] , G. Giraudo[g] , P. Mereu[g] , G.F. Dalla Betta[h], G. Soncini[h], G. Fontana[h], M. Bomben[i], L. Bosisio[i], P. Cristaudo[i], D. Jugovaz[i], L. Lanceri[i], I. Rashevskaya[i], L. Vitale[i], G. Venier[i]

(a) Universita degli Studi di Pisa and INFN-Pisa, Italy
(b) Scuola Normale Superiore and INFN-Pisa, Italy.
(c) Universita degli Studi di Bergamo and INFN-Pavia, Italy.
(d) Universita degli Studi di Bologna and INFN-Bologna, Italy.
(e) Universita degli Studi di Milano and INFN-Milano, Italy.
(f) Universita degli Studi di Pavia and INFN-Pavia, Italy.
(g) Universita degli Studi di Torino and INFN-Torino, Italy.
(h) Universita degli Studi di Trento and INFN-Padova, Italy.
(i) Universita degli Studi di Trieste and INFN-Trieste, Italy.

Silicon Vertex Tracker



BaBar SVT

5 Layers of double-sided Si strip sensor

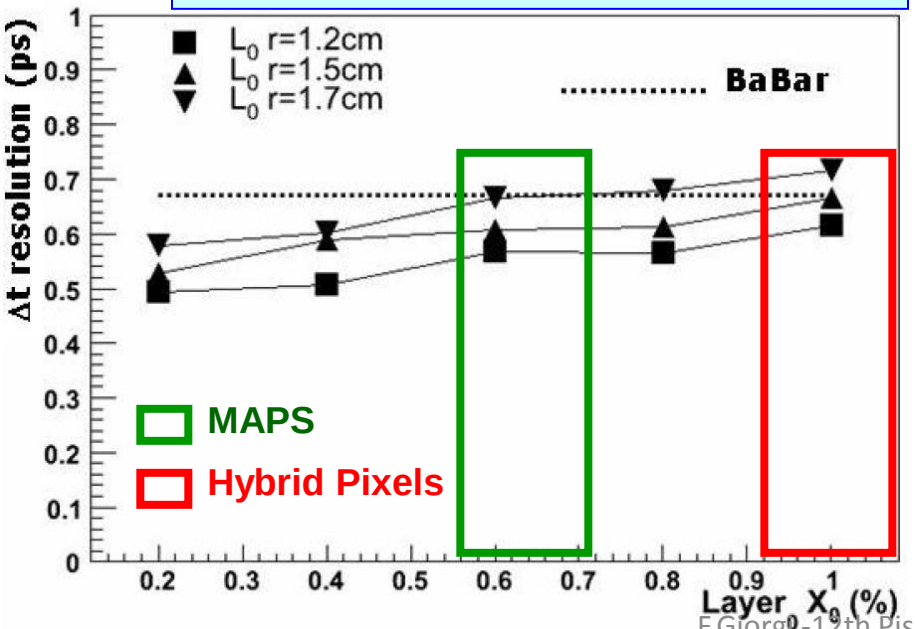
Low-mass design. (P_t < 2.7 GeV)

Stand-alone tracking for slow particles.

97% reconstruction efficiency

Resolution ~15μm at normal incidence

B→π π decay mode, βγ=0.28, beam pipe X/X0=0.42%, hit resolution =10 μm



Design based on the 5-layer Babar SVT (R>3cm)

BUT:

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- Layer0 **area 100 cm²**

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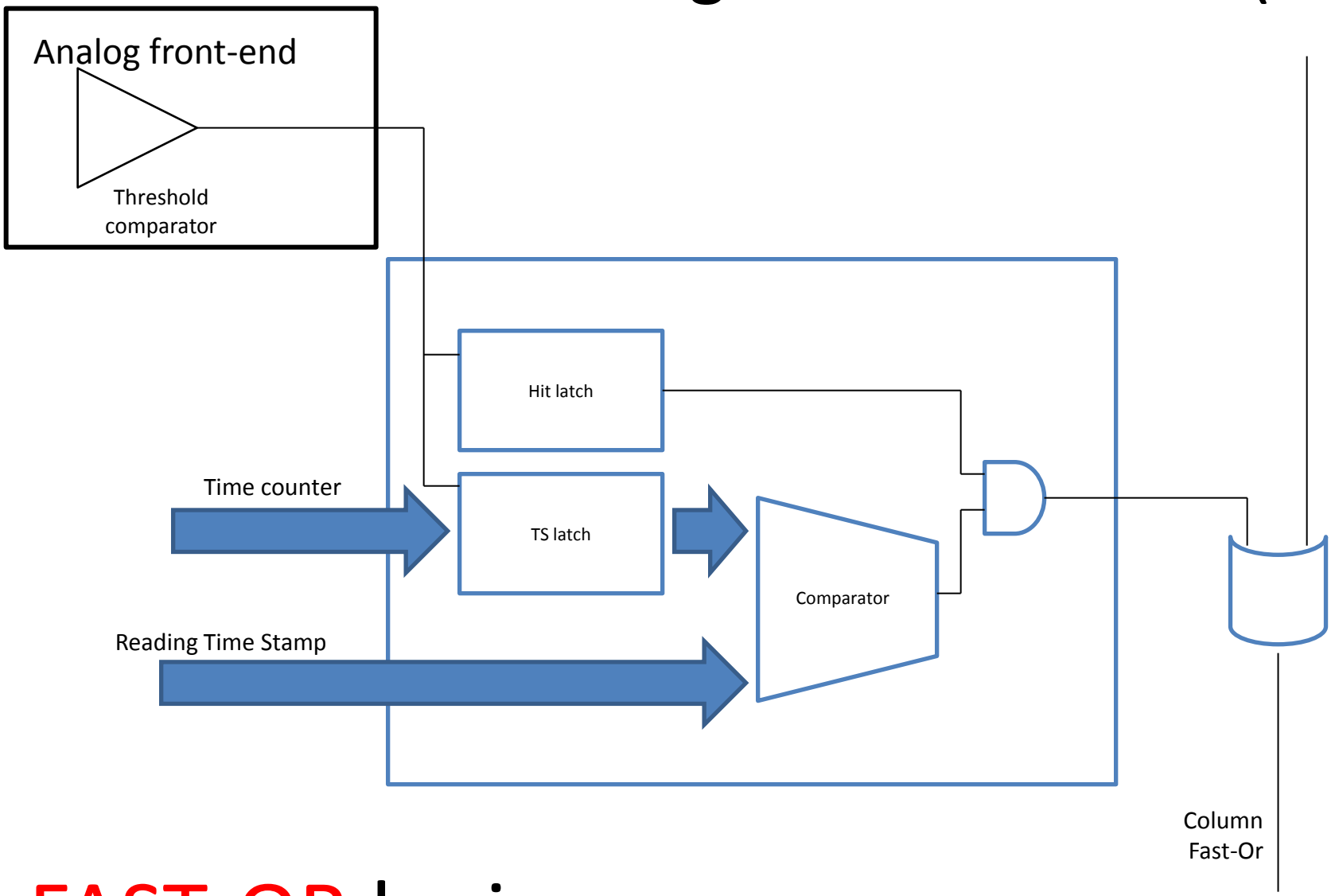
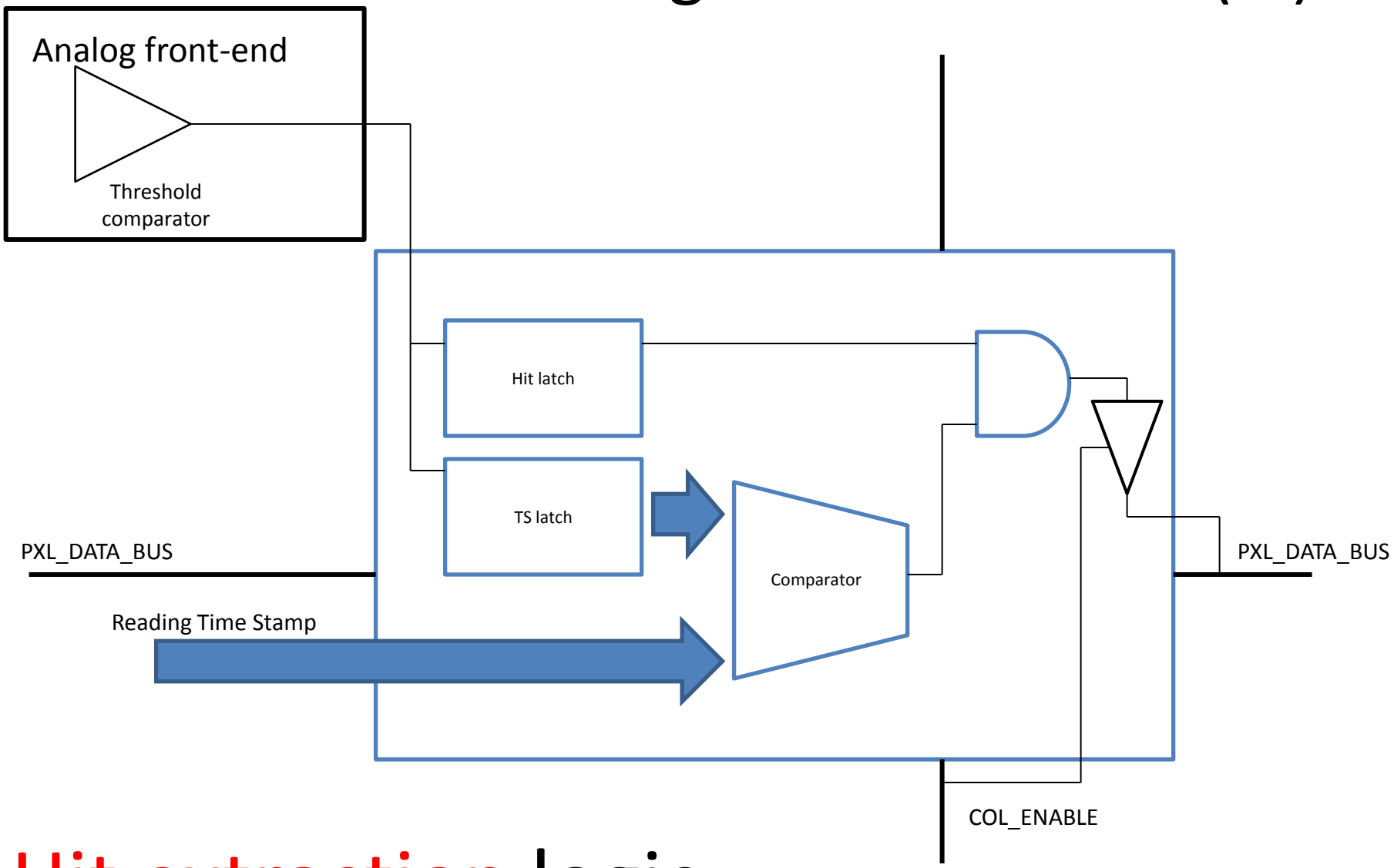
Pixel digital architecture (PI)



FAST-OR logic

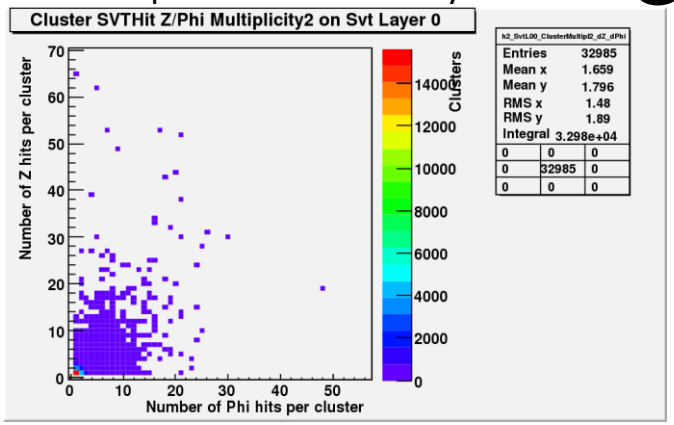
Pixel digital architecture (PI)



Hit extraction logic

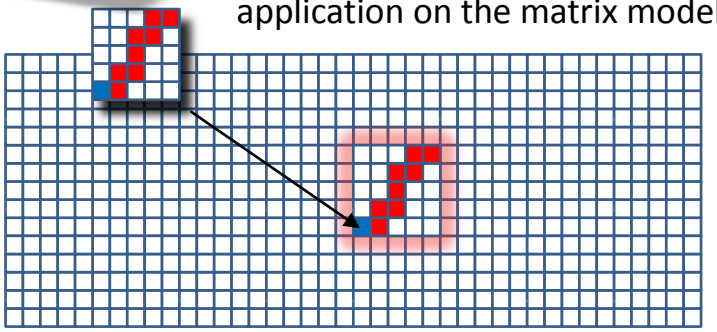
Cluster generator inherited by pixel test bench

Input Cluster spread dist. From Physics



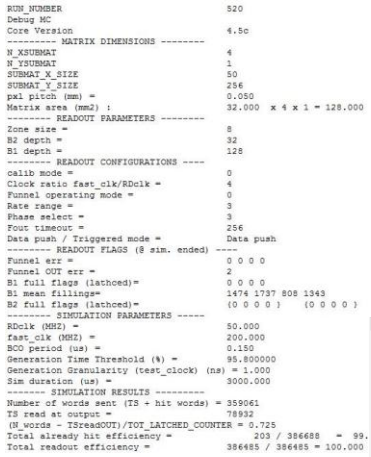
→

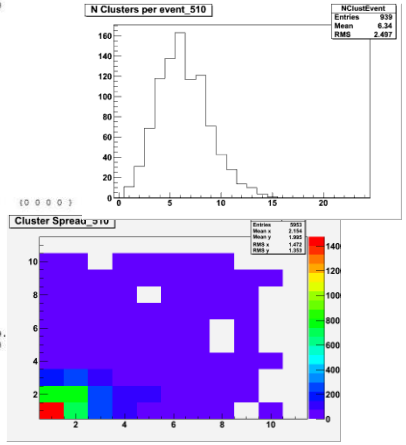
MC hit extraction and application on the matrix model



Monte Carlo tuned to obtain 100 MHz/cm^2 **hit** rate on area

C++ Reports, efficiency check, analysis tools …





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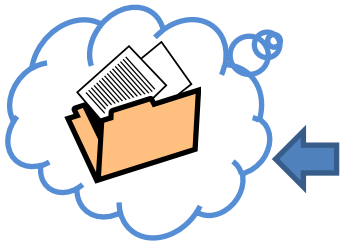
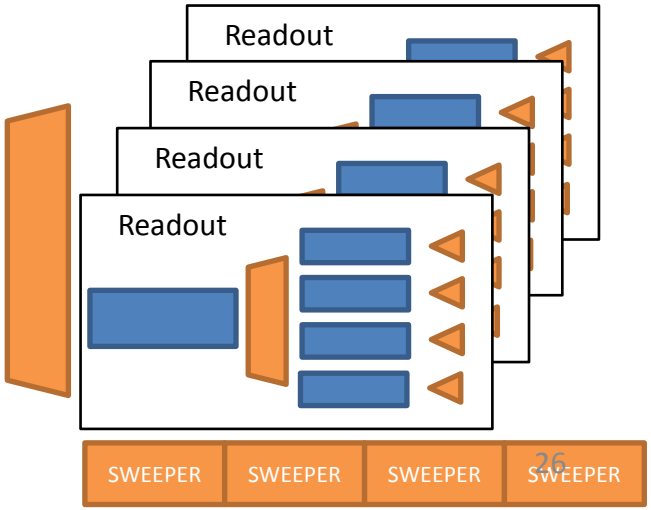


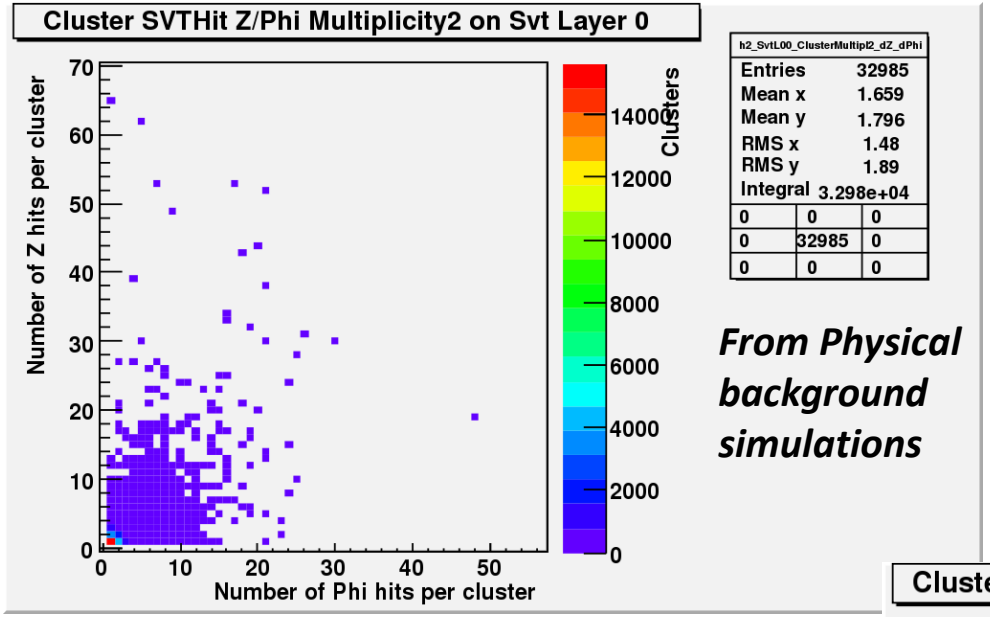
Generation of report files

↓ Simulating hit extraction, encoding and sequencing



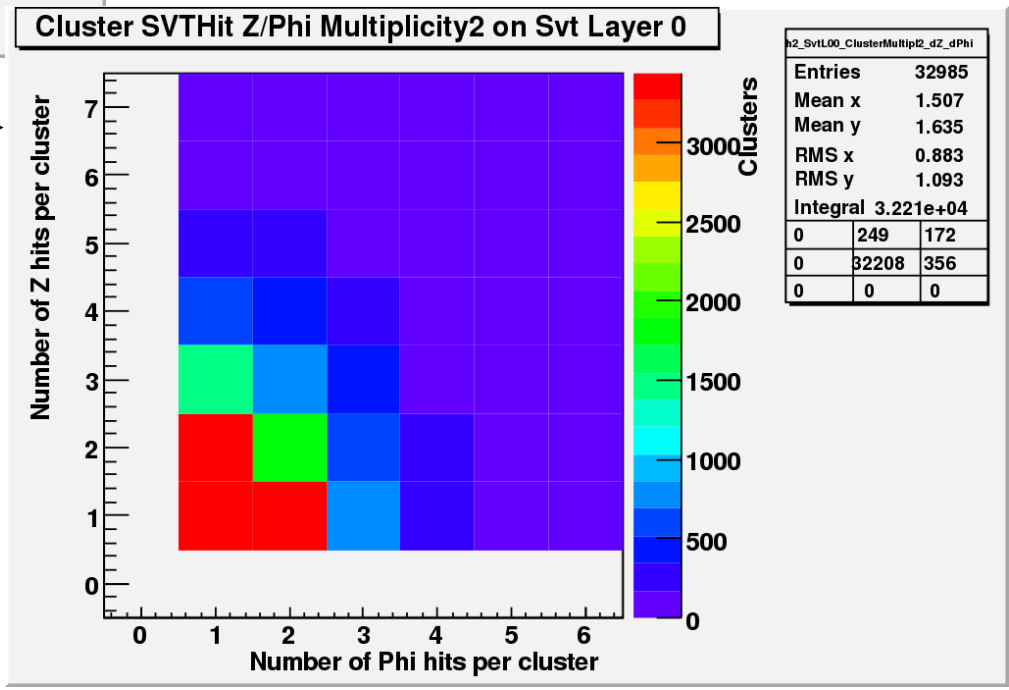
cluster spread distribution

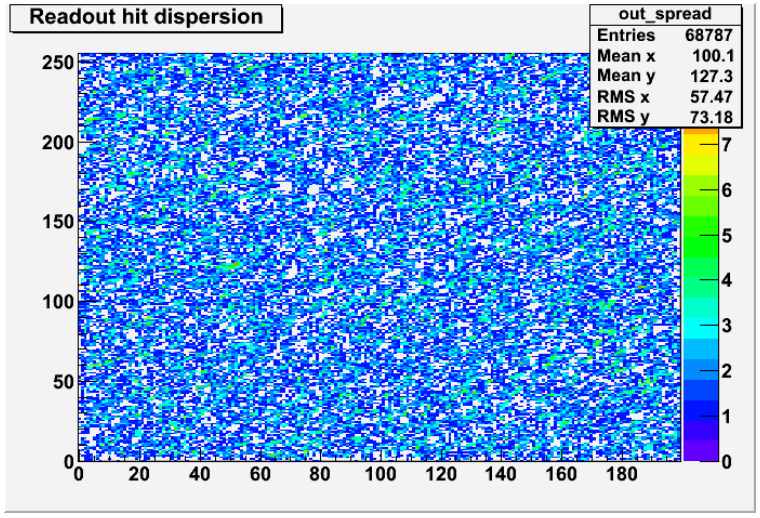
zeta/phi from physics simulations



From Physical background simulations

Zoom IN





Simulated architecture:
few clustered events read out

Simulation results

2 MHz/strip : Layer 0

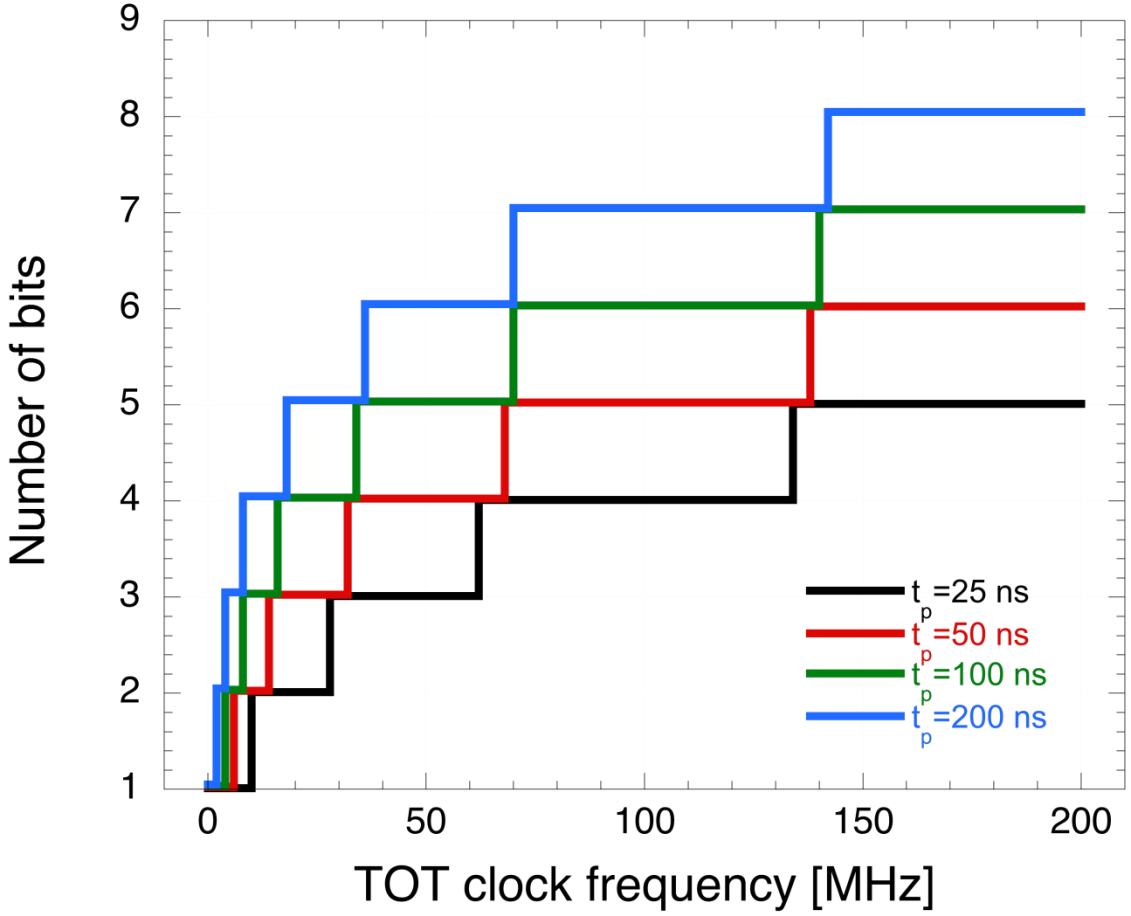
buffer size	16	32	64
buffered hits	3.8 M	12.9 M	12.9 M
of which triggered	23363	76850	23363
output triggered hits	14679	76849	23363
triggered hit lost	8684	1	0
Efficiency (%)	**62.8**	**99.9987**	**100**

760 kHz/strip : Layer 1

buffer size	8	16	32
buffered hits	1.4 M	7 M	7 M
of which triggered	8748	28829	28829
output triggered hits	6788	28825	28829
triggered hit lost	1960	4	0
Efficiency (%)	**77.6**	**99.986**	**100**

TOT counter bit number

Shaper linearity over the full signal dynamic range (15 MIPs) is assumed



Uncertainty in the estimation of t_0

$$t_0 = t_{th} - \mathrm{t_{walk}}$$

Layer	t_p [ns]	$t_p/T_{CK,TOT}$	$f_{CK,TS}$ [MHz]	σ_{walk} [ns]	σ_{t0} [ns]
0	25	4	30	1.6	9.8
1	100	4	30	6.2	11.4
2	100	4	30	6.2	11.4
3	200	4	30	12.5	15.8
4	500	4	30	31.2	32.6
5	1000	4	30	62.5	63.2

Actually σ_{walk} gets smaller for larger values of TOT, so better estimation of t_0 could be obtained

Layer	Hit rate/strip [kHz]	Peaking time [ns]	Efficiency - random waveform generation	
			safety factor 5 included	no safety factor
0 – side 1	933	25	0.955	0.991
0 – side 2	937	25	0.967	0.994
1 - phi	853	50	0.943	0.989
		75	0.917	0.983
		100	0.889	0.979
1 - z	671	50	0.938	0.987
		75	0.908	0.981
		100	0.879	0.975

Layer	Hit rate/strip [kHz]	Peaking time [ns]	Efficiency - random waveform generation	
			safety factor 5 included	no safety factor
2 - phi	668	50	0.952	0.990
		75	0.927	0.985
		100	0.903	0.980
2 - z	667	50	0.941	0.988
		75	0.912	0.982
		100	0.881	0.976
3 - phi	580	100	0.877	0.975
		150	0.815	0.962
		200	0.765	0.948
3 - z	397	100	0.929	0.985
		150	0.896	0.978
		200	0.863	0.971