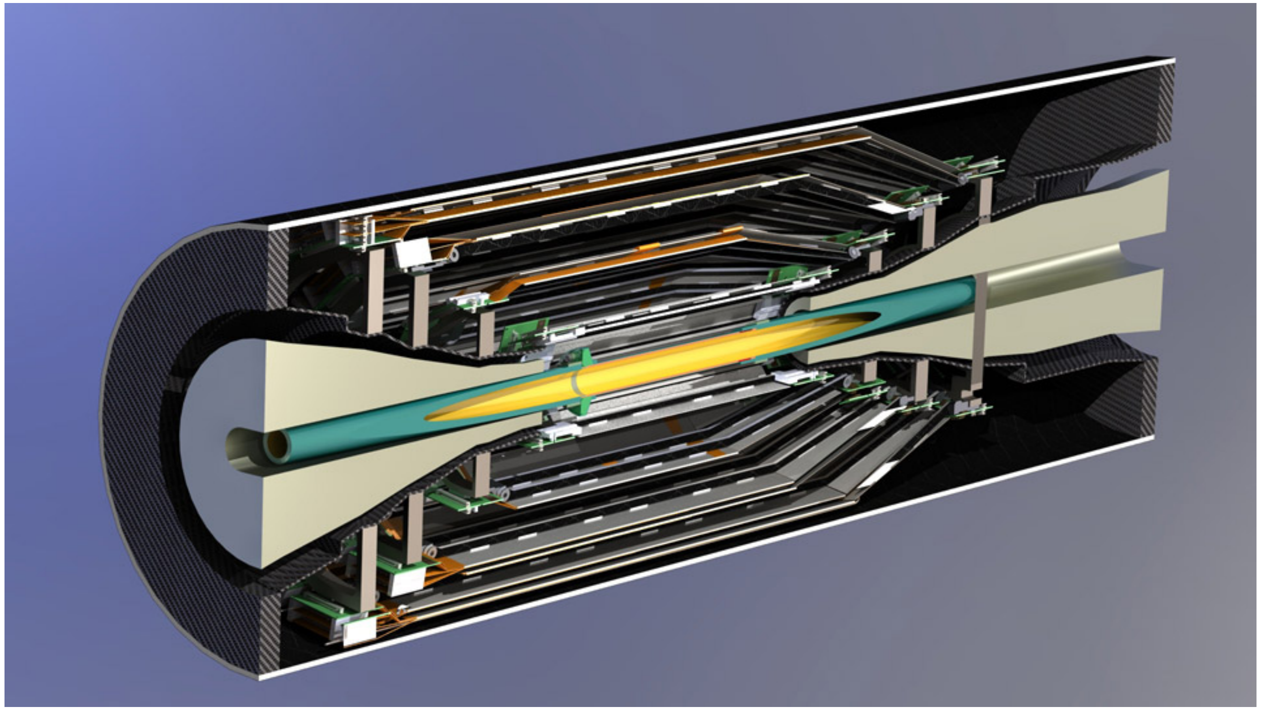
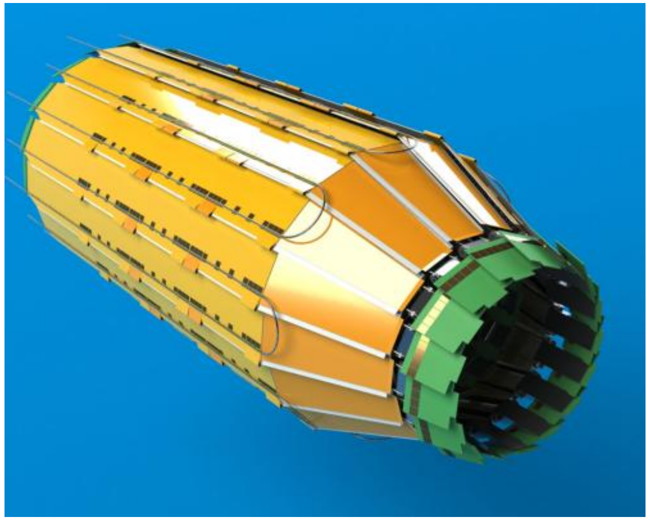
Institute of High Energy Physics



The Silicon Vertex Detector of the Belle II Experiment

Thomas Bergauer (HEPHY Vienna)

12th Pisa Meeting on Advanced Detectors 24. May 2012



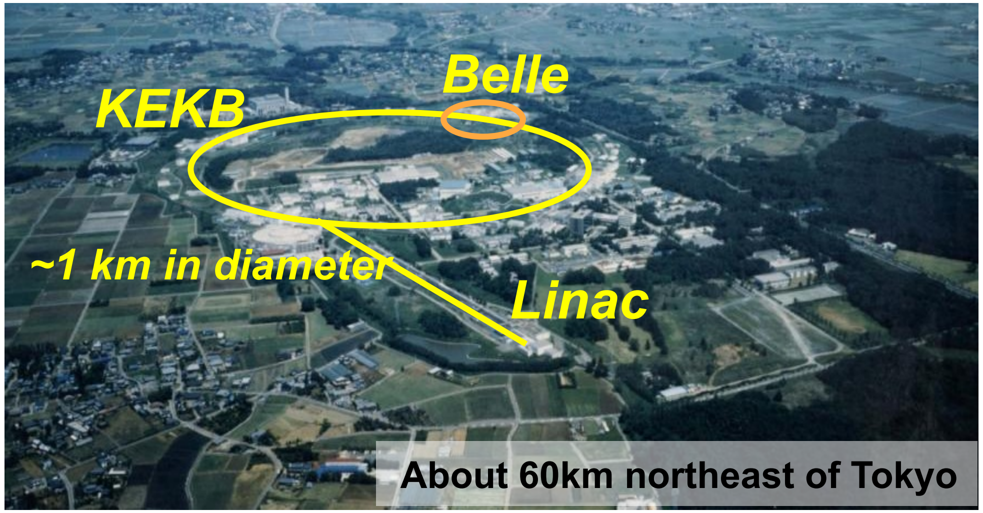
Belle and Belle II

DEPFET Pixel Detector

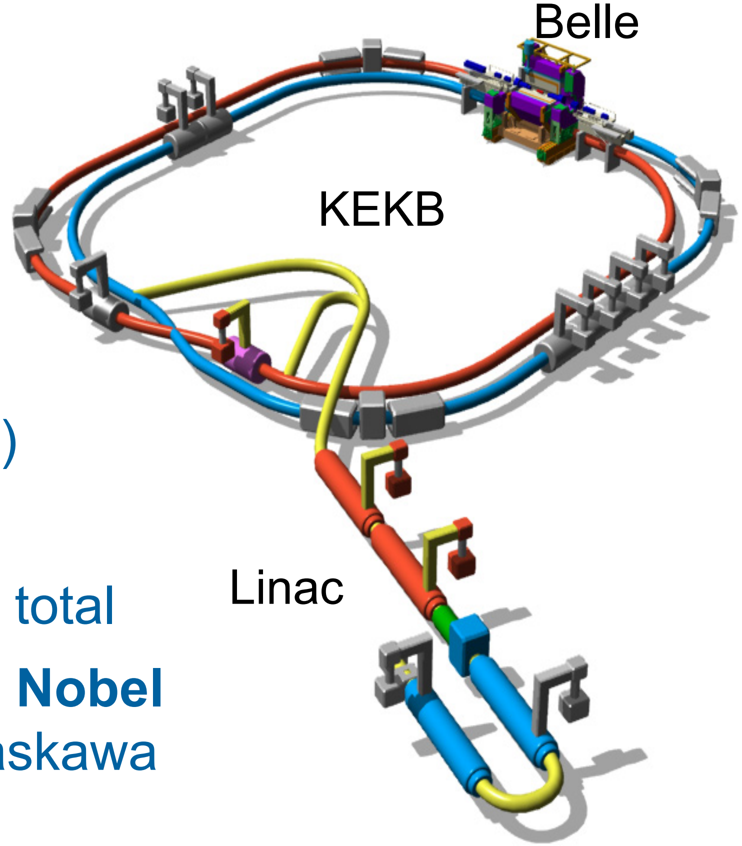
Double-sided Strip Detector

Summary

KEKB and Belle @ KEK (1999-2010)

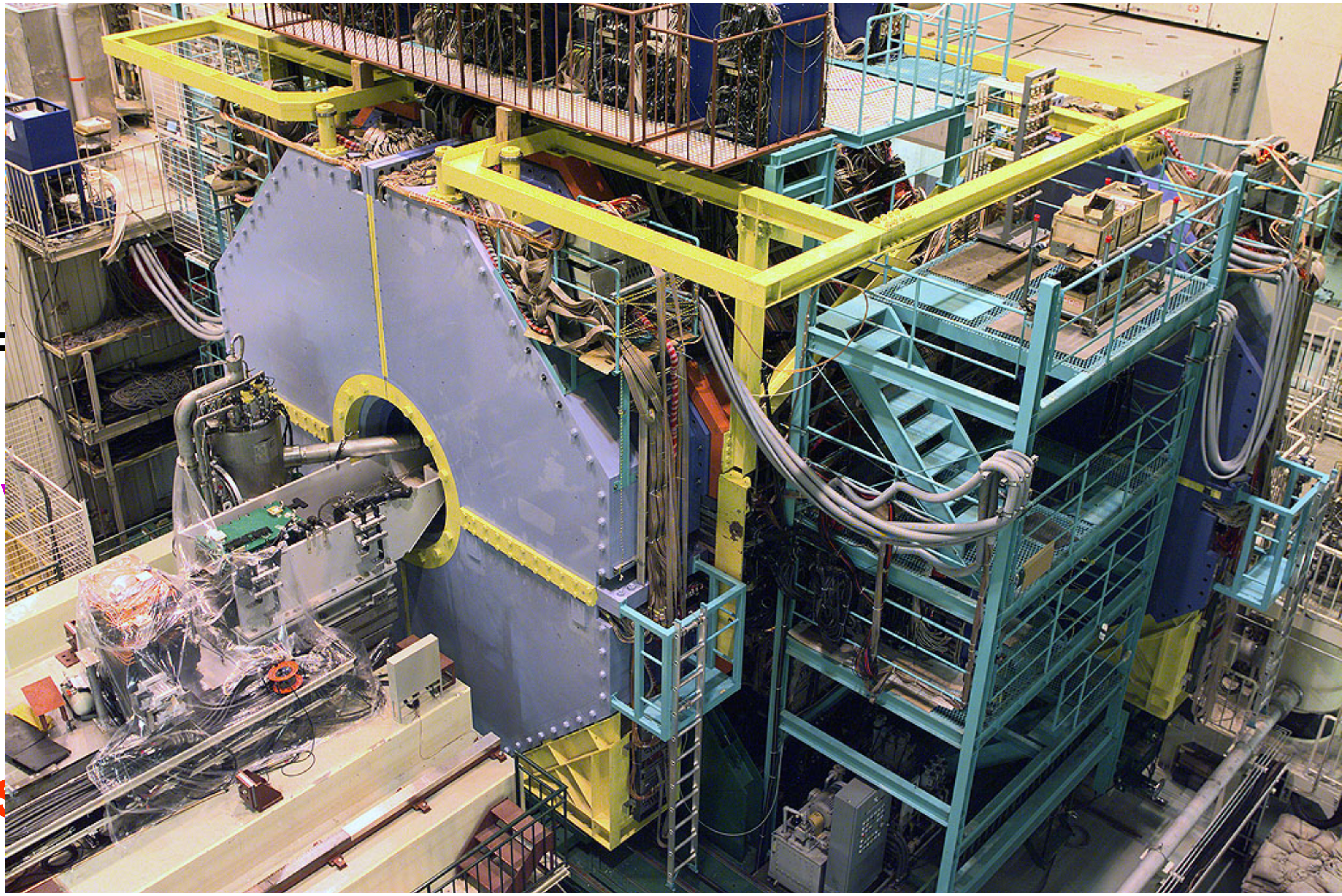


- **Asymmetric** machine: 8 GeV **e⁻** on 3.5 GeV **e⁺**



- Center of mass **energy**: Υ(4S) (10.58 GeV)
- **High intensity** beams (1.6 A & 1.3 A)
- Integrated luminosity of **1 ab^{-1} recorded** in total
- Belle mentioned explicitly in **2008 Physics Nobel Prize** announcement to Kobayashi and Maskawa

Belle Detector (1999–2010)



ter

TOF

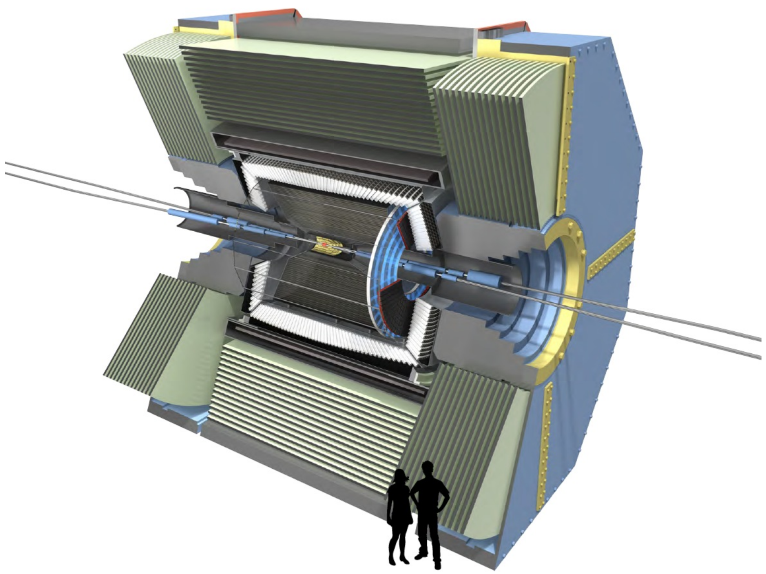
8 Ge

er

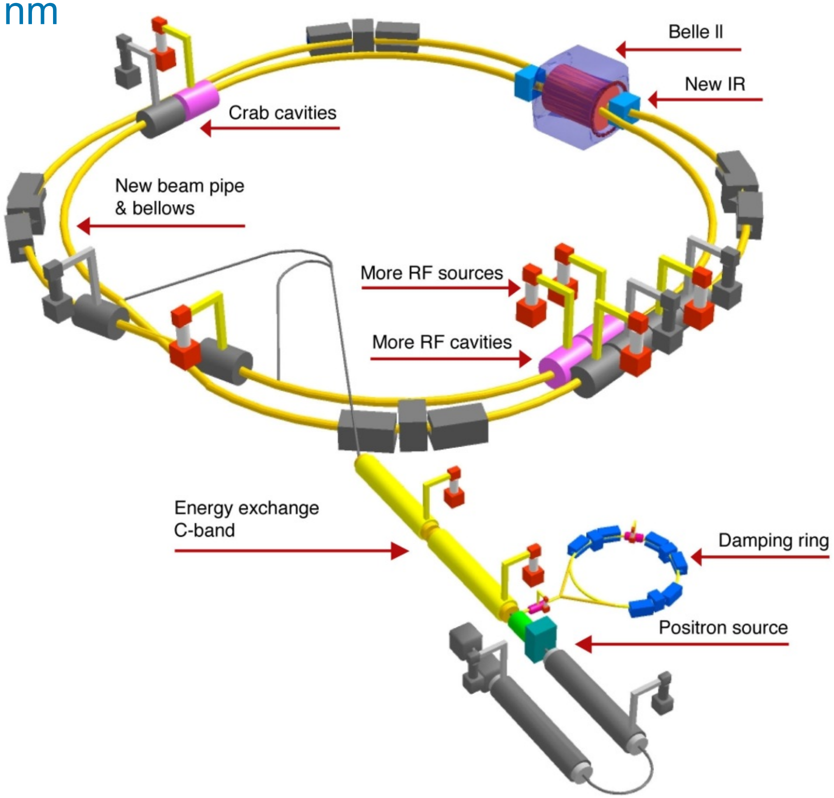
$_2H_5$

SuperKEKB/Belle II Upgrade: 2010–2015

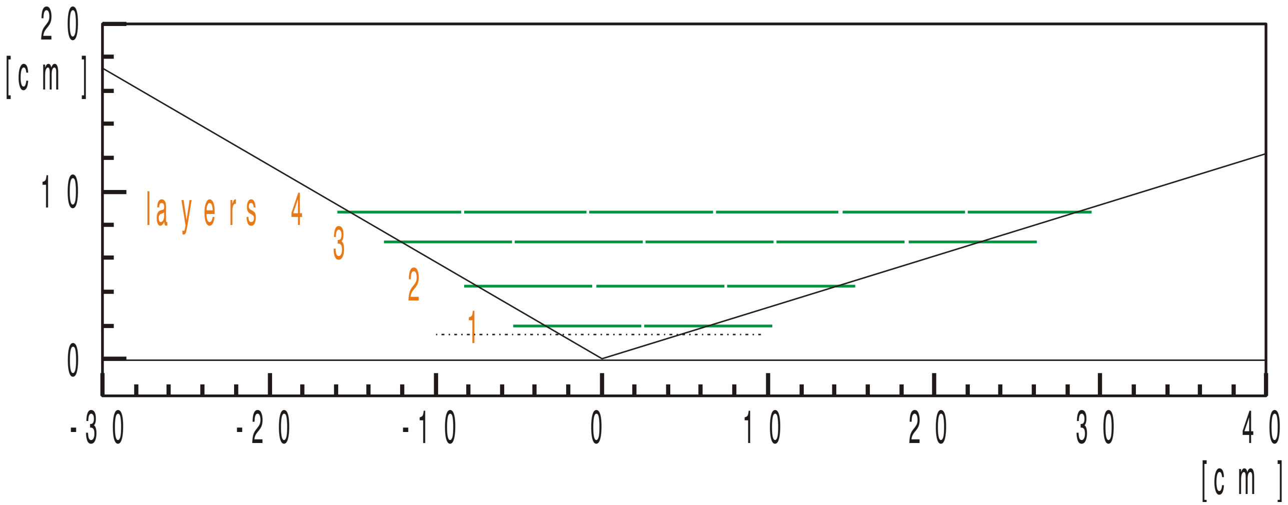
- Aim: super-high luminosity ~$8{\times}10^{35}$ $cm^{-2}s^{-1}$ → $1{\times}10^{10}$ $B\overline{B}$ / year
- LoI published in 2004; TDR published in 2010
- Refurbishment of accelerator and detector required
  - nano-beams with cross-sections of ~10 μm x 60 nm
  - 10 mm radius beam pipe at interaction region



http://belle2.kek.jp

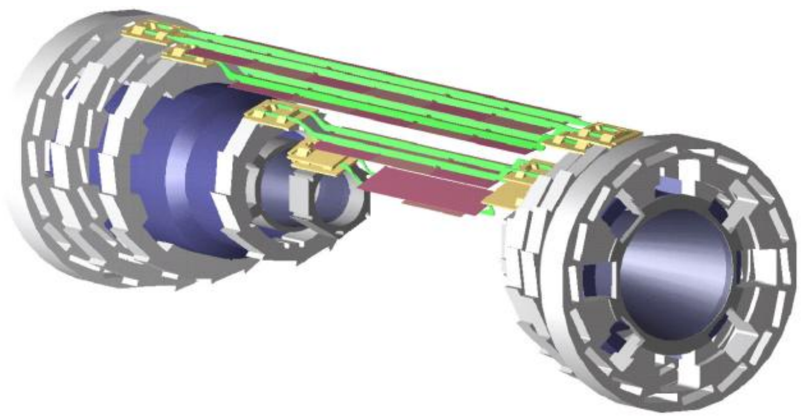


Previous SVD Layout (until 2010)



- **4 straight layers** of **4" double-sided silicon detectors** (DSSDs)
- Outer radius of r~8.8 cm

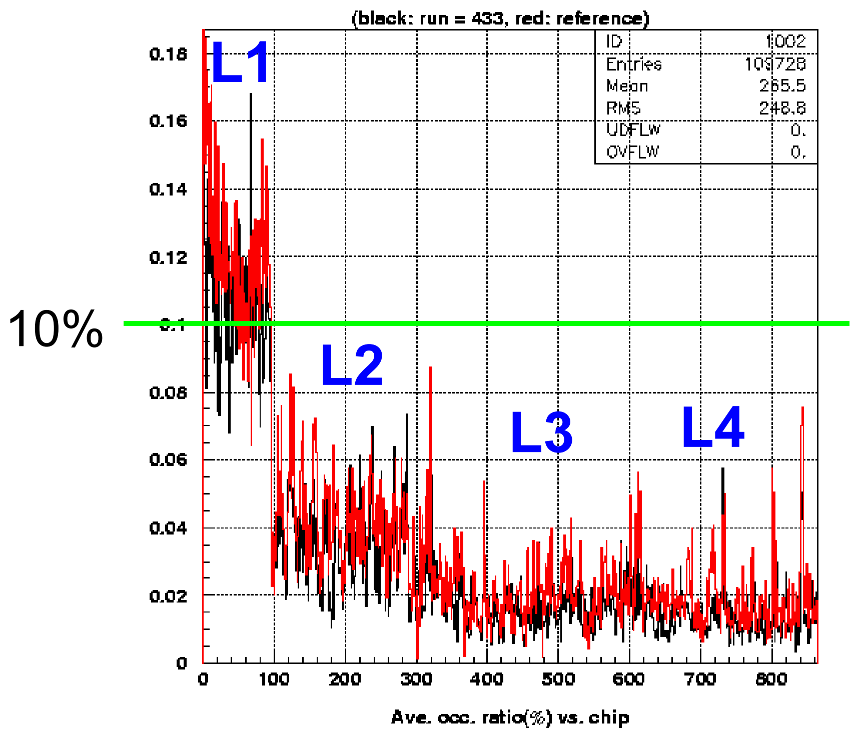
- **Up to three 4" sensors are daisy- chained** and read out by one hybrid located outside of acceptance region (VA1 chip)



Belle Silicon Vertex Detector (SVD)

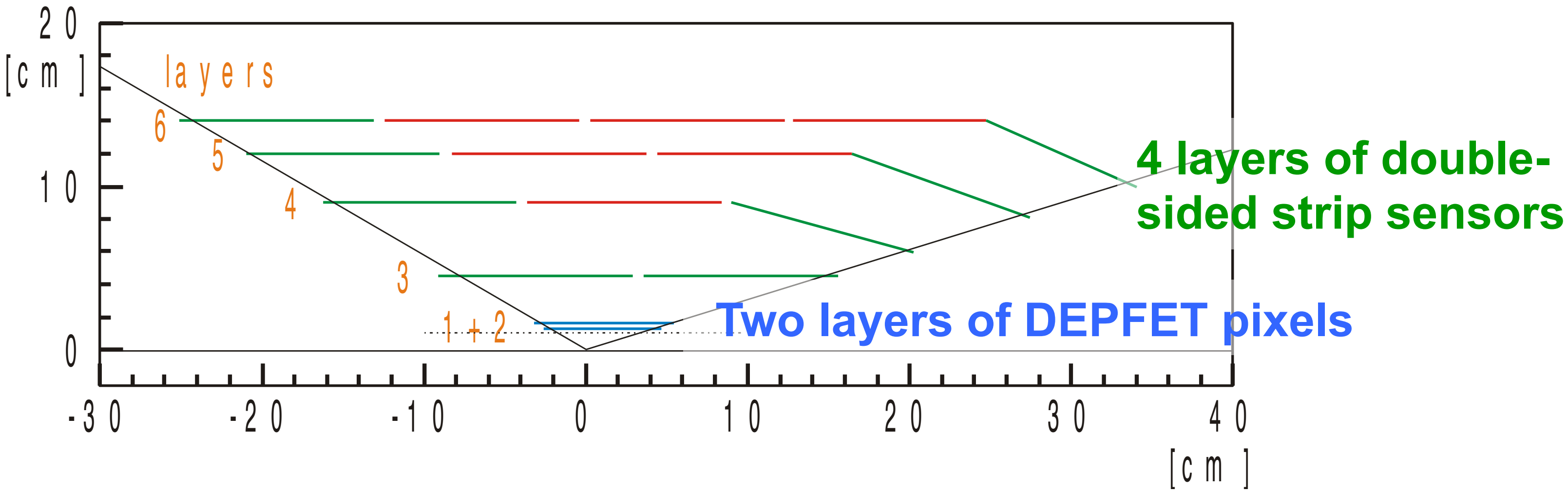
- Previous SVD limitations were
  - **occupancy** (currently ~10% in innermost layer) → need faster shaping
  - **dead time** (currently ~3%) → need faster readout and pipeline

- Belle II needs detector with
  - high **background tolerance**
  - **pipelined** readout
  - **robust tracking**
  - **low material budget** in active volume



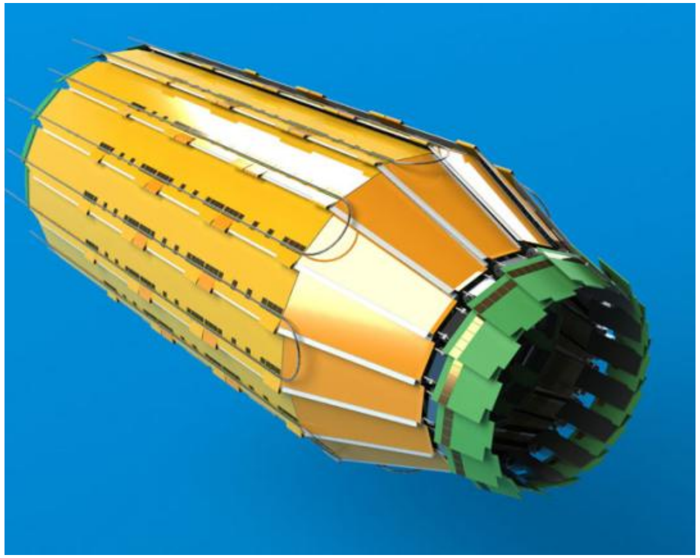
Current SVD is not suitable for Belle II

New Layout for Belle II SVD (2014-)

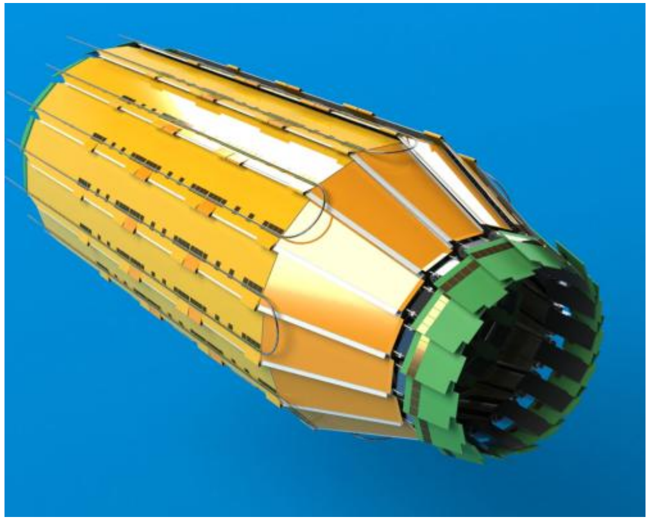


- New double-layer pixel detector using **DEPFET** technology
- Four layers with 6” **double-sided strip detectors** and **forward part**

optimized for precision vertex reconstruction of the decays of short-lived B-mesons



Belle II



Belle and Belle II

DEPFET Pixel Detector

Double-sided Strip Detector

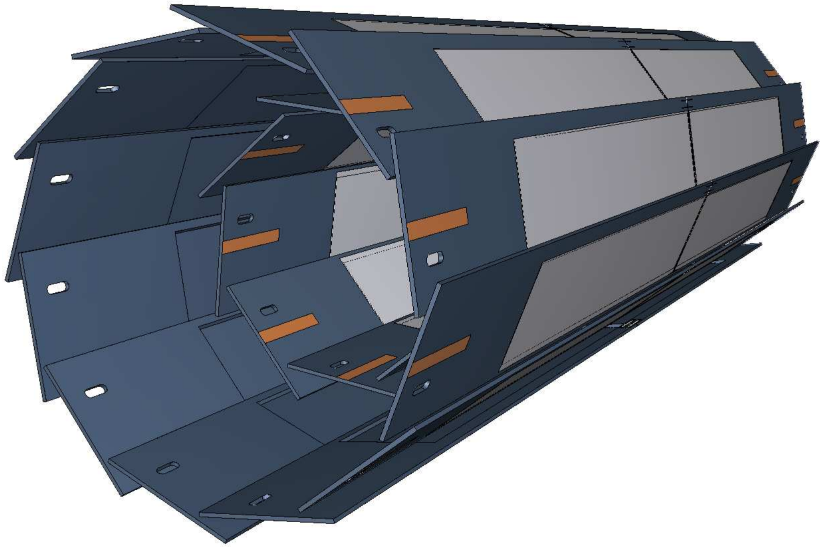
Summary

DEPFET Active Pixel Detector

DEPFET PXD Posters:

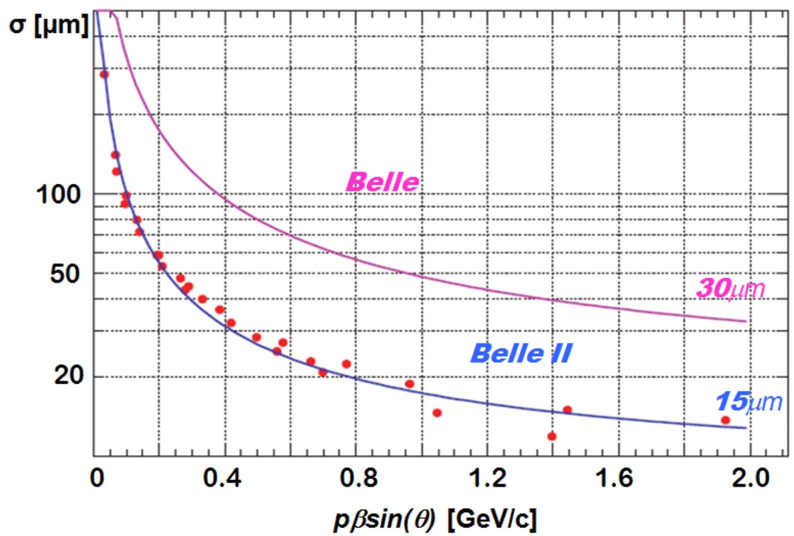
- Ultra-thin fully depleted DEPFET active pixel sensors for future e+/e- colliders– C. Koffmane
- The DEPFET Active Pixels for Belle II - Resolution in 50 micron thinned Sensor – P. Kodys

The DEPFET Belle-II PXD



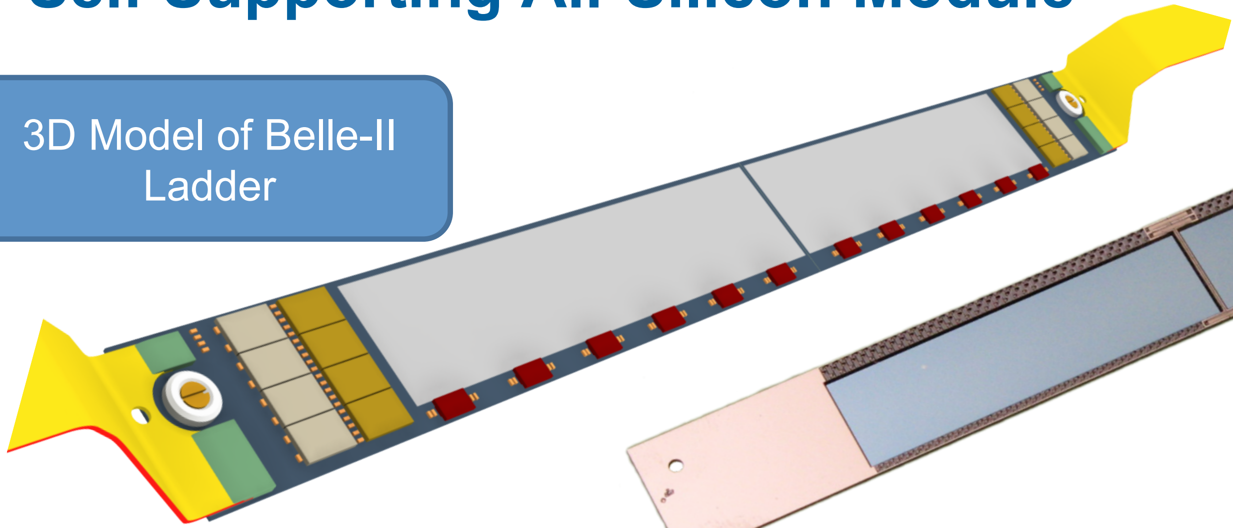
- Two layers mounted onto beam-pipe
- Angular coverage 17°<θ < 155°
- material budget below 0.5 % X_0
- low power density of 0.1 W/cm^2
- background occupancy to 1 - 3 %
- z vertex resolution significantly improved (PXD & SVD) compared to Belle-I

	Inner layer	Outer layer
# ladders	8	12
Sens. length	90 mm	123 mm
Radius	1.4 cm	2.2 cm
Pixel size	50x50 µm^2	50x75 µm^2
# pixels	1600(z)x250(R-ϕ)	1600(z)x250(R-ϕ)
Thickness	75 µm	75 µm
Frame/row rate	50 kHz/10 MHz	50 kHz/10 MHz



Self Supporting All-Silicon Module

3D Model of Belle-II Ladder



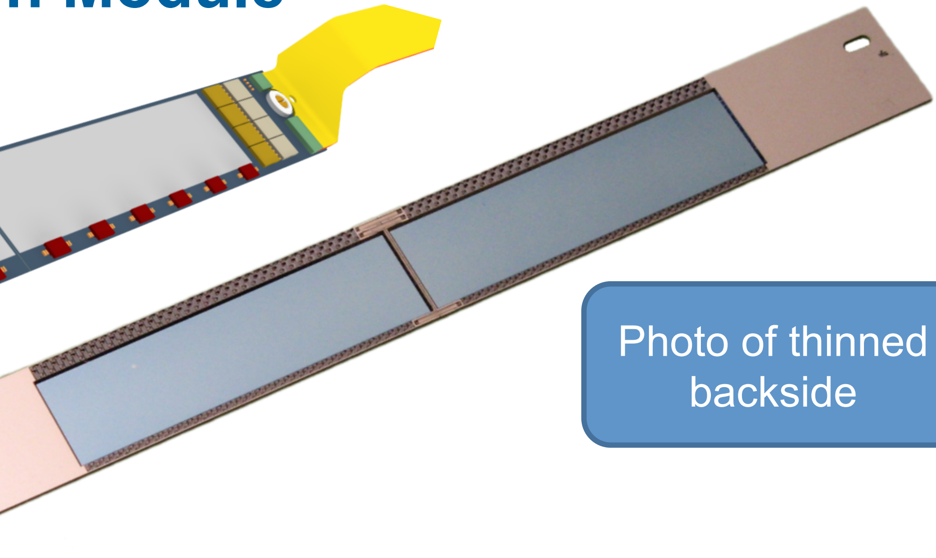
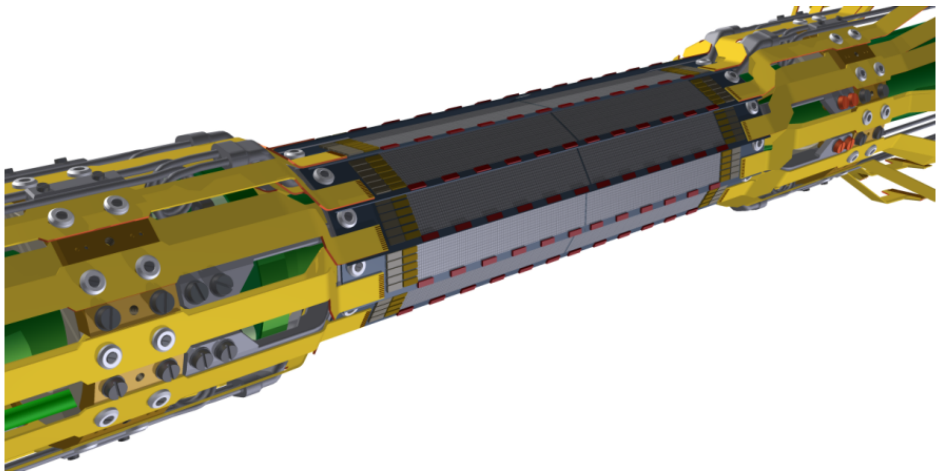
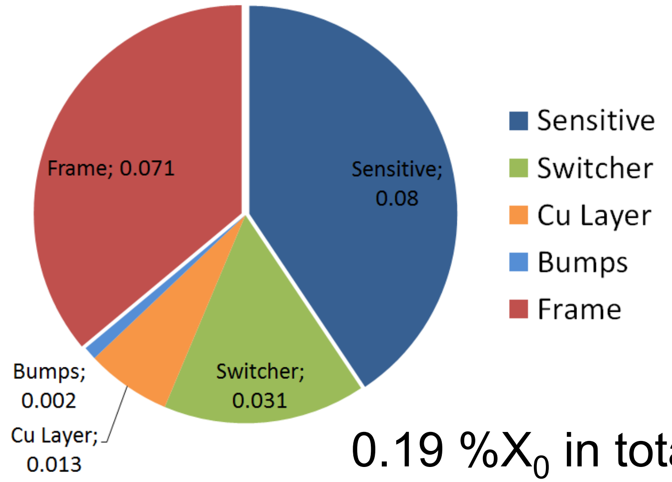


Photo of thinned backside



Material Budget Distribution:

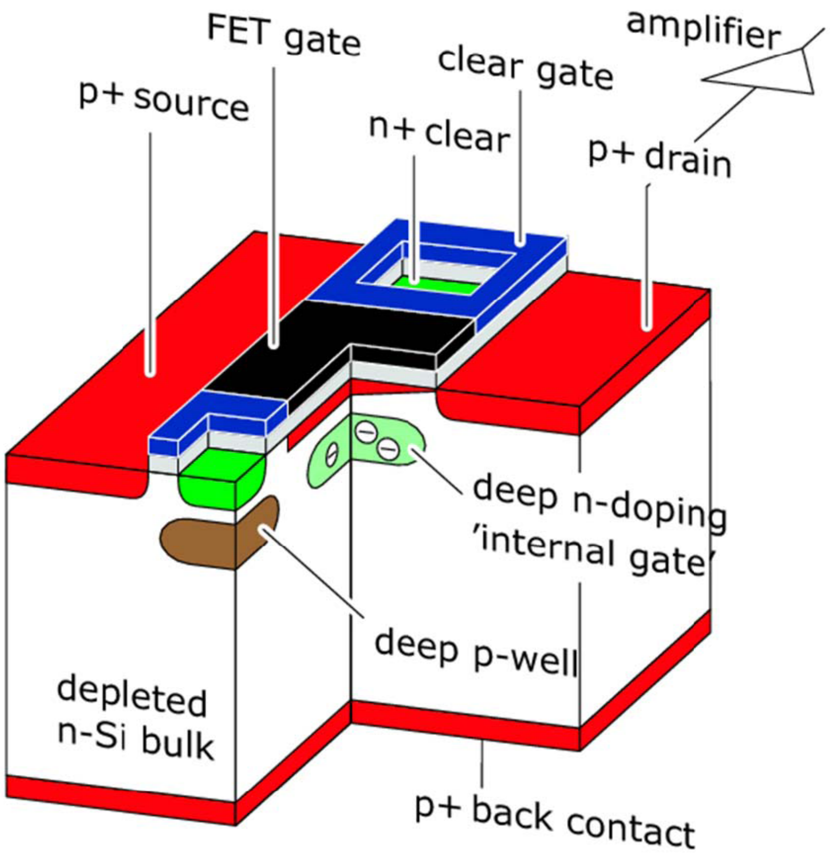


$0.19\ \%X_0$ in total

DEPFET Sensors

- DEPFET = depleted p-channel field effect transistor
- Fully depleted sensitive volume

- Charge collection in the "off" state, read out on demand
- Modulation of the FET current by the charge in the internal gate
- *Clear contact* to empty the internal gate

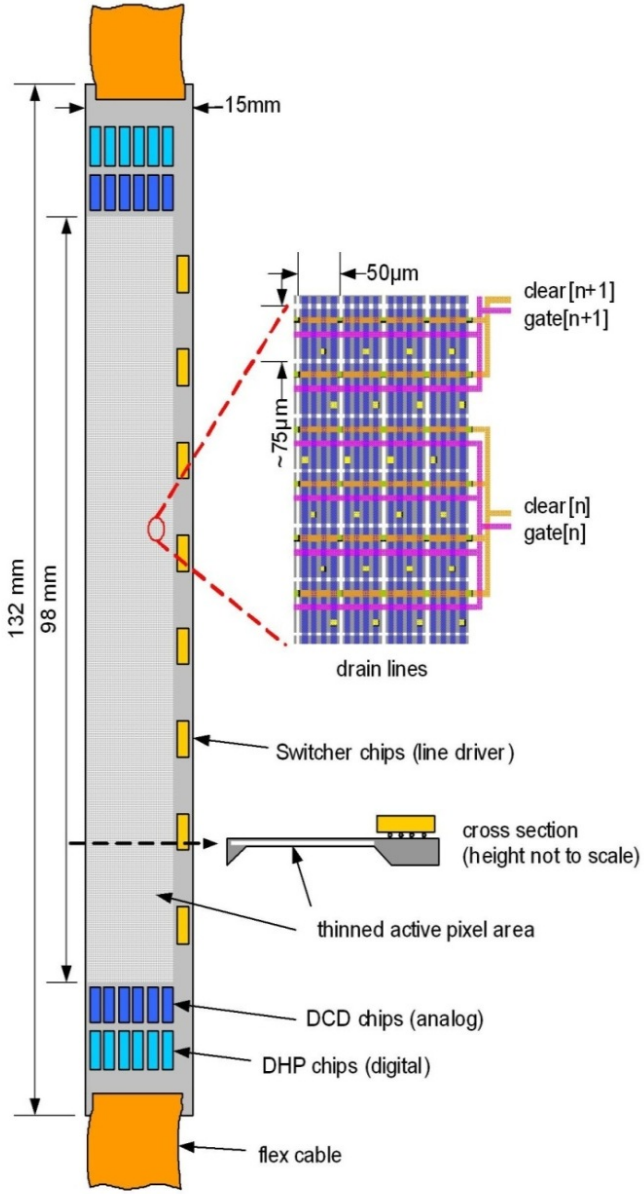


PXD Module Read-out

- **Switcher** devices control the GATE and CLEAR (reset) lines
- **DCD** (**Drain Current Digitizer**) is the readout chip with A/D converters
- **DHP** (**Digital Handling Processor**) chips - first-stage preprocessing and data reduction

→ Belle II PXD produces **huge** data streams: raw **180 GB/s** (20 PXD ladders, 8M pixels in total, occupancy up to 3%, trigger rate of 30kHz)

→ Data reduction necessary



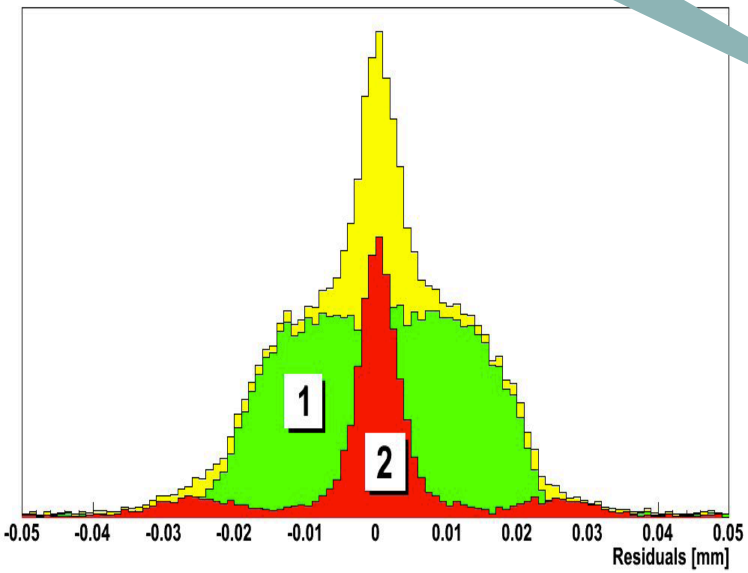
DEPFET/DCD-B Test System

Switcher-B
for Clear and Gate Control

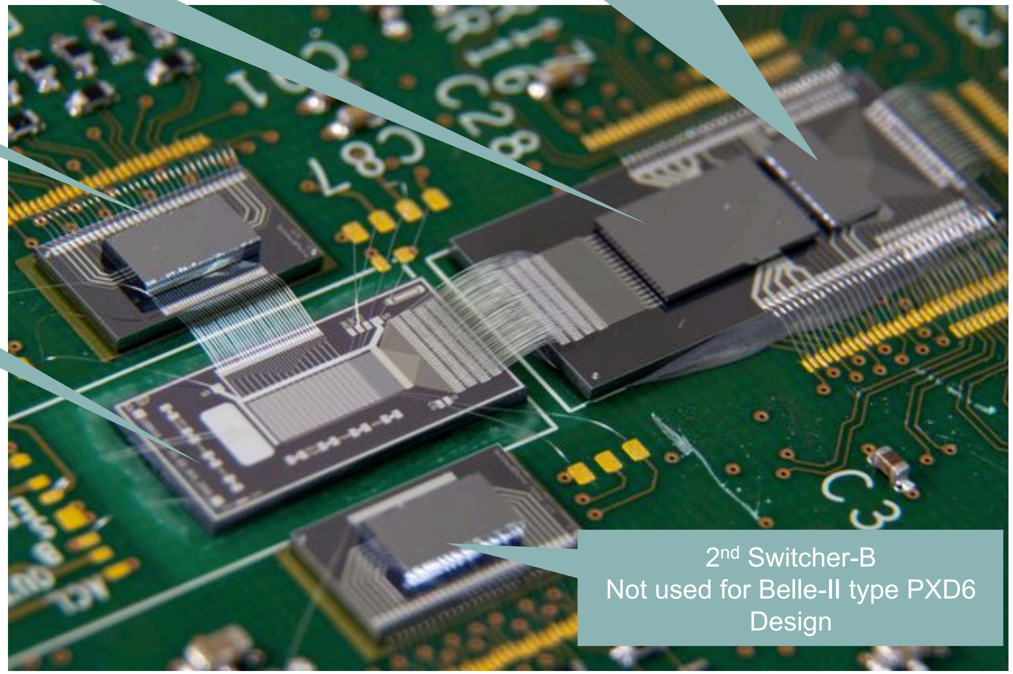
DCD-B
Read-out Chip

DCD-RO
Line Driver and Buffer to FPGA

PXD6 Belle-II DEPFET
Matrix 32x64 Pixels
L = 6 µm
Pixel Size 50 x 50 µm²
Thickness 50 µm



Residuals distribution for perpendicular tracks with single pixel response (1) and more than 1 pixel response (2), σ=12 µm

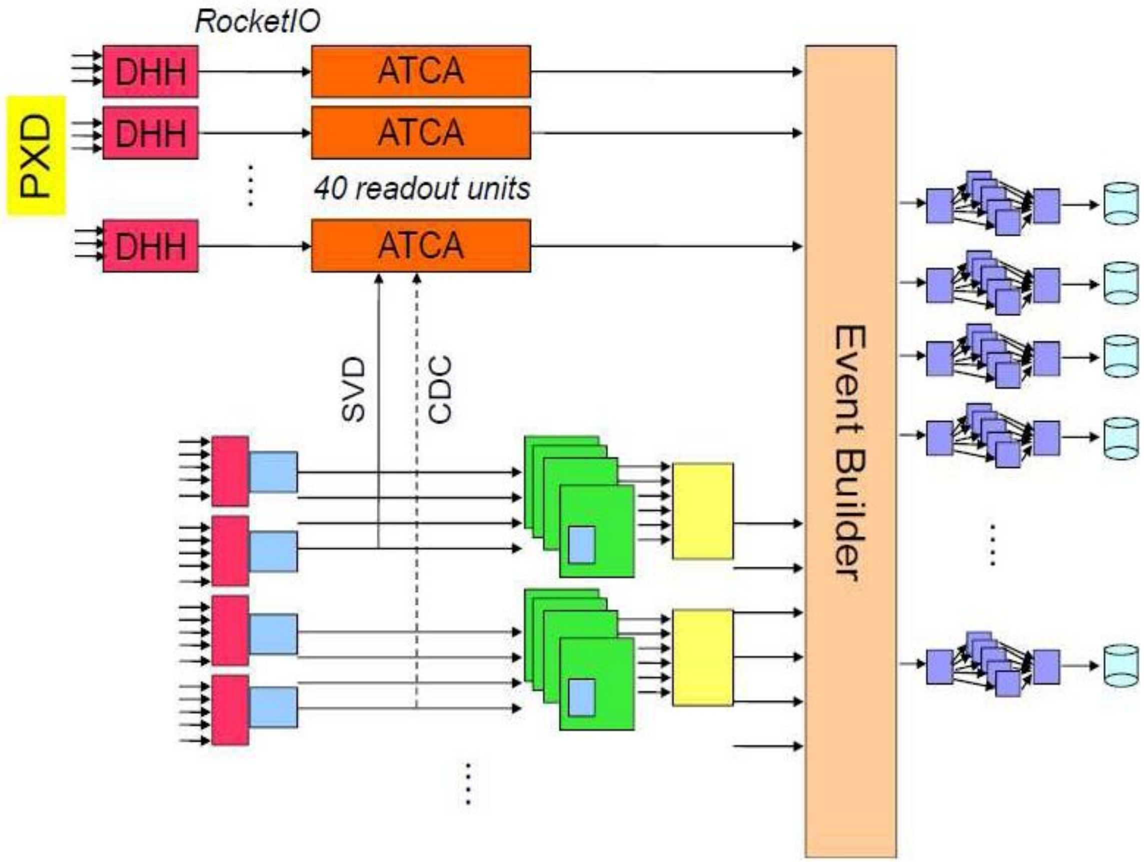


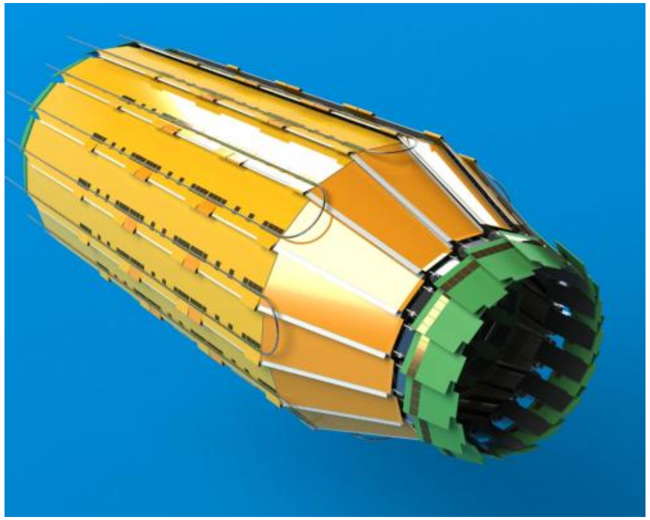
2^{nd} Switcher-B
Not used for Belle-II type PXD6 Design

- ▷ 320 MHz DCD-B clock
- ▷ → **100 ns** signal processing time per row

DAQ system of Belle II PXD

- From DHP to **DHH (Data Handling Hybrid)** via 15m line: kapton converted to twisted-pair in a passive patch panel
- DHHs via optical links to ATCA Compute Nodes
  - ATCA CNs **reduce data** based on triggers
  - ATCA CNs compute fast tracking **using SVD data** to quickly **identify regions of interest** in the PXD

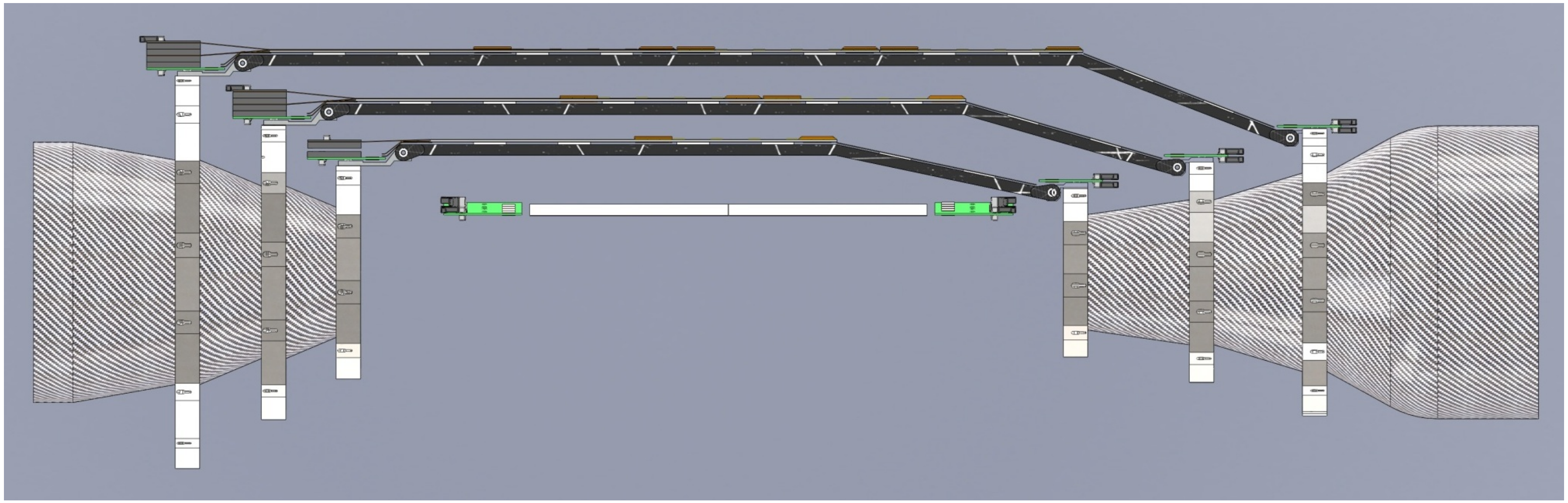




Belle and Belle II
DEPFET Pixel Detector
Double-sided Strip Detector
Summary

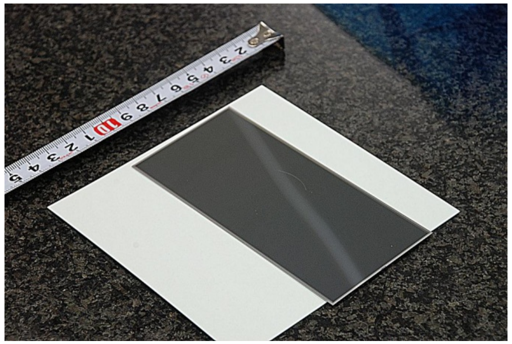
SVD Configuration

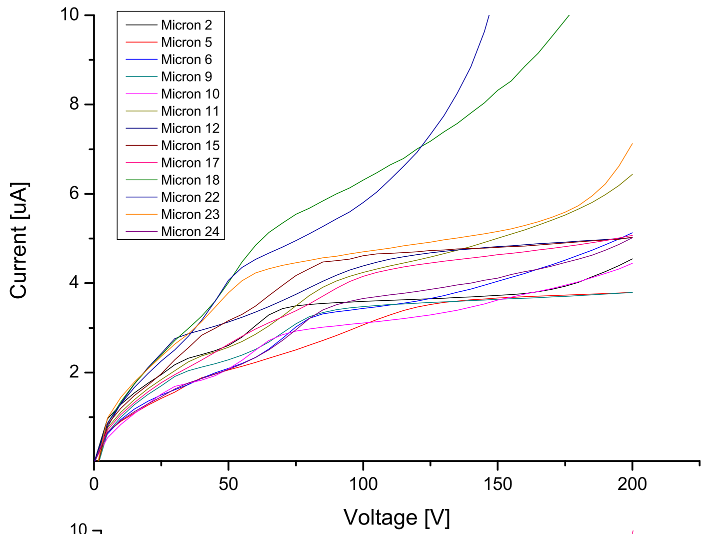
- Outermost layers 4-6 with slanted forward part (trapezoidal sensors)
- Layer 3 with straight ladders: mechanics still under discussion
- Sensors need to be read out individually (no daisy-chaining)
  - High background -> fast shaping time to keep occupancy low -> high noise -> short strips
- However, very low material budget necessary

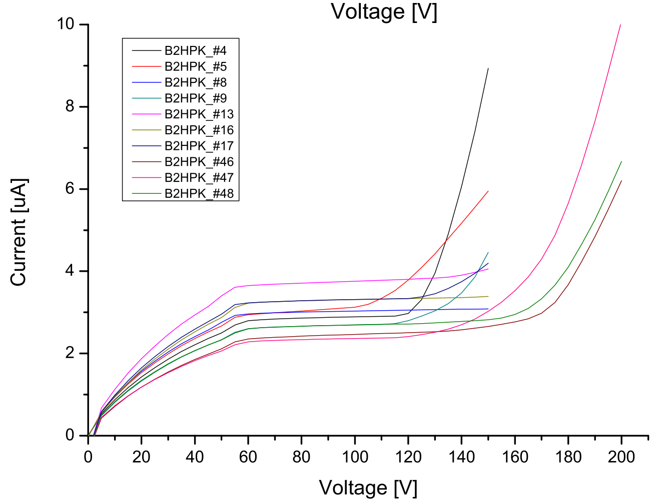


Double-sided strip sensors from 6” wafer

- Double sided strip silicon detectors with **AC-coupled** readout and **poly-silicon resistor** biasing made of **6 inch wafers**
  - **Size 12 x 6 cm**
- After market survey, prototypes ordered and delivered from
  - **Hamamatsu** (rectangular)
  - **Micron** (trapezoidal)



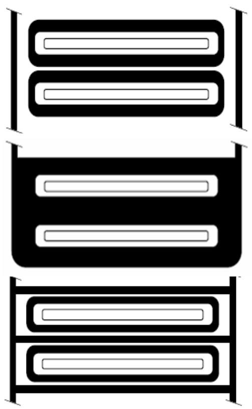


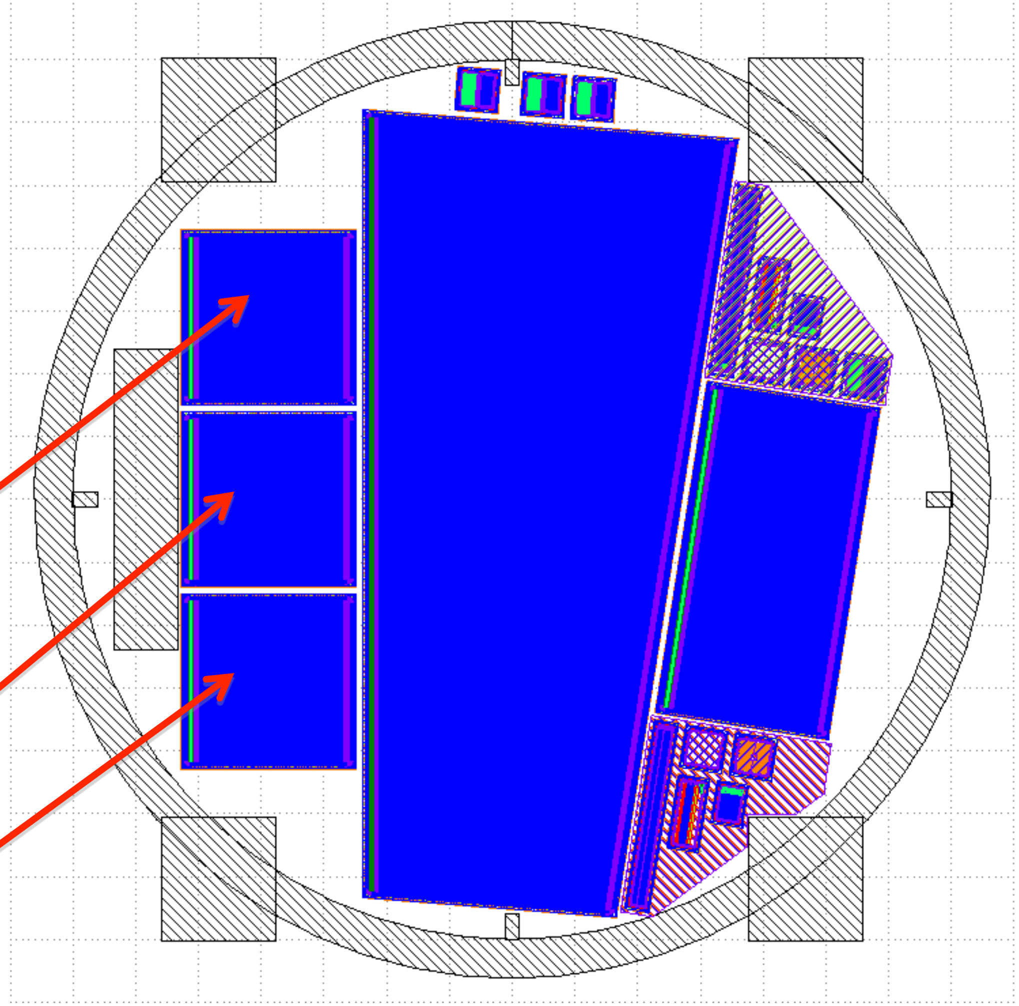


Trapezoidal Sensors for Forward Region

MICRON SEMICONDUCTOR ltd

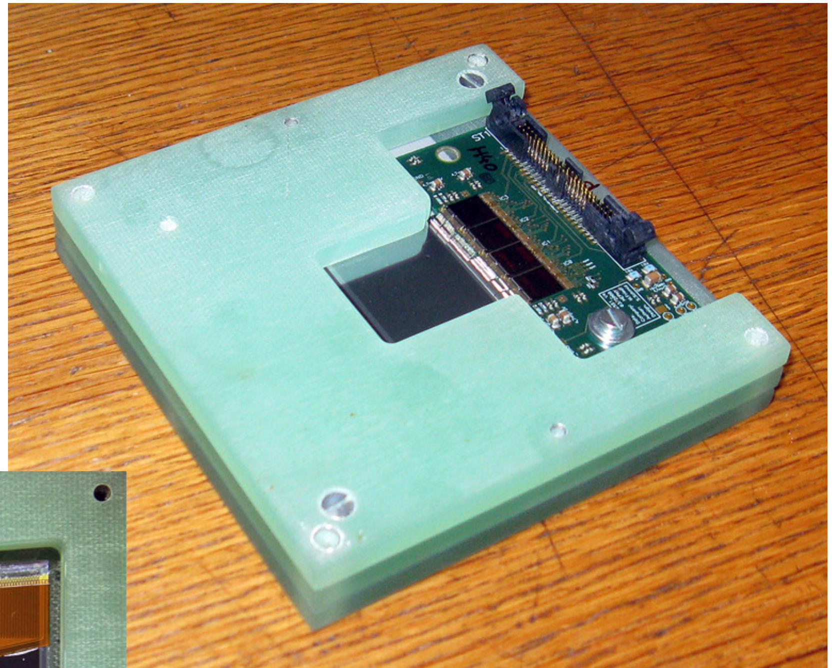
- Trapezoidal sensor for forward region
- Different p-stop layouts on test sensors





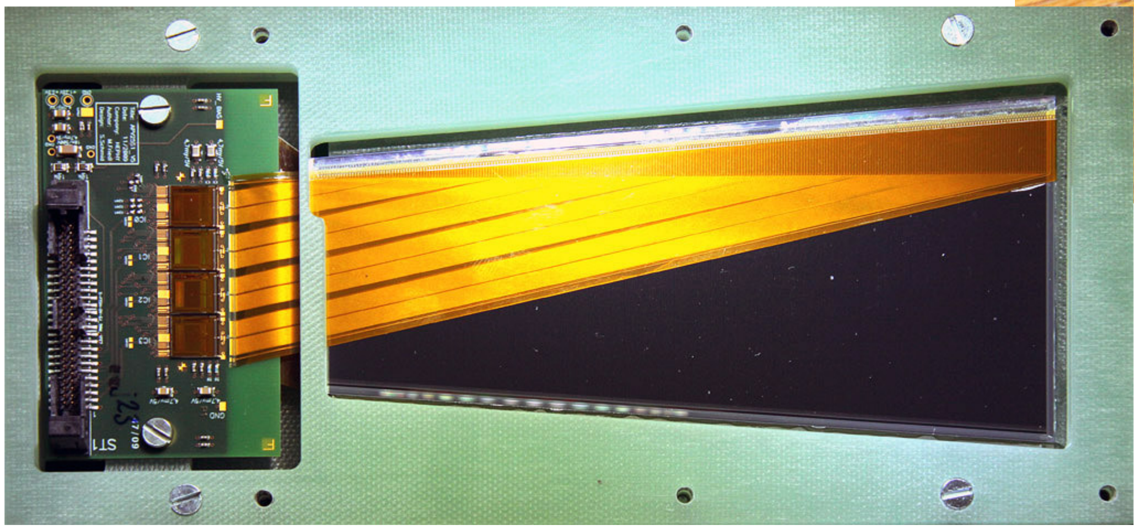
Modules for Beam Test

- Baby Modules used to verify p-stop layouts and geometries



Baby Module

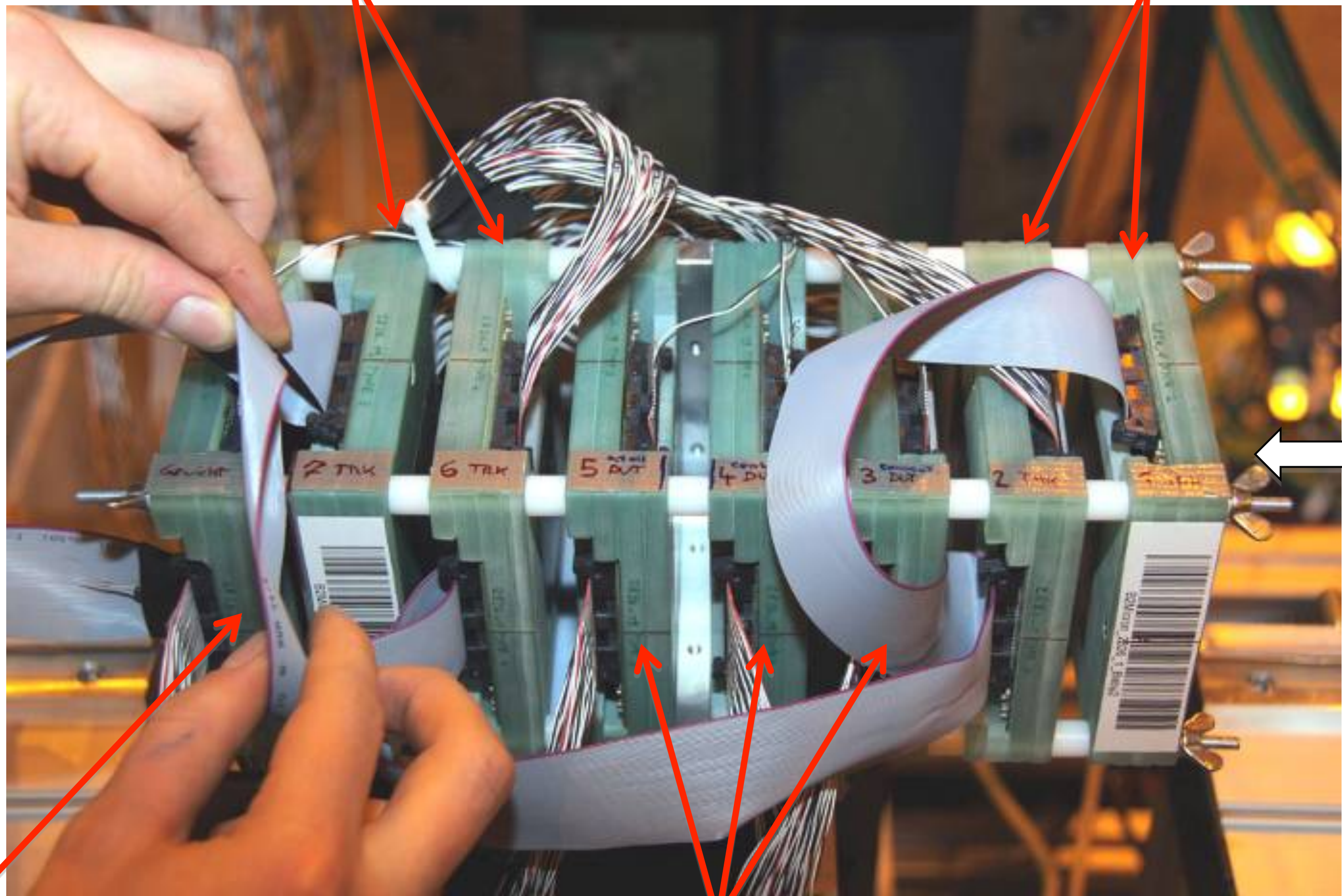
Trapezoidal Module



Stack Setup

Two sensors for tracking (p-side)

Two sensors for tracking (p-side)



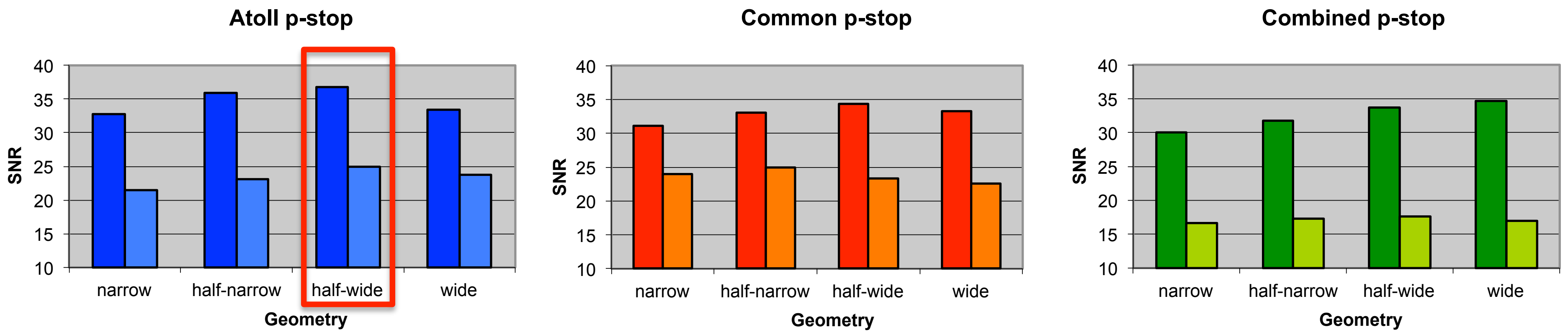
120 GeV hadrons (mostly π)

One module just for balance

Three DUTs, one of each p-stop pattern (n-side)

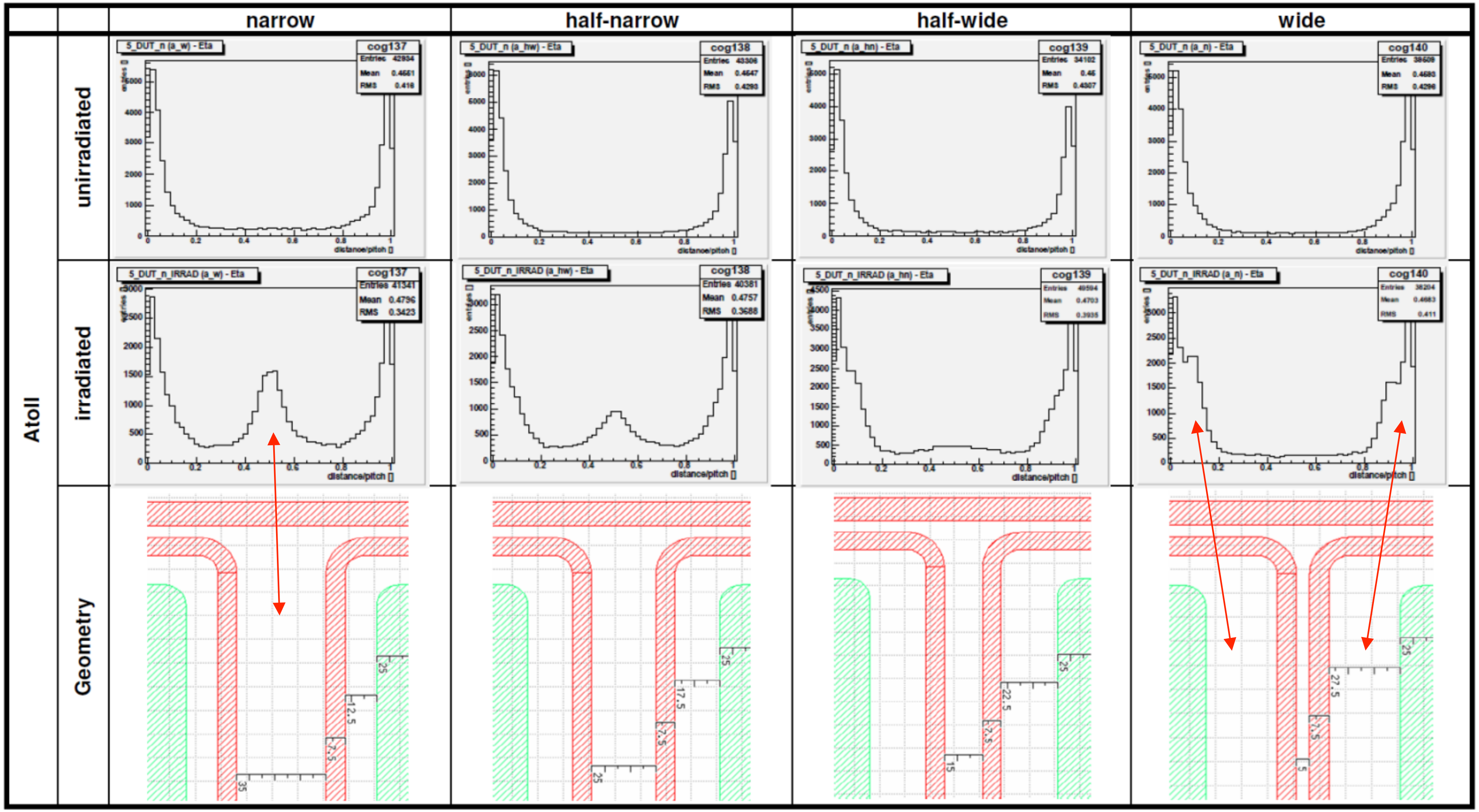
Signal-to-noise-ratios

- Test sensors have been Gamma-irradiated with Co-60 (70 Mrad)
- Tested before and after at CERN beam test (120 GeV hadrons)



- Dark colors: non-irradiated, Light colors: irradiated
- Four geometries: width of „virtual“ strip defined by p-stop
- Atoll pattern (half-wide) performs best, both irradiated and non-irradiated
  - Chosen for final sensor

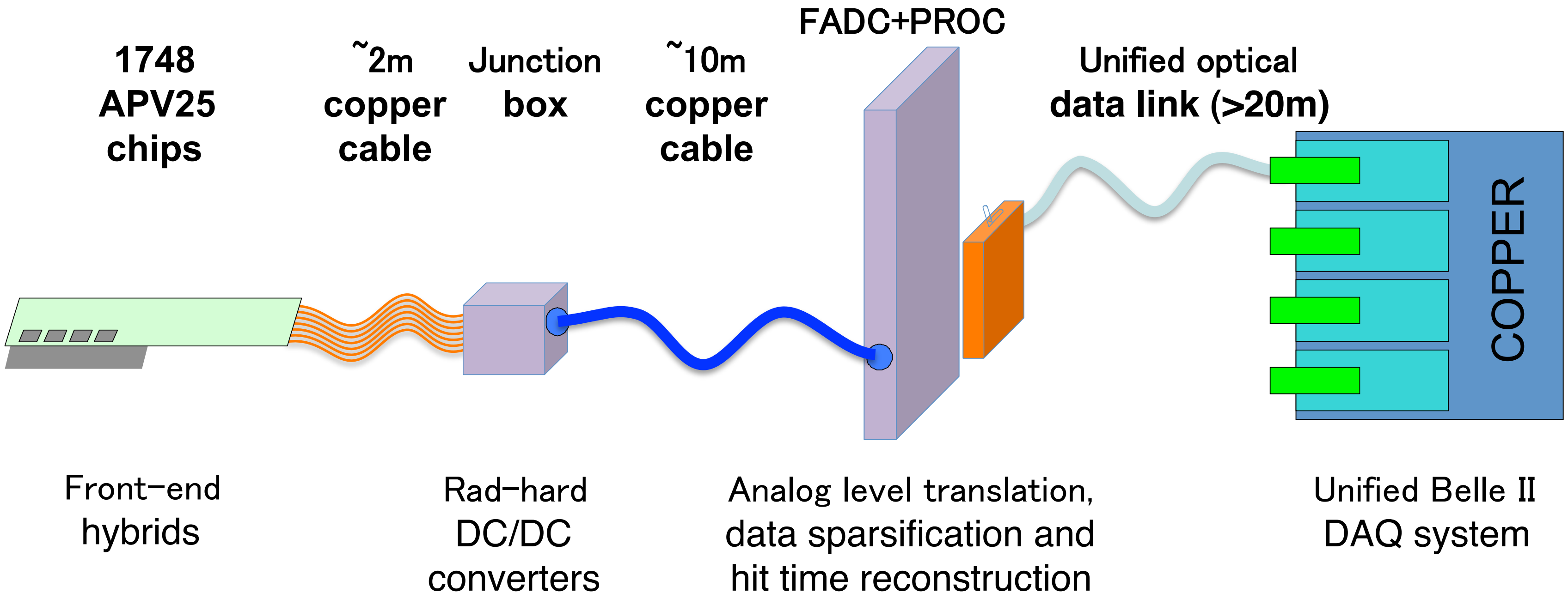
Eta Distributions for Atoll p-Stop



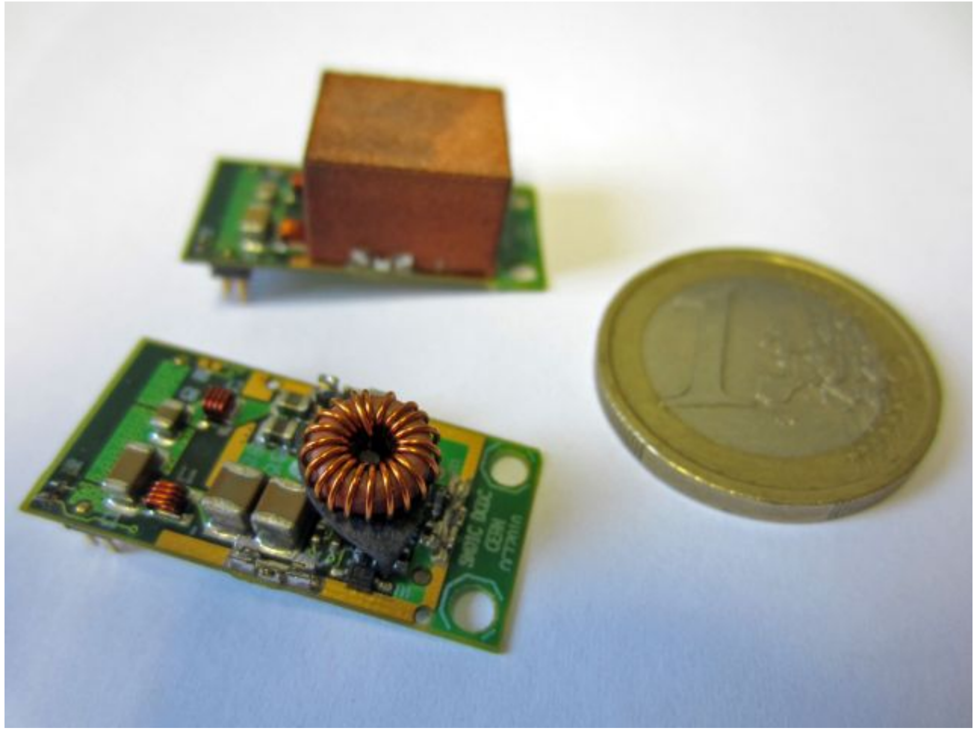
Charge accumulation in unimplanted region

Readout System Concept

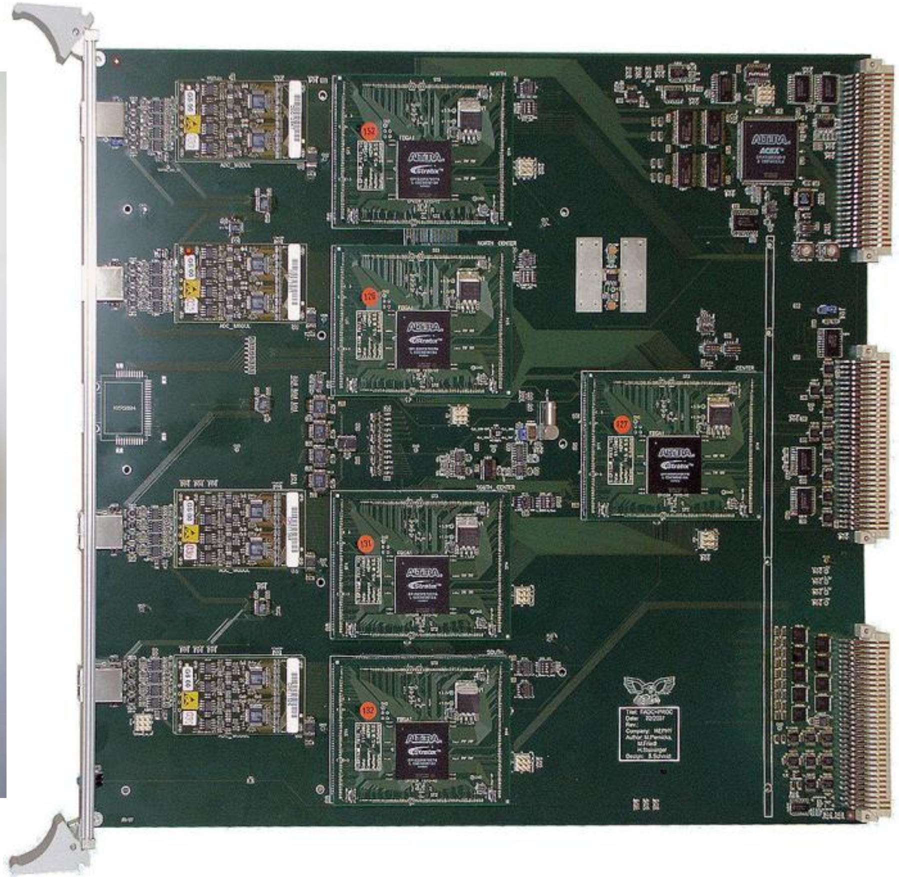
- **Analog data transmission** up to FADC by copper cable
  - Signal conditioning using FIR (Finite Impulse Response) filter
- Prototype **readout system exists**
  - **Verified** in several **beam tests**
  - **Needs to be adapted for higher integration (chips/boards)**



Prototypes



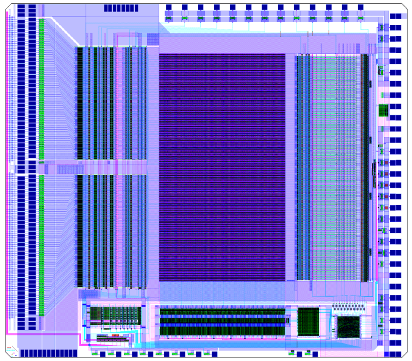
4A DC/DC converter prototype
(developed at CERN)

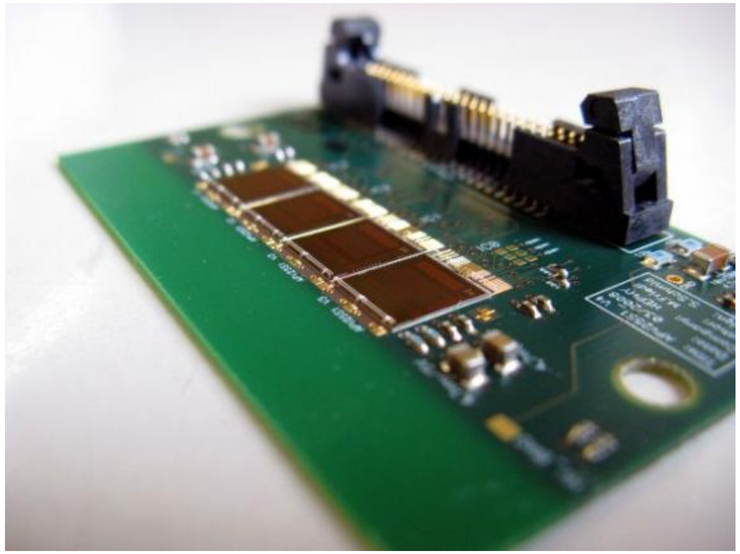


FADC+PROC (9U VME)
Digitization, zero-suppression,
hit time reconstruction

Readout Chip: APV25

- Developed for **CMS** (LHC) by *Imperial College* London and *Rutherford Appleton Lab*
  - 70.000 chips installed
- 0.25 µm CMOS process (**>100 MRad tolerant**)
- 128 channels
- **192 cell analog pipeline** → no dead time
- **50 ns shaping time** → low occupancy
- **Multi-peak mode** (read out several samples along shaping curve)
- **Noise:** 250 e + 36 e/pF → must minimize capacitive load!!!
- **Thinning** to 100µm successful



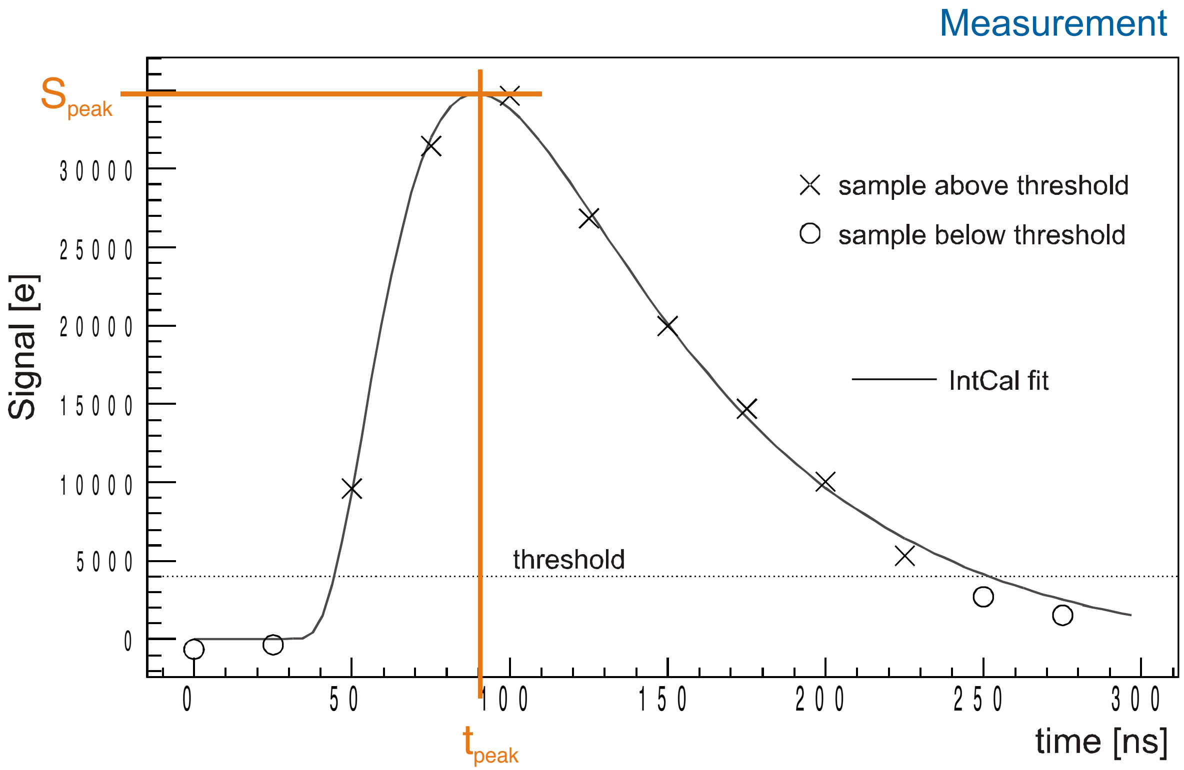


APV25 – Hit Time Reconstruction

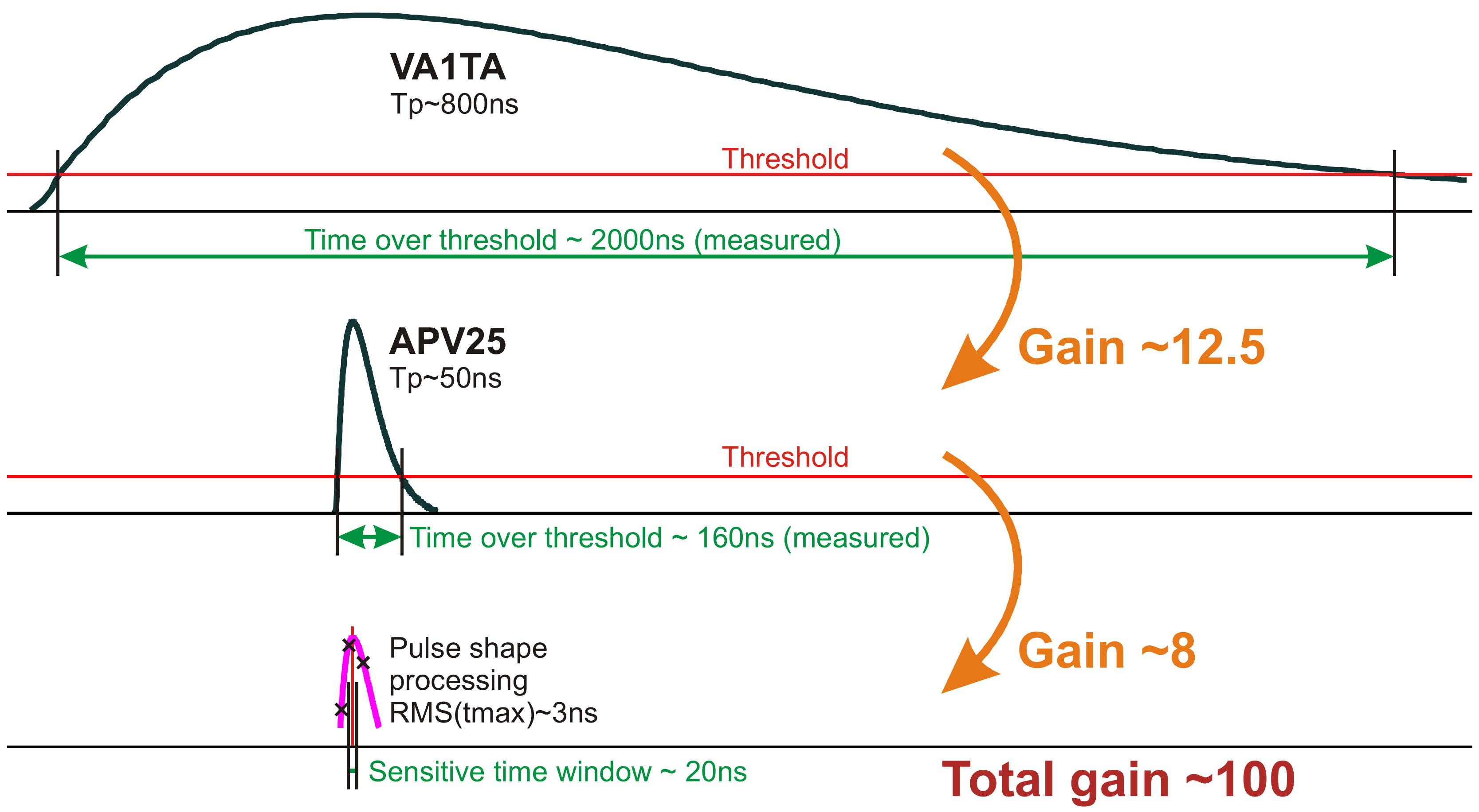
- Possibility of recording **multiple samples** (**x**) along shaped waveform (feature of APV25)

- Reconstruction of **peak time** (and amplitude) by waveform fit
  - Offline now
  - Hardware later

- Is used to **remove off-time background** hits

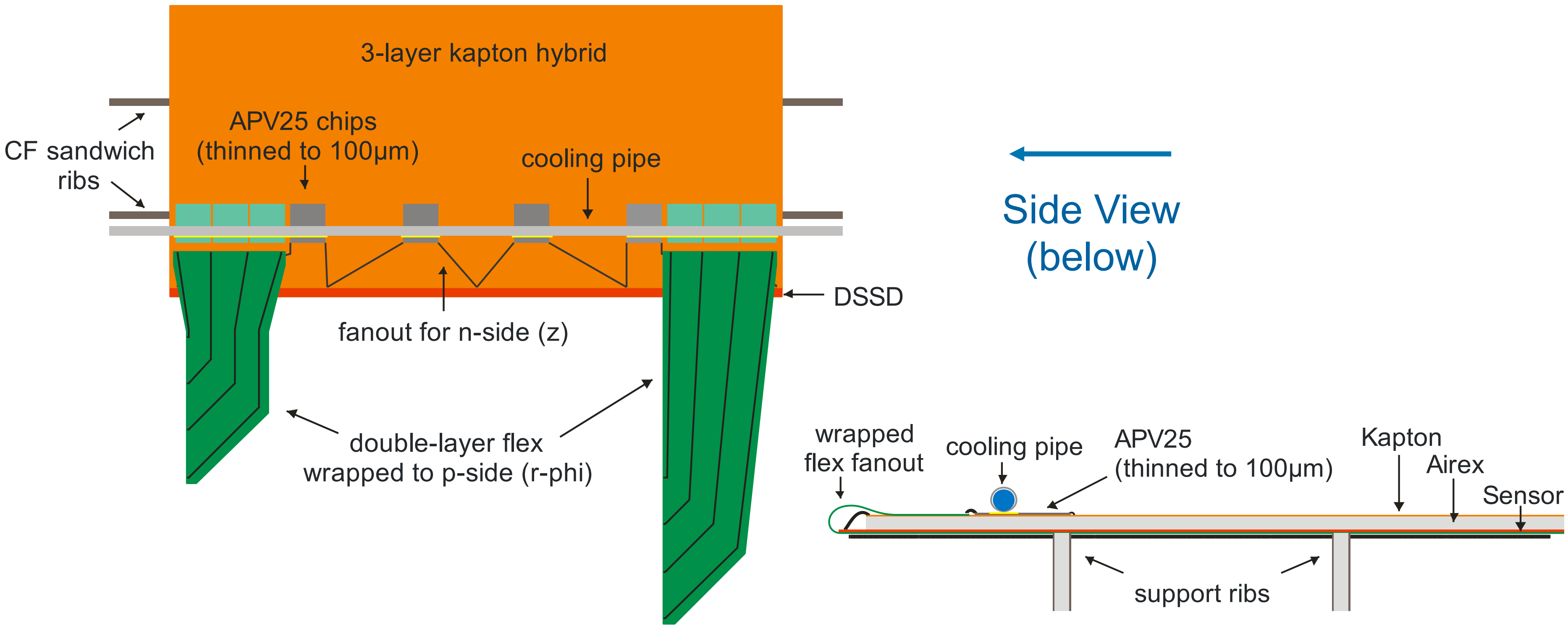


Occupancy Reduction Belle -> Belle II



Chip-on-Sensor Concept

- **Chip-on-sensor** concept for **double-sided readout**
- **Flex fan-out** pieces **wrapped** to opposite side (hence "Origami")
- All chips aligned on one side → **single cooling pipe**



Origami Module Assembly

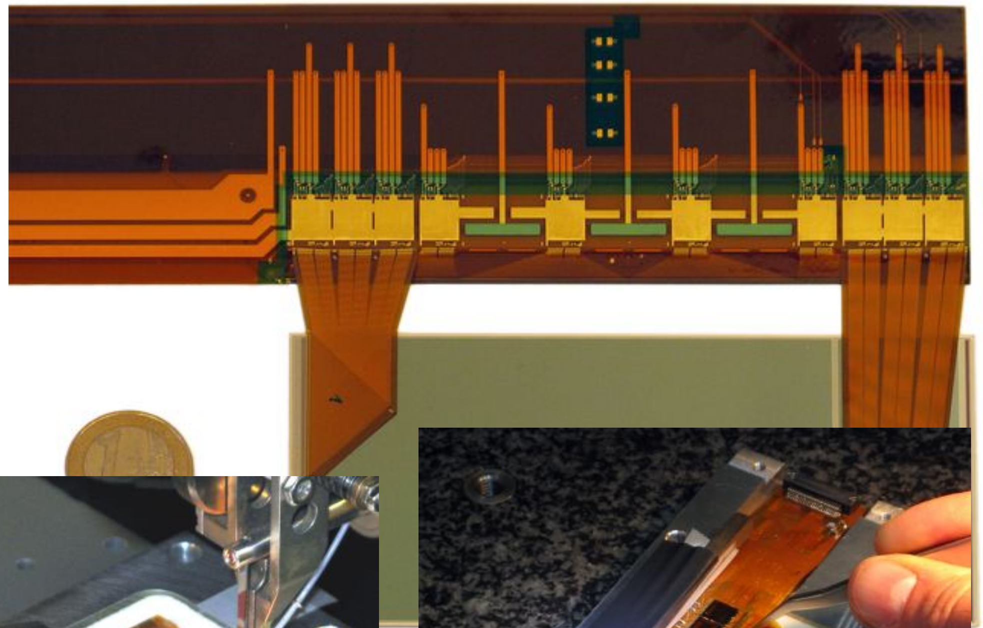
Ingredients:

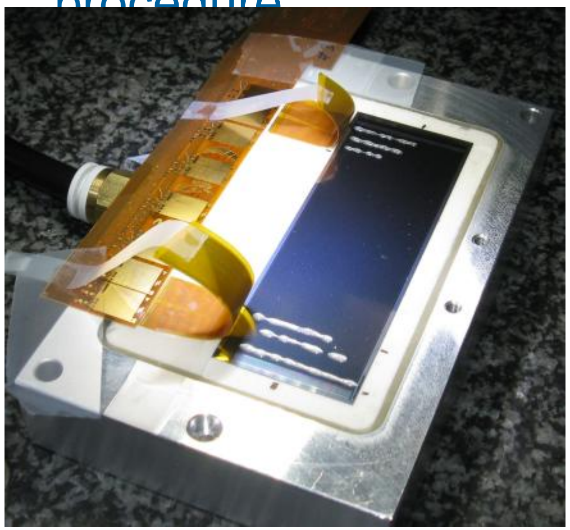
- DSSD sensors
- Kapton PCB and pitch-adapters
- APV Readout chips

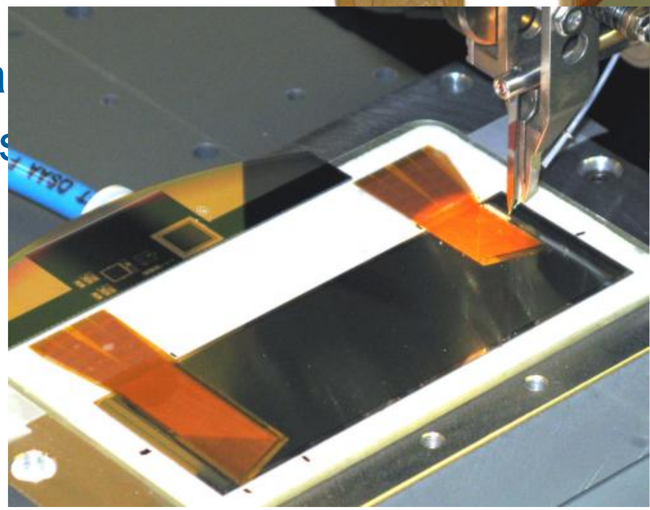
Followed by complicated assembly procedure

a

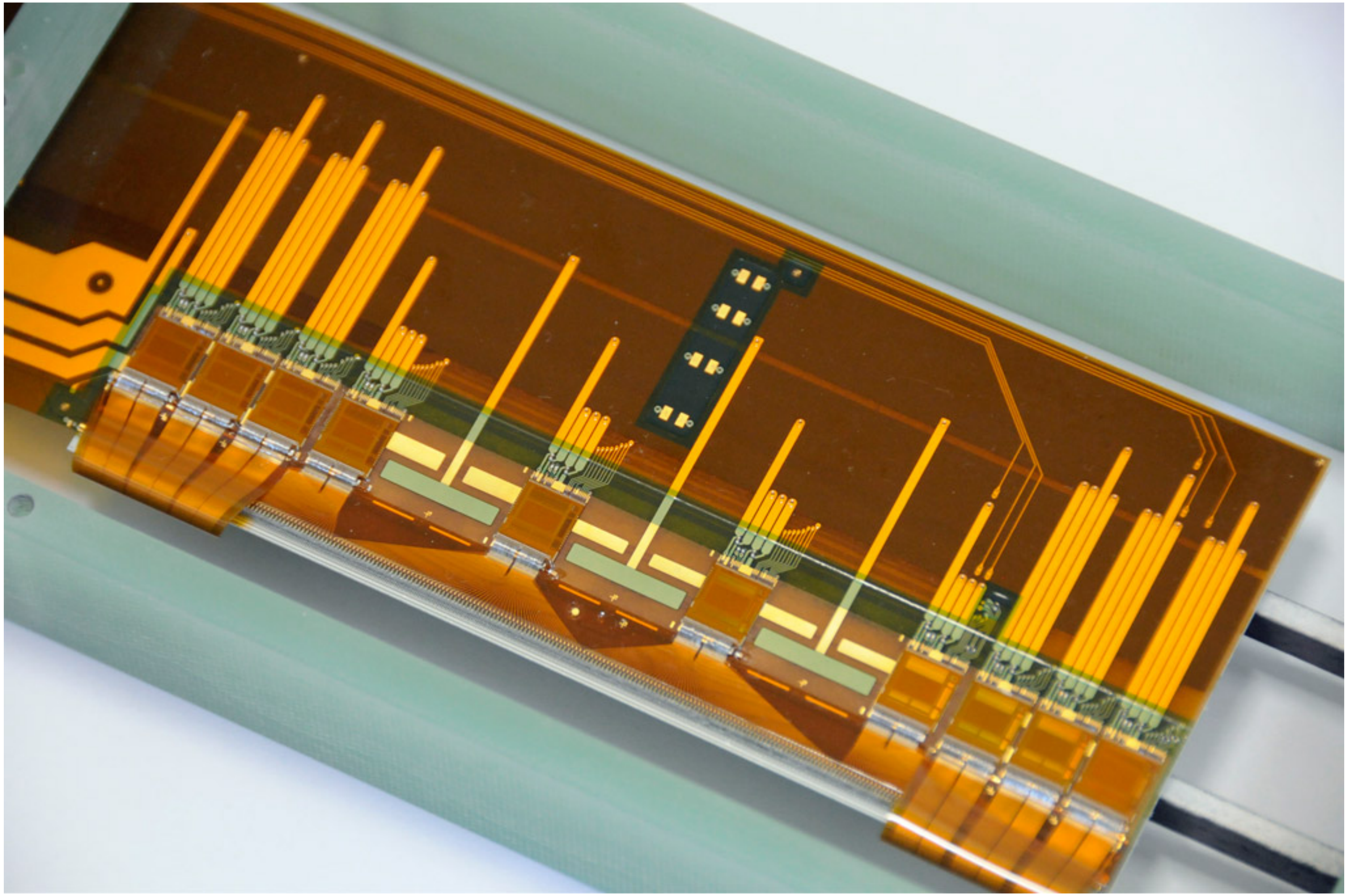
as





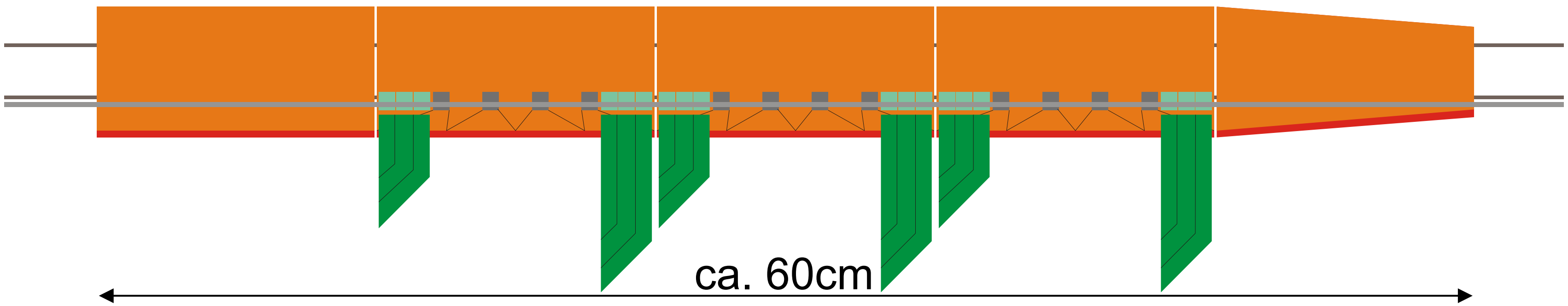


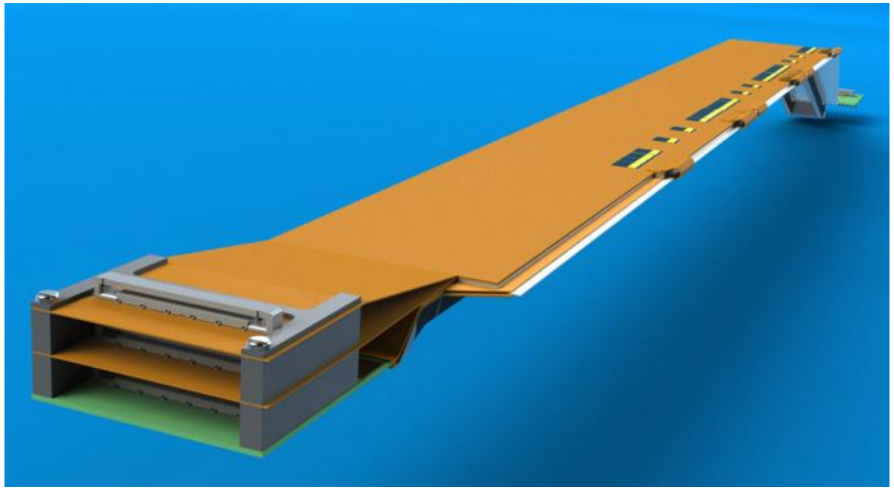
Origami Module with 6” HPK DSSD

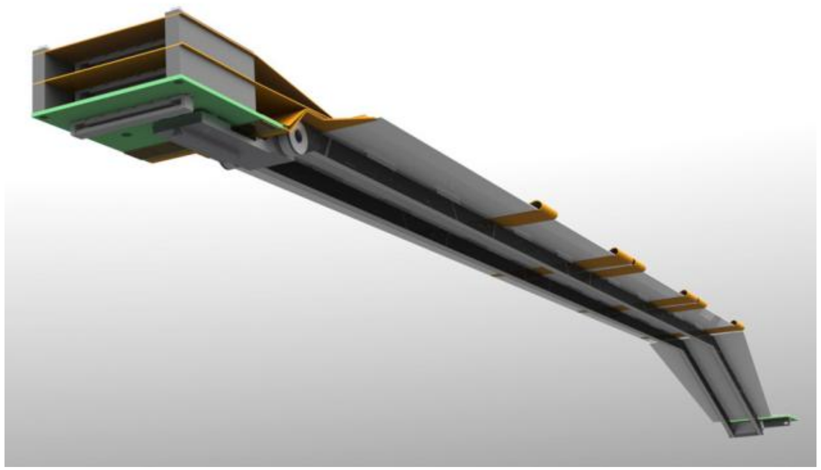


Sketch of the Outermost Ladder (Layer 6)

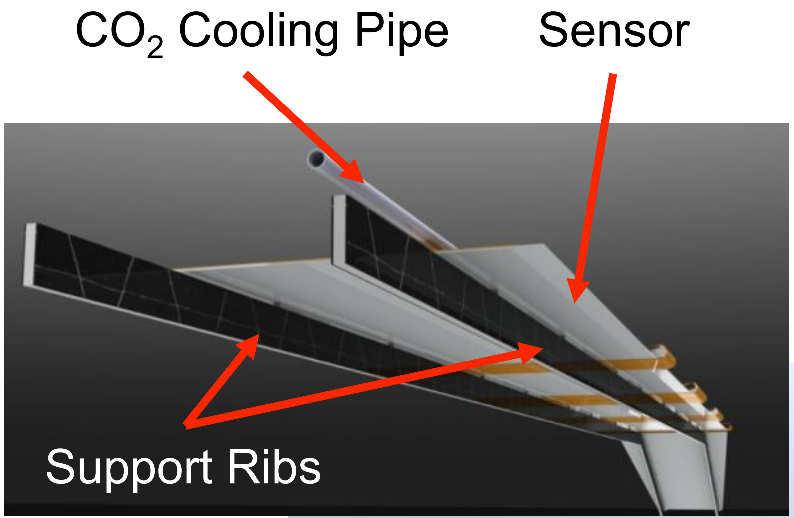
- Composed of 5 x 6” double-sided sensors
- Center sensors have Origami structure
- Averaged material budget over the full module: 0.55% X_0



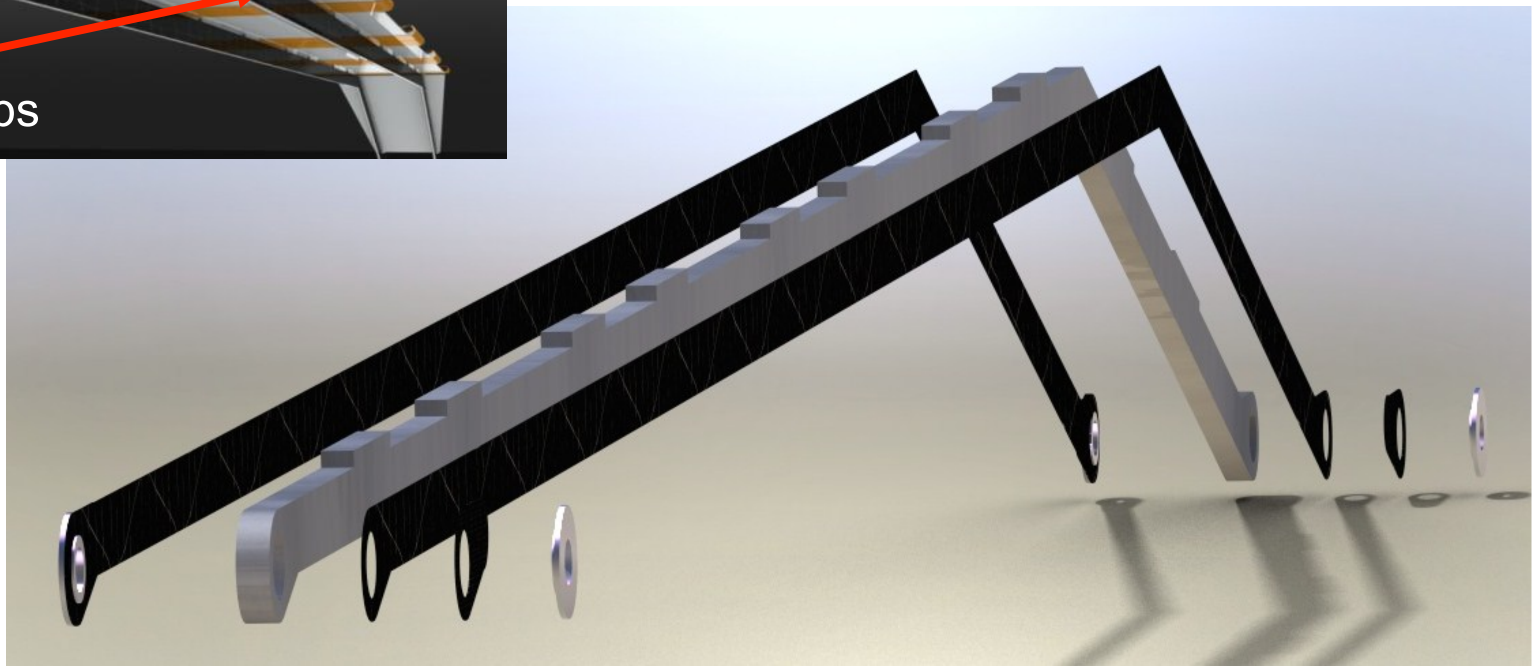




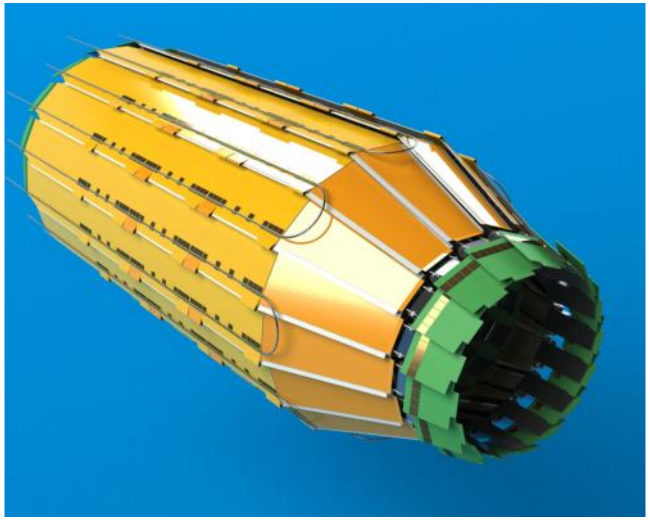
Ladder Mechanics



- Carried by ribs made of carbon fiber and *Airex* foam
- Very stiff, yet lightweight thanks to the sandwich construction



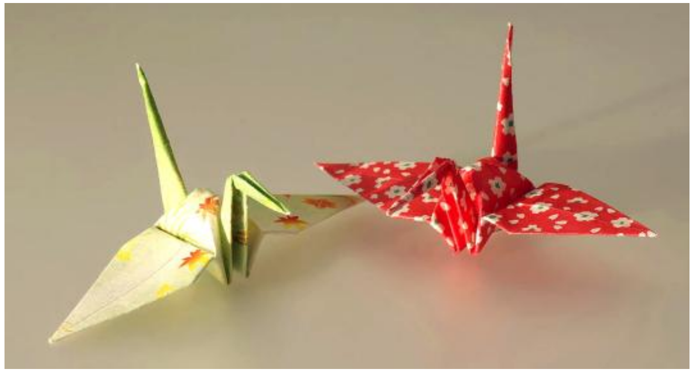
Belle II



Belle and Belle II
DEPFET Pixel Detector
Double-sided Strip Detector
Summary

Summary

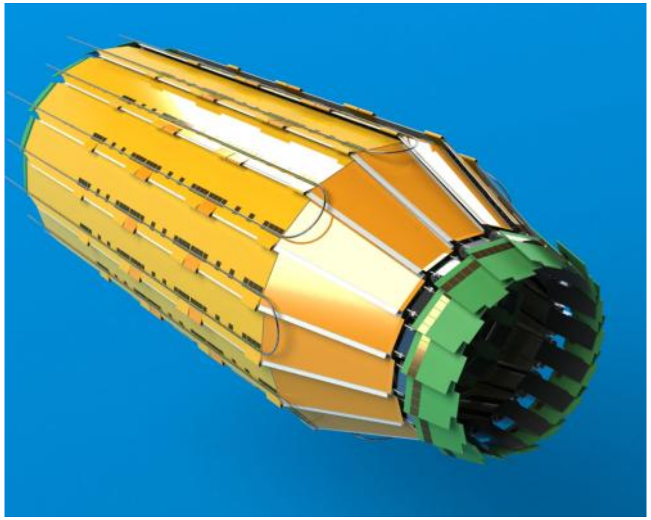
- **KEKB** is the **highest luminosity** machine in the world
- **Upgrade** of KEKB and Belle (2010-2015)
  - 40-fold increase in **luminosity**
  - Needs upgrades of all sub-detectors
- New, enlarged **Silicon Vertex Detector**
  - Two layers of **DEPFET** pixels
  - Four **double-sided strip** layers



- Strip Detector **R&D**
  - **6 inch Double Sided Strip Detectors**
    - Optimal p-stop geometry identified by SNR measurements before and after irradiation
  - Readout with **hit time reconstruction** for improved background tolerance
  - **Origami** chip-on-sensor concept for low-mass DSSD readout

Advertisment

http://vci.hephy.at



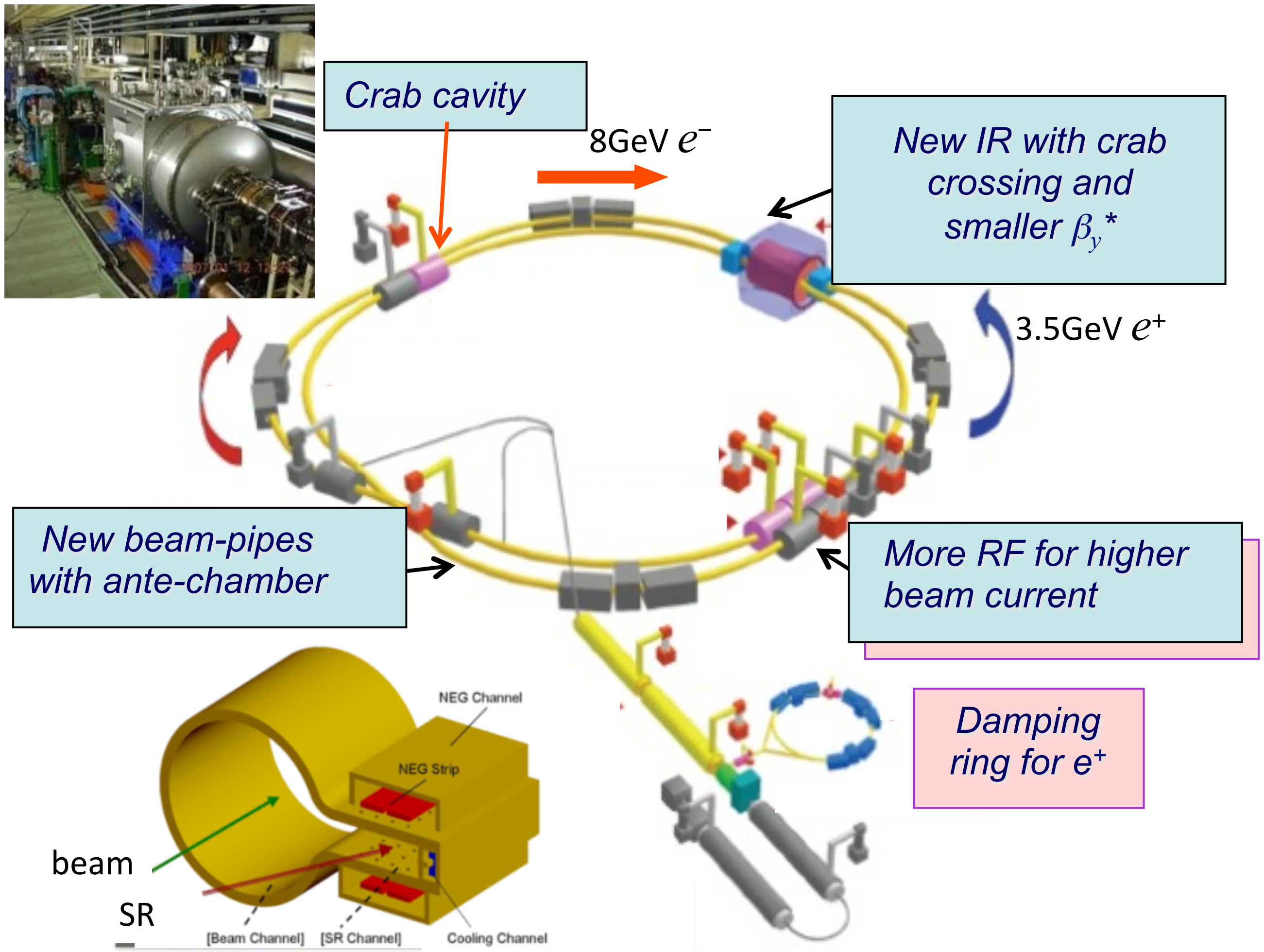
The End.

Backup Slides follow

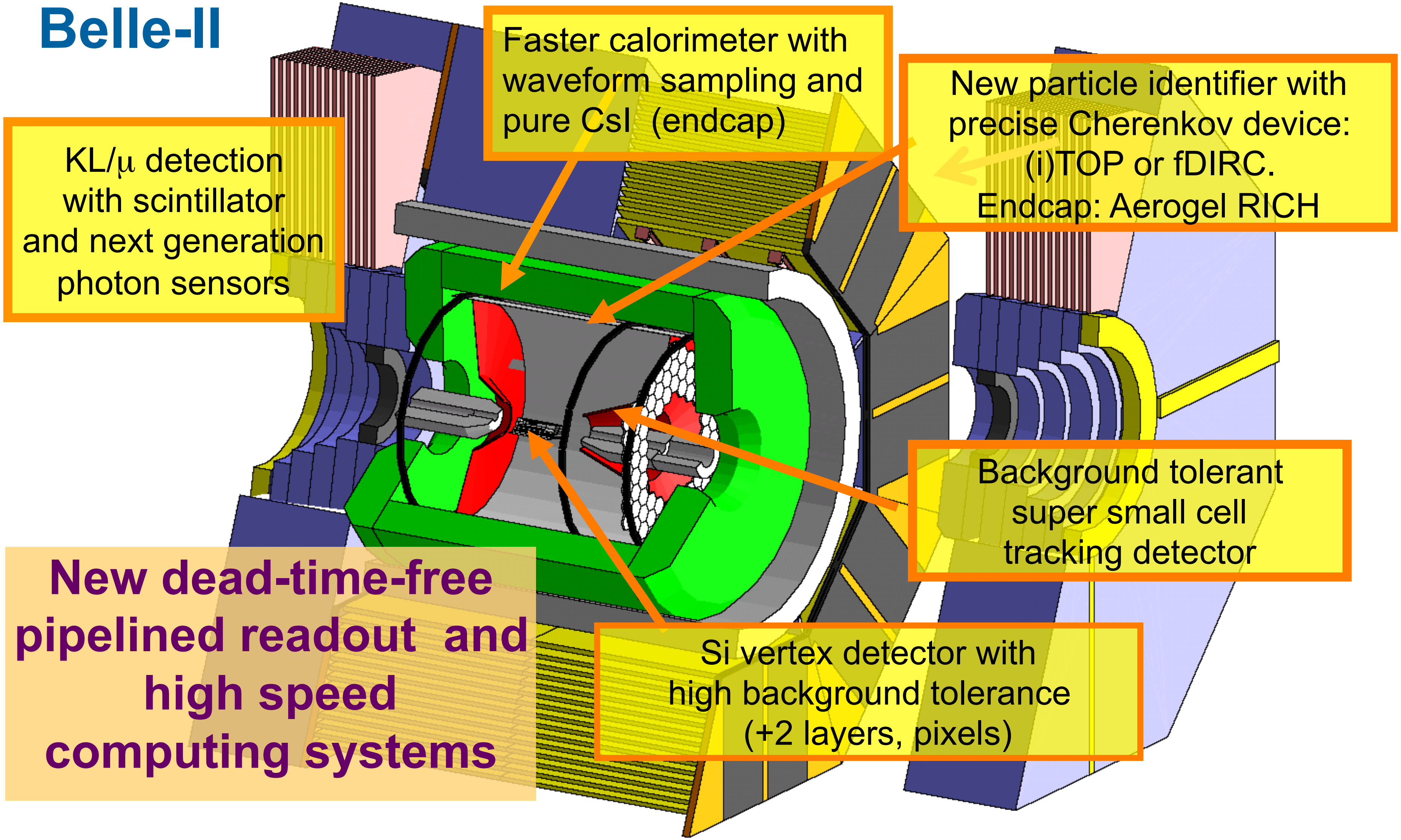
Beam Parameters

	KEKB Design	KEKB Achieved : with crab	SuperKEKB High-Current	SuperKEKB Nano-Beam
Energy (GeV) (LER/HER)	3.5/8.0	3.5/8.0	3.5/8.0	4.0/7.0
β_y^* (mm)	10/10	5.9/5.9	3/6	0.27/0.42
ε_x (nm)	18/18	18/24	24/18	3.2/2.4
σ_y(μm)	1.9	0.94	0.85/0.73	0.059
ξ_y	0.052	0.129/0.090	0.3/0.51	0.09/0.09
σ_z (mm)	4	~ 6	5/3	6/5
I_{beam} (A)	2.6/1.1	1.64/1.19	9.4/4.1	3.6/2.6
$N_{bunches}$	5000	1584	5000	2503
Luminosity (10^{34} cm^{-2} s^{-1})	1	2.11	53	80

KEKB accelerator upgrade



Belle-II



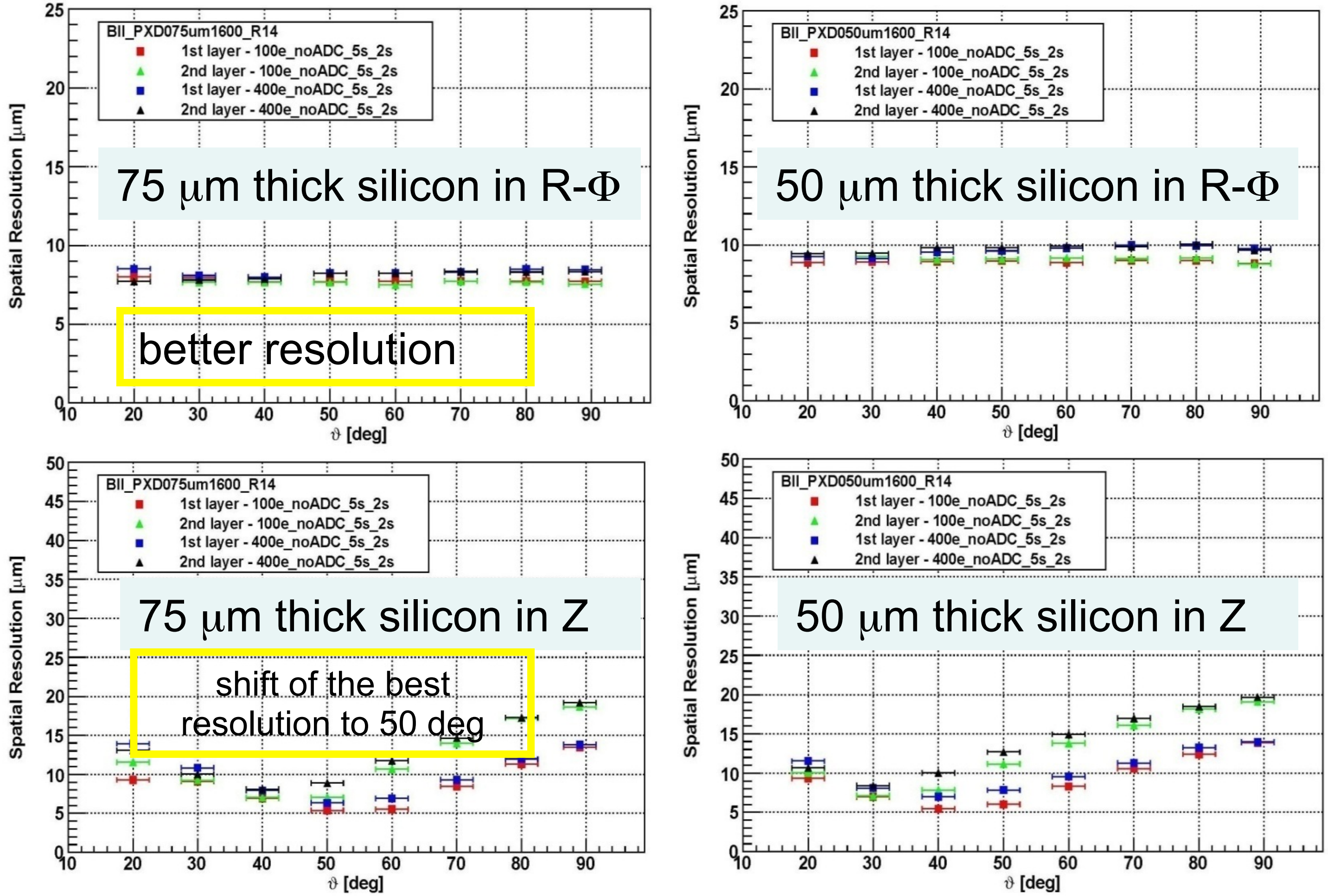
New dead-time-free pipelined readout and high speed computing systems

Spatial Resolution of the Belle II Detector

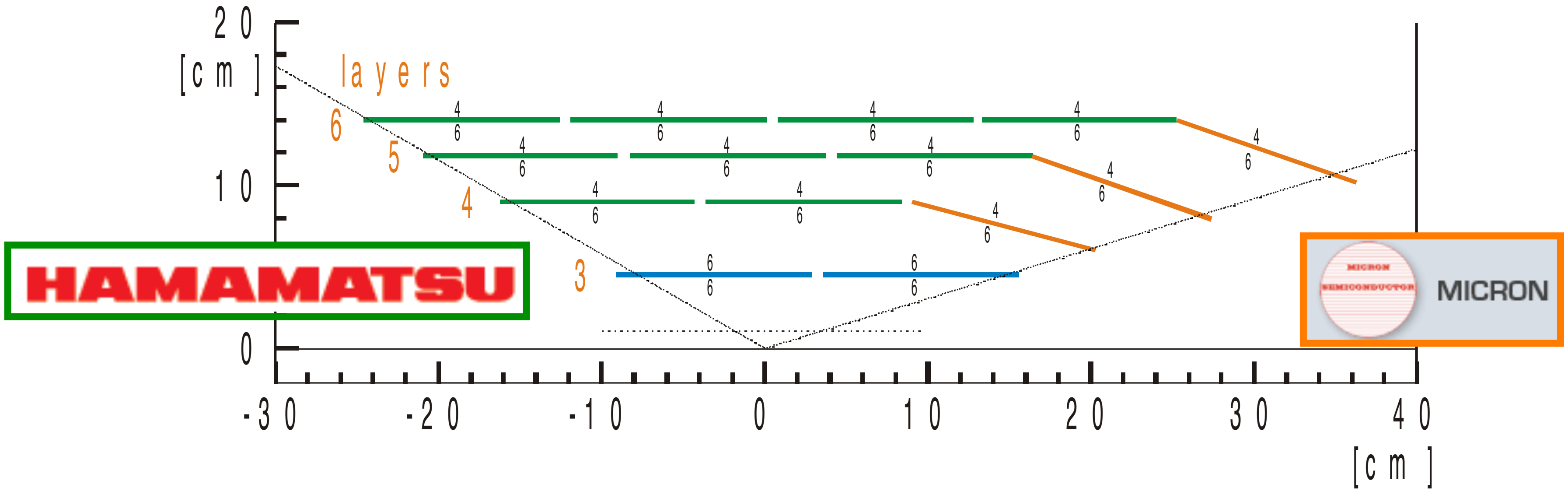
MC simulation for 50 and 75 μm thick silicon: intrinsic resolution in R-Φ and Z

Extensive simulation study (ILC software framework):

- To determine the expected Belle II PXD resolution
- Cluster sizes
- A/D conversion
- Signal processing
- Impact parameter
- Vertex resolutions



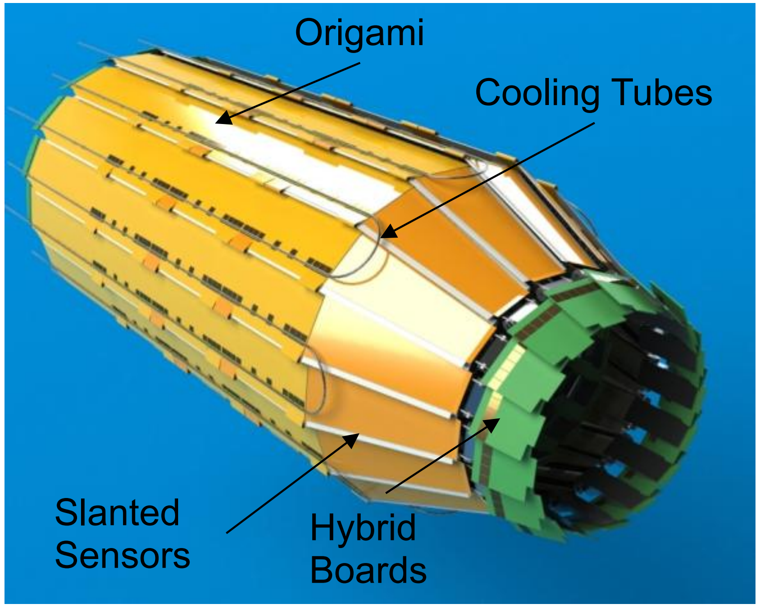
Sensor Types and Vendors

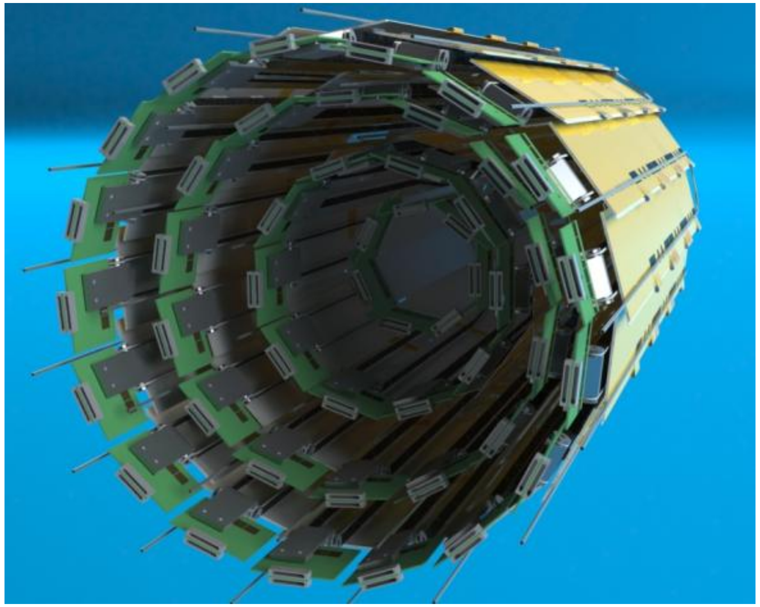


Layer	# of Ladders	Rect. Sensors [narrow]	Rect. Sensors [wide]	Wedge Sensors	APVs
6	16	0	64	16	800
5	12	0	36	12	480
4	10	0	20	10	300
3	7	14	0	0	168
Sum:	**49**	**14**	**120**	**38**	**1748**

Current Barrel Layout

Layer	Sensors/ Ladder	Origamis/ Ladder	Ladders	Length [mm]	Radius [mm]	Slant Angle [°]
3	2	0	7	262	38	0
4	3	1	10	390	80	11.9
5	4	2	12	515	105	16
6	5	3	16	645	135	21.1





Comparison VA1TA – APV25

VA1TA (SVD)

- Commercial product (IDEAS)
- Tp = 800ns (300 ns – 1000 ns)
- no pipeline
- <10 MHz readout
- 20 Mrad radiation tolerance
- noise: ENC = 180 e + 7.5 e/pF
- time over threshold: ~2000 ns
- single sample per trigger

APV25 (Belle-II SVD)

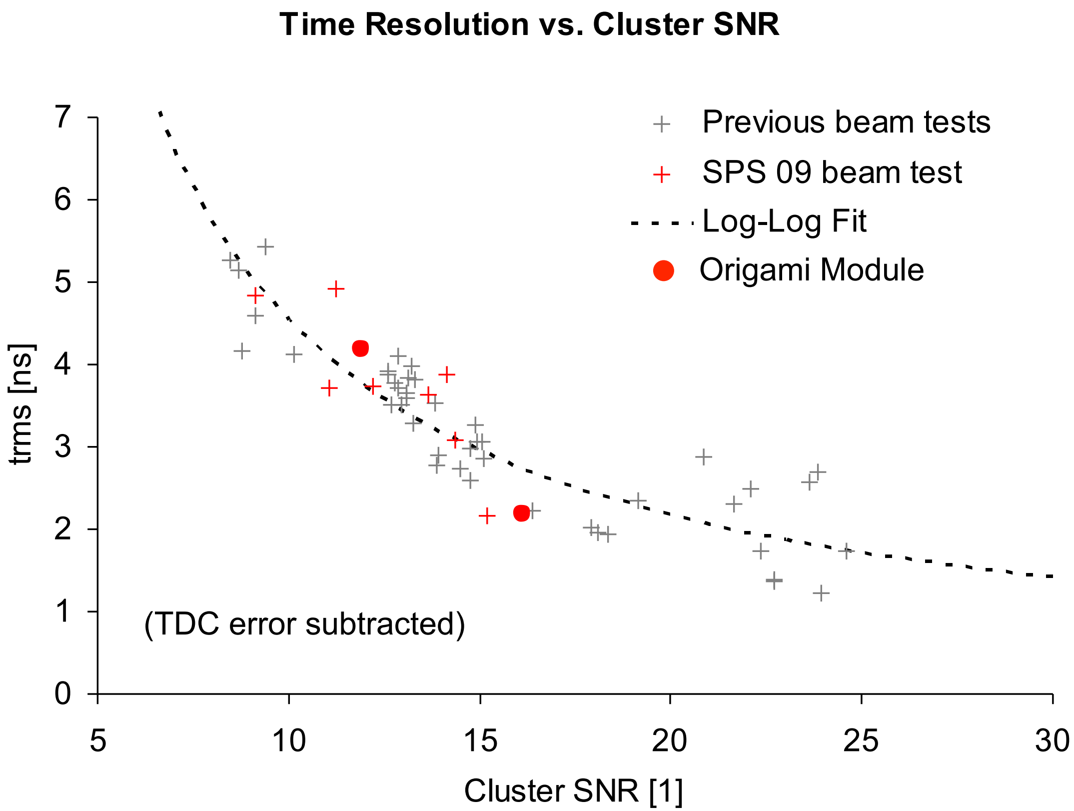
- Developed for CMS by IC London and RAL
- Tp = 50 ns (30 ns – 200 ns)
- 192 cells analog pipeline
- 40 MHz readout
- >100 Mrad radiation tolerance
- noise: ENC = 250 e + 36 e/pF
- time over threshold: ~160 ns
- multiple samples per trigger possible (Multi-Peak-Mode)

Measured Hit Time Precision

- Results achieved in **beam tests** with several different types of Belle DSSD prototype modules (covering a broad range of SNR)

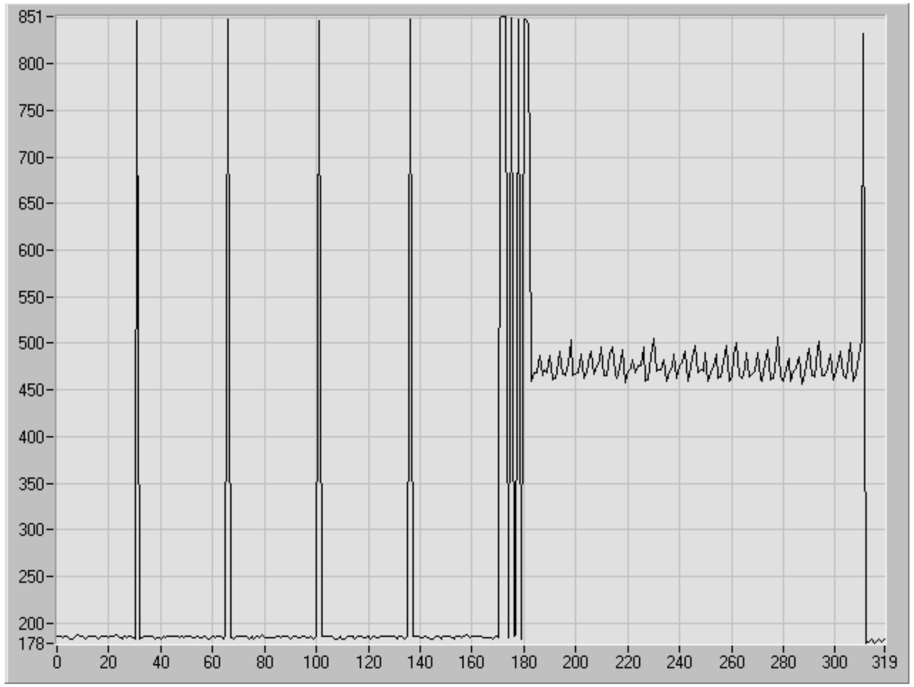
- **2...3 ns RMS** accuracy at typical cluster SNR (15...25)

- Working on implementation in **FPGA** (using lookup tables) – simulation successful

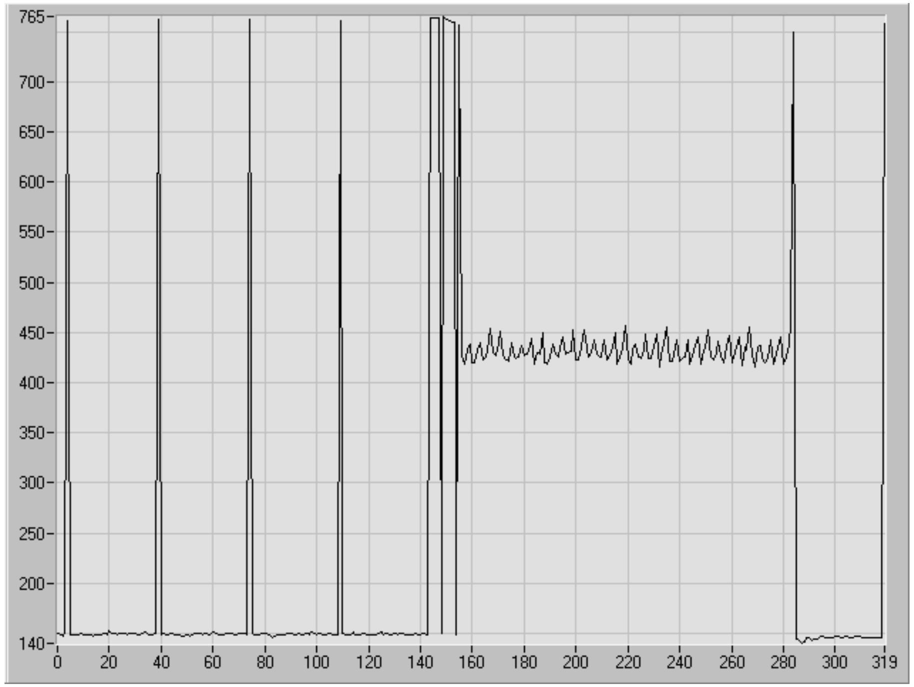


Finite Impulse Response (FIR) Filter

- Optimized channel



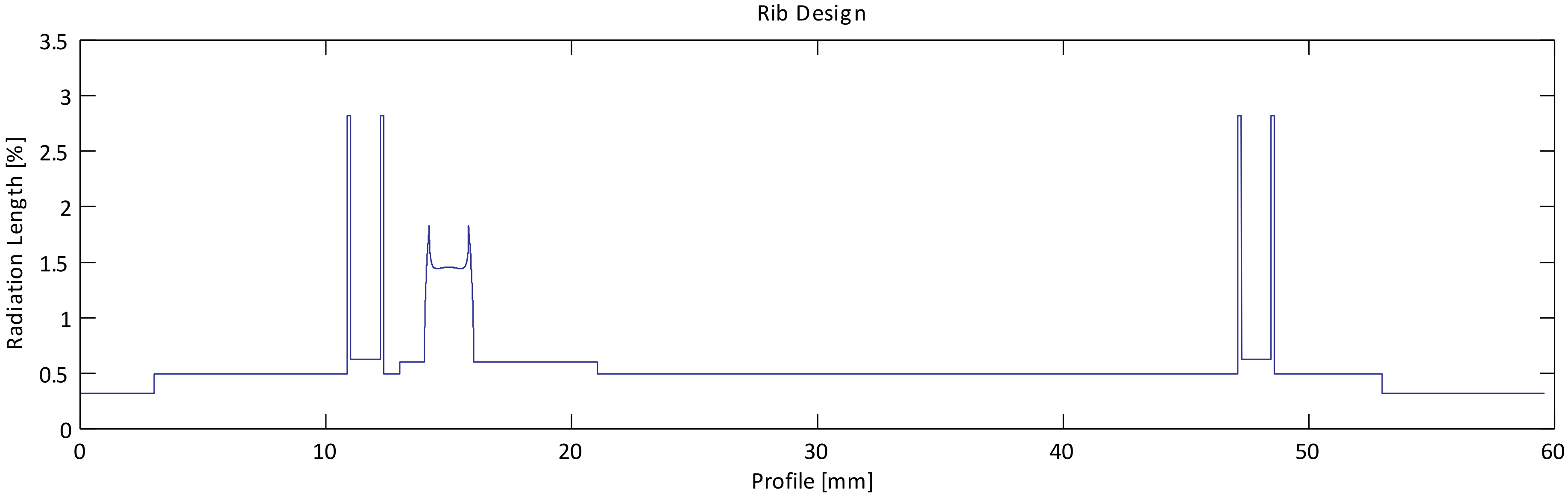
- Non-optimized channel

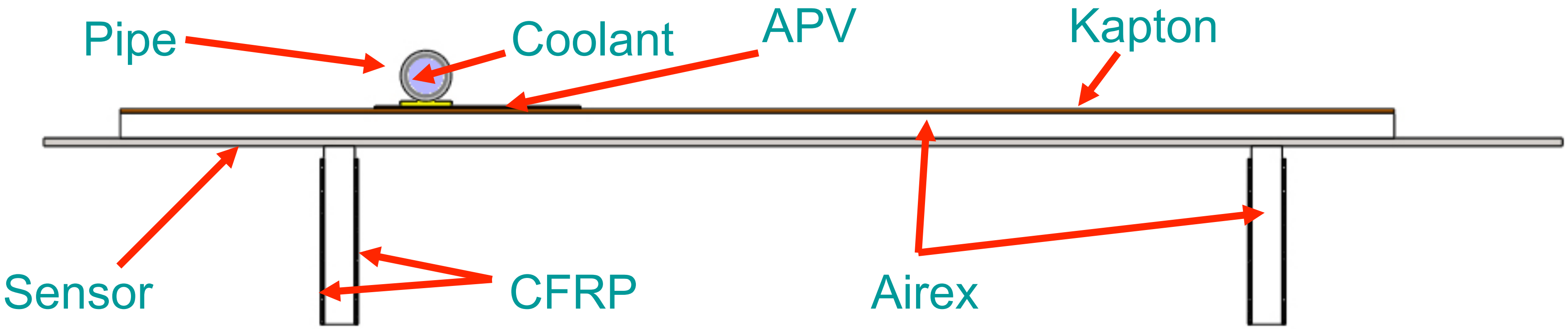


Raw APV25 output **with** FIR

- FIR filter with 8 coefficients
- Convolution (16-bit multiplications & sum) of incoming data at 40MHz

Maximum Radiation Length Distribution





Cooling Boundary Conditions

- Power dissipation per APV: 0.40 W
- 1 Origami sensor features 10 APVs

	Origamis /Ladder	Ladders	# APVs Origami	# APVs Hybrid	Power/ Layer [W]	Power Origami [W]
Layer 6	3	16	480	320	320	192
Layer 5	2	14	240	240	192	96
Layer 4	1	10	100	200	120	40
Layer 3	0	7	0	140	56	0
Sum		47	820	900	688	328

- Total Origami power dissipation: 328 W
- 360 W dissipated at the hybrid boards
- Total SVD power dissipation: 688 W

CO_2 Cooling

- Closed CO_2 cooling plant under development
- Collaboration with CERN
- First step is to gain experience with open (blow) system