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Prototype of a Gigabit Data Transmitter in 65~nm CMOS for DEPFET Pixel Detectors at Belle-II

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The Belle-II pixel detector (PXD) is the inner-most detector currently under development for the upgraded KEK-B factory in Japan. The PXD consists of two layers of DEPFET sensor modules located at radius 1.8 and 2.2~cm. Each module is equipped with three different ASIC types mounted on the detector substrate with flip-chip technique: (a) SWITCHER for generating steering signals for the DEPFET sensors, (b) DCD for digitizing the signal currents, and (c) DHP for performing data processing and sending the data off the module to the back-end data handling hybrid via 40~cm Kapton flex and 12–15~m twisted pair cables.

To meet the requirements of the PXD data transmission, a prototype of the DHP data transmitter has been developed in a 65nm CMOS technology. The transmitter consists of a current-mode logic (CML) driver and phase-locked loop (PLL) which generates a clock signal for a 1.6~Gbit/s output data stream from a 80~MHz reference clock. A programmable pre-emphasis circuit in the CML driver compensates signal losses in the long cable by shaping the transmitted pulse response.
The status of the chip developments for the DEPFET PXD will be shown and recent results of the performance of the Gbit link driver will be discussed.

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