Prototype of a Gigabit Data Transmitter in 65-nm CMOS for DEPFET Pixel Detectors at Belle-II

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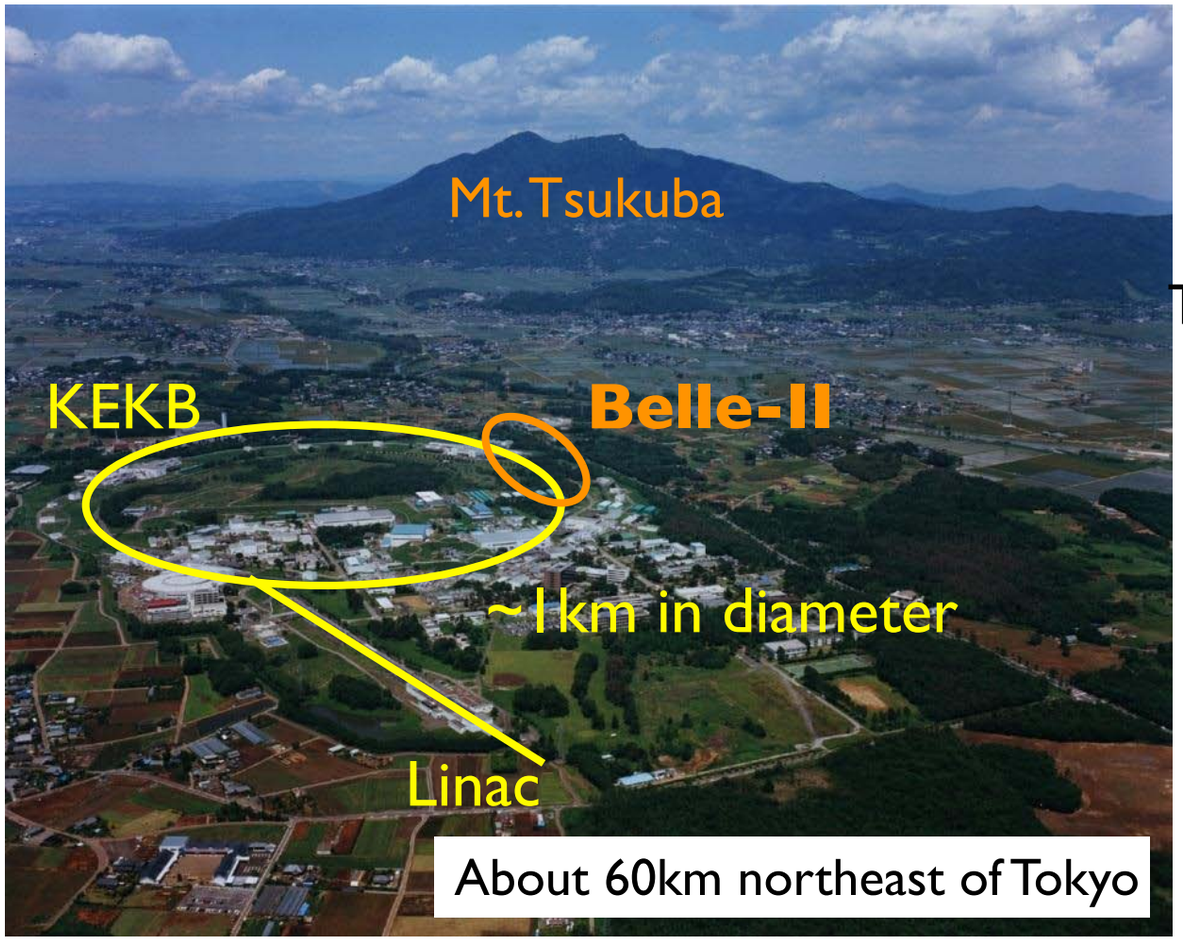
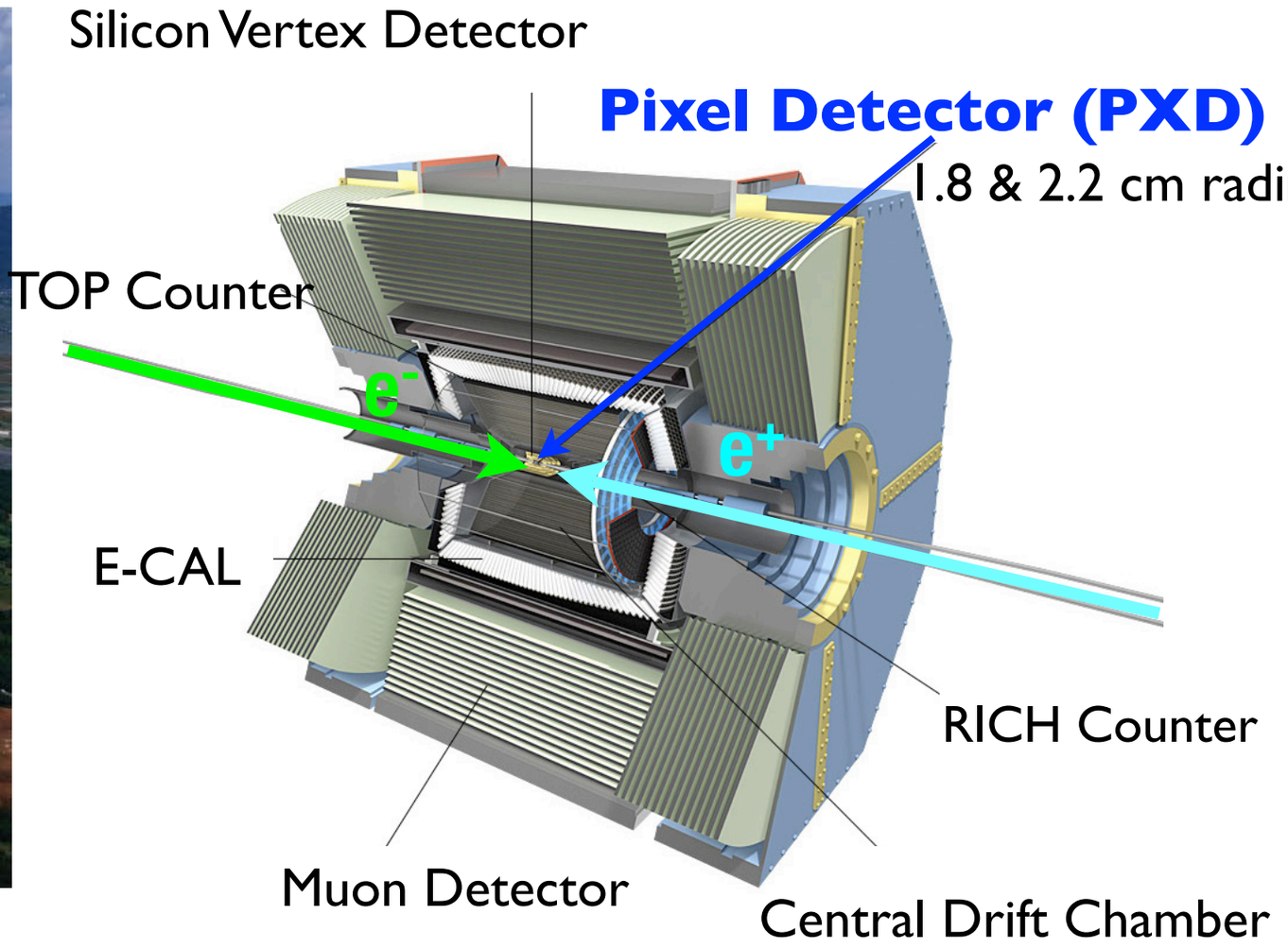
Outline

- ✦ Pixel Detector (PXD) at Belle-II
- ✦ Data Handling Processor (DHP)
- ✦ Gbit Data Transmitter
- ✦ Measurement Results
- ✦ Summary

Belle-II Experiment at Super-KEKB





KEKB/Belle upgrade (2010–2013)

- study CP violation via B^0/B^0-bar decays
- rare decay modes → more statistics

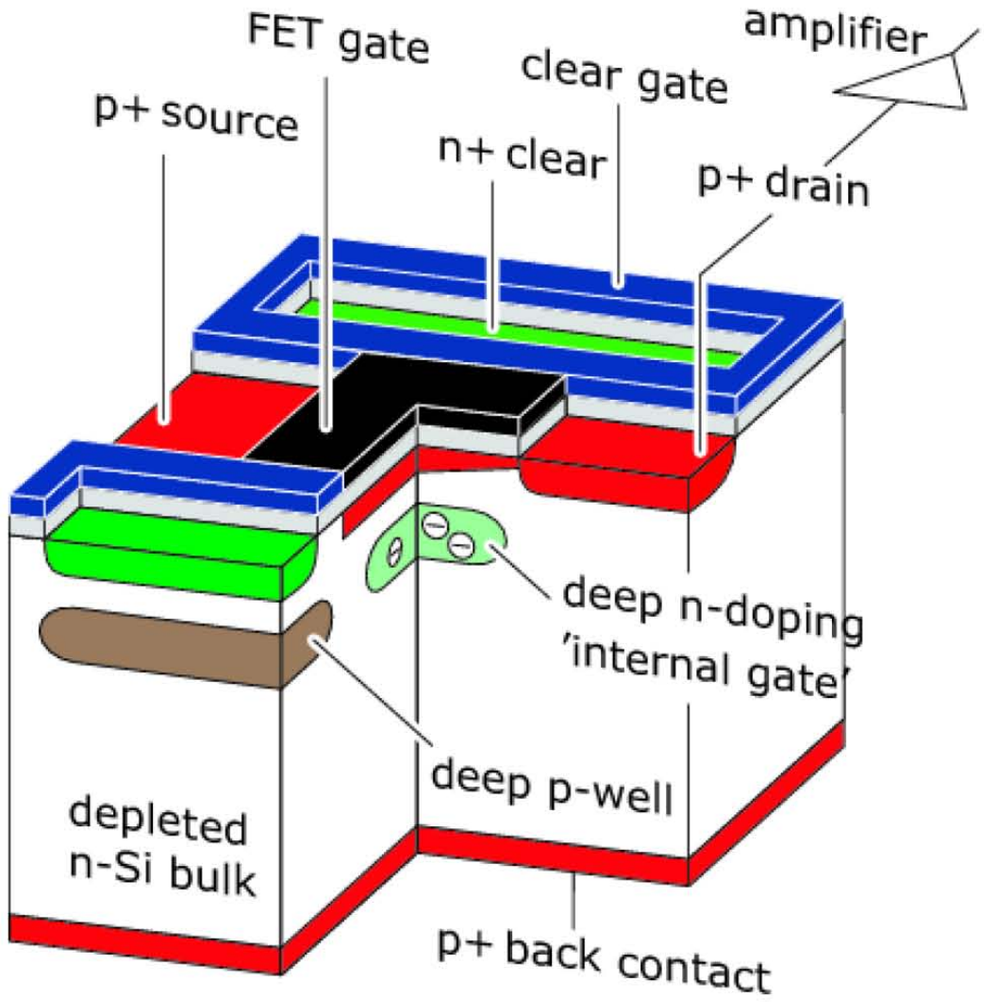
✦Super-high luminosity ~8×10^{35} $cm^{-2}s^{-1}$ (**x40 higher**)

✦Radiation environment: **~1 Mrad per year**

✦Refurbishment of accelerator and detector required

Pixel Detector with DEPFET sensor

- ✦ p-FET (MOSFET) on a **fully depleted bulk** (sideward depletion)
- ✦ signal electrons accumulated in the internal gate modulate the transistor current (g_q~600pA/e-) → **low C_D, low noise**
- ✦ charge collection during external gate being switched off → **low power**
- ✦ integrating device, discharge internal gate with positive pulse applied to the clear contact



→See posters by Peter Kodys & Christian Koffmane

Front-end ASICs for PXD

- Active pixel area thinned to 50 µm
- Independent read-out from both sides
- ASICs bump bonded onto the DEPFET substrate

✦ **SWITCHER**

- high voltage (10-20V) pulses for clear and gate lines

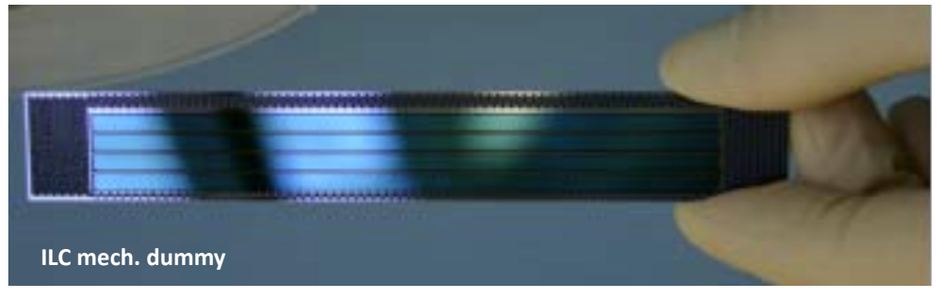
✦ **DCD** (Drain Current Digitizer)

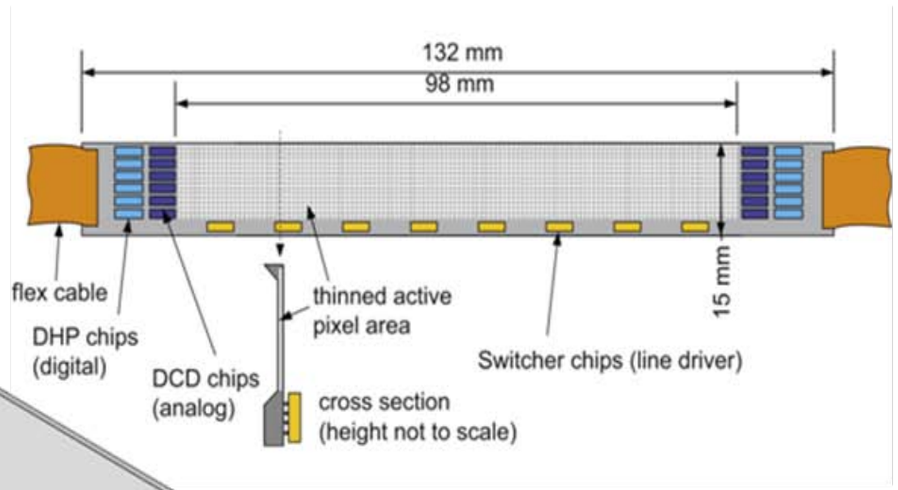
- receive drain current signals from DEPFET
- sample and subtract pedestal currents
- digitize signals
- 4:1 multiplex ADC outputs

✦ **DHP (Data Handling Processor)**

- data reduction
- sending data off the module to the backend

"All-silicon" DEPFET module





Data Handling Processor (DHP)

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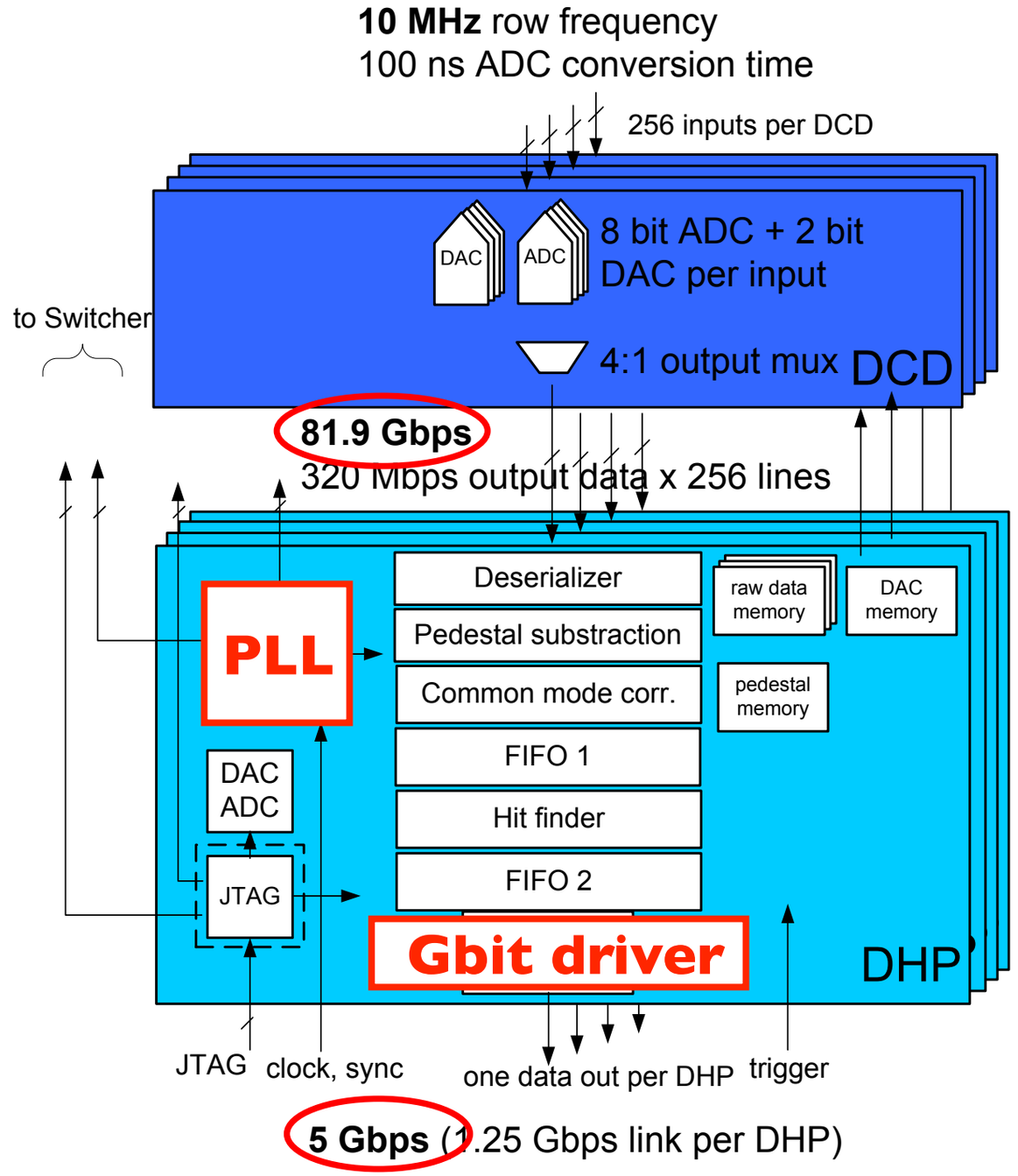
✦ **Functionality**

– Module controller
  • JTAG bus to DCD and SWITCHER chips
  • Clock & timing generation & distribution
– Data reduction (1/20)
  • 0-suppression
  • triggered r/o

✦ **Data processing**

– Raw data buffer
– Fixed pattern noise correction
– Hit finder (FIFO1 + FIFO2)
– Framing (AURORA)
– Serializer + Gbit link driver



Synchronized clock generation (PLL) + Gbit link driver

DHP Data Link Specifications

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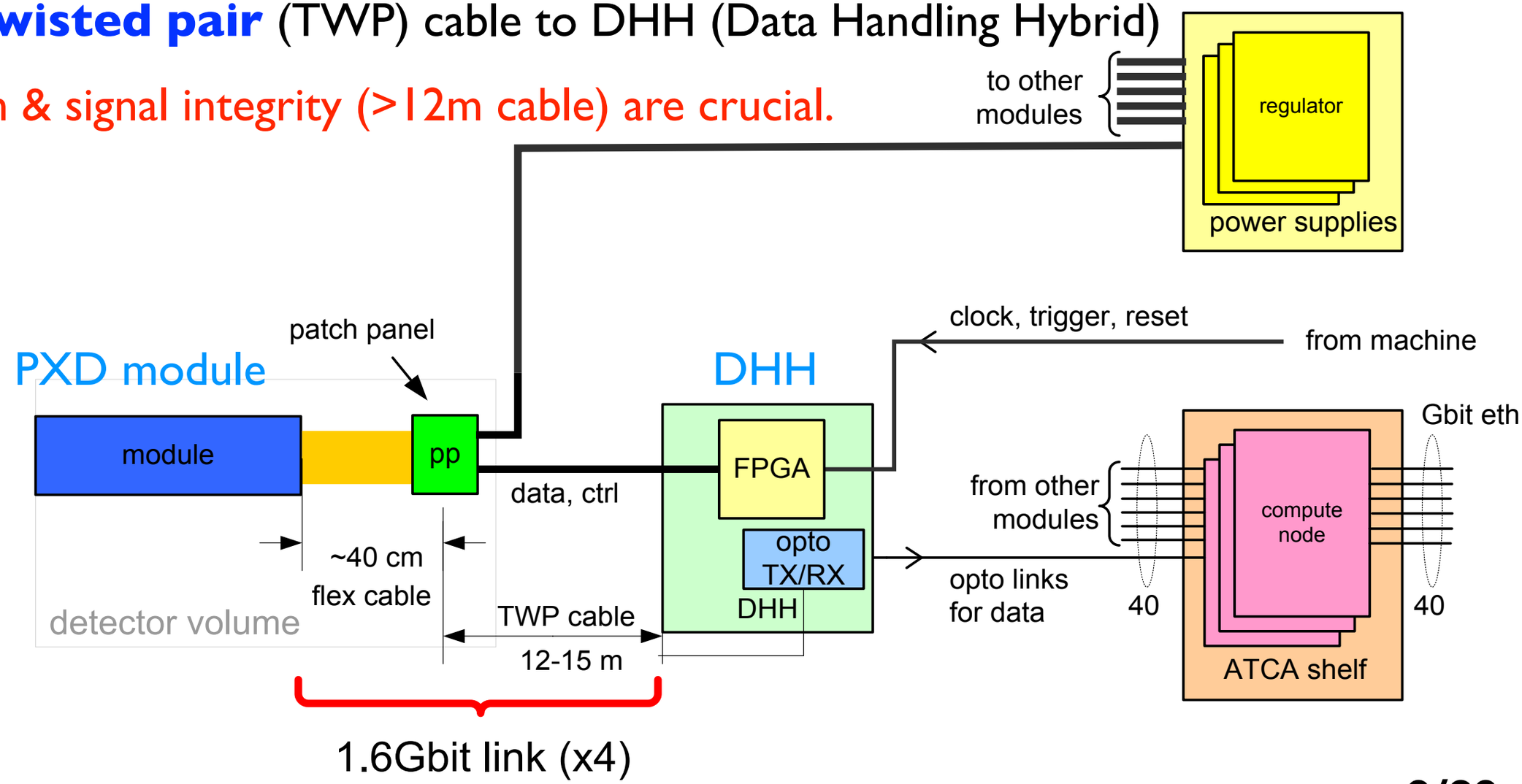
- ✦ 1.6 Gbps per DHP chip, four links per module (incl. 20 % overhead)
- ✦ Electrical link (optical data transmission not feasible due to radiation tolerance requirements)
- ✦ **40 cm flex-cable** up to patch panel (PP)
- ✦ **12-15m twisted pair** (TWP) cable to DHH (Data Handling Hybrid)

Link bandwidth & signal integrity (>12m cable) are crucial.



Test Chips

✦ DHP 0.1, **IBM 90nm**, submitted March 2010

– C4 bumps

– **half size** chip (32 inputs)

– Full data processing

(1.6 GHz PLL , Gbit link driver)

✦ DHP 0.2, **IBM 90nm**, submitted July 2011

– **full size** chip (64 inputs)

– improved data processing & hit finder

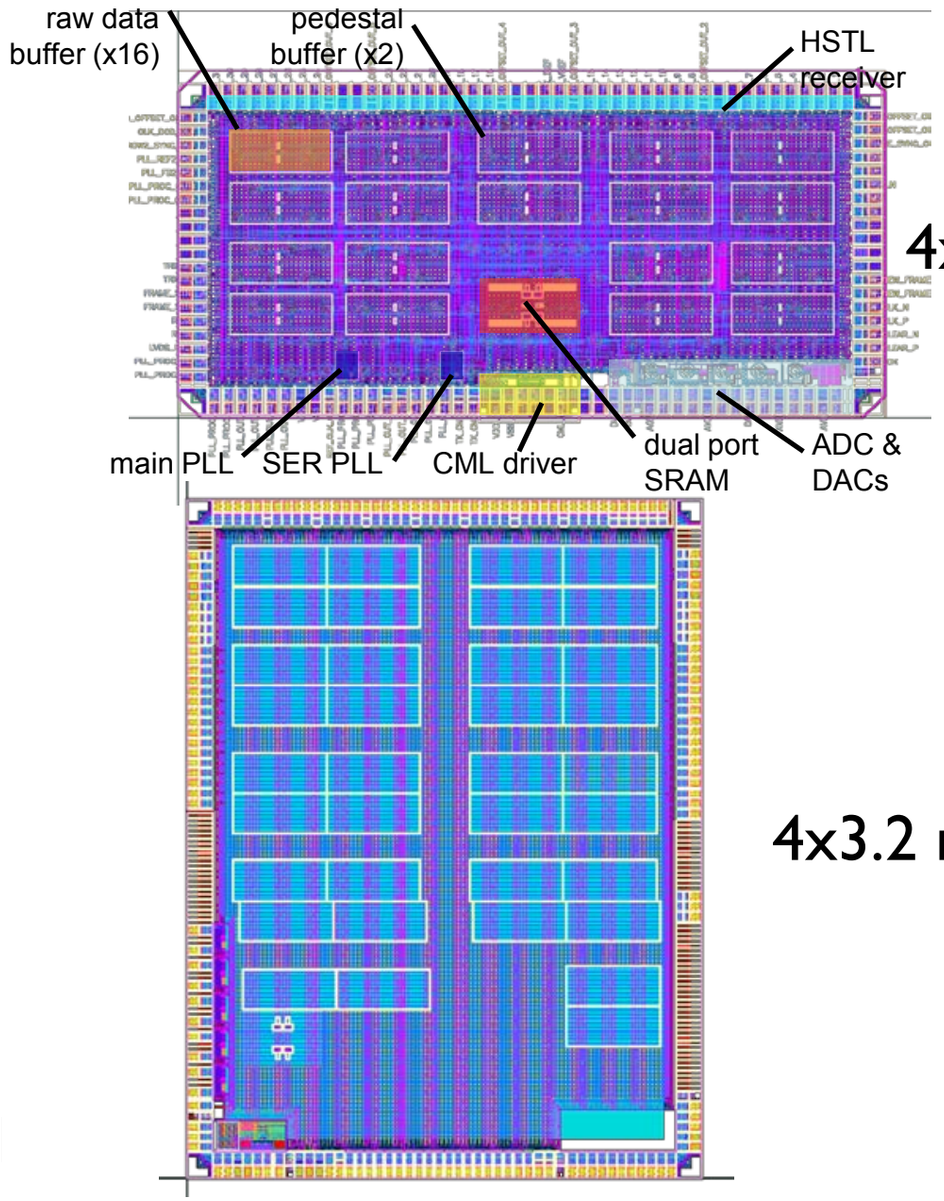
– CML driver with programmable pre-emphasis

– Bias DACs & temperature sensor

✦ **DHPT 0.1**,**TSMC 65nm**, submitted Oct 2011

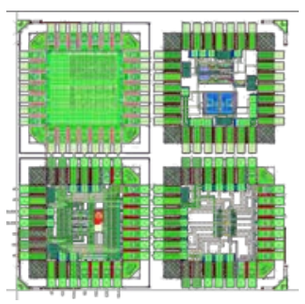
– 4 separate chiplets:

Analog designs are challenging.



4x2mm^2

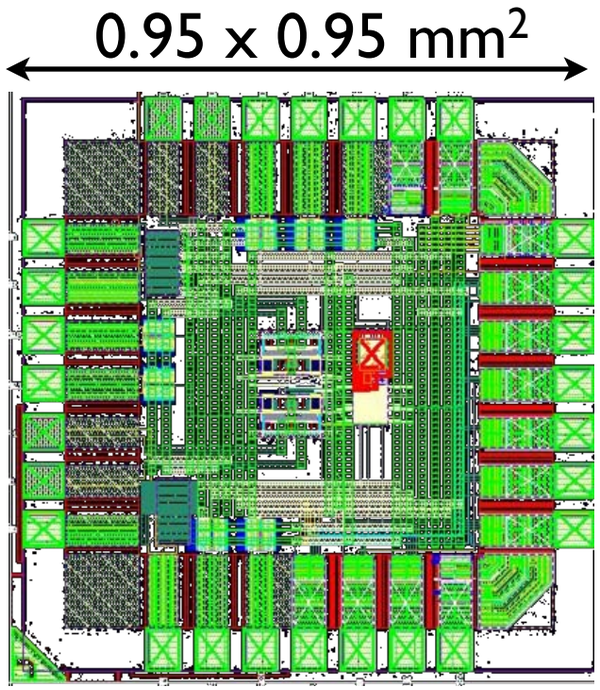
4x3.2 mm^2



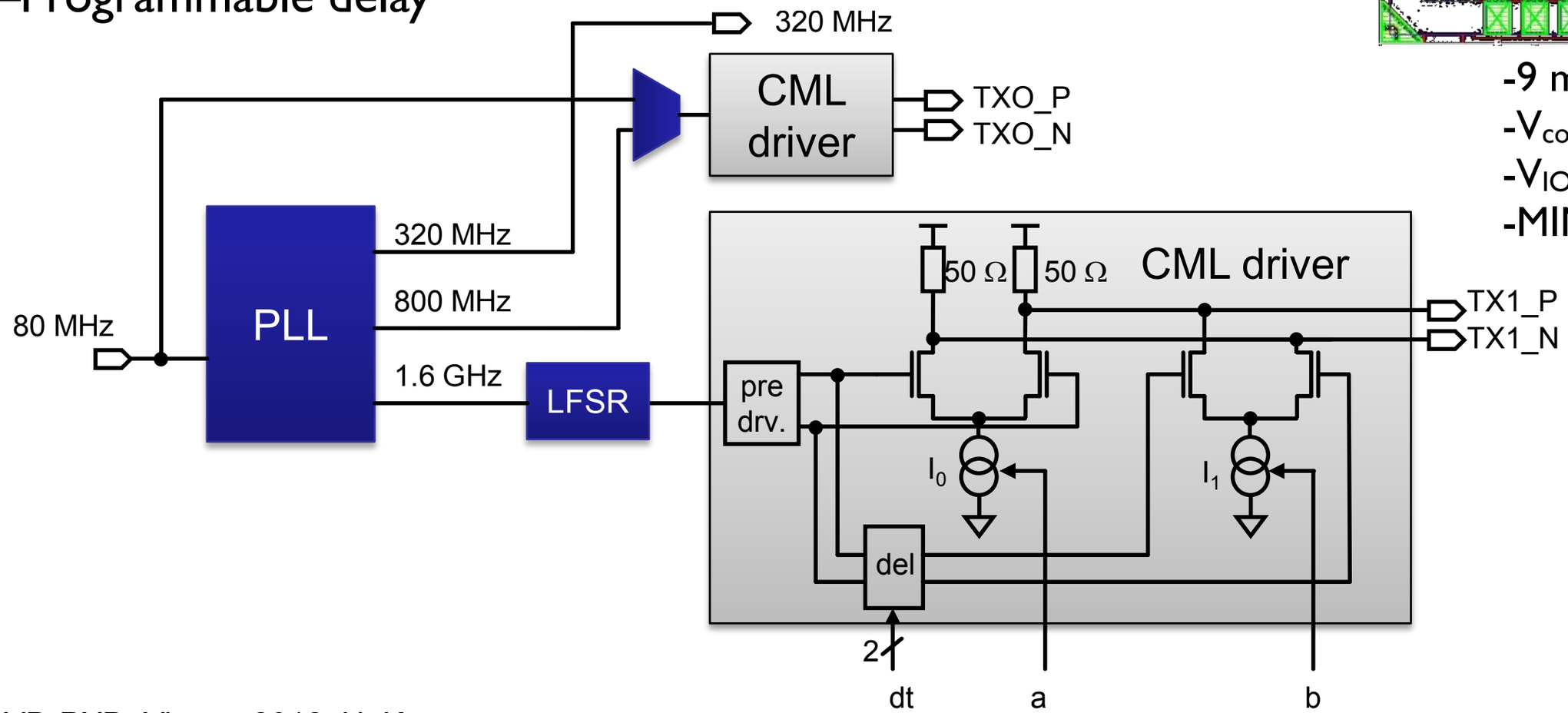
1.9x1.9 mm^2

DHPT0.1 with TSMC 65-nm CMOS

- ✦ **PLL (Phase-Locked Loop)**
  - 80 MHz reference clock
  - 1.6 GHz, 800MHz & 320 MHz outputs
- ✦ **Pseudo random bit sequence generator**
  - 8 bit LFSR
- ✦ **CML link driver** with programmable pre-emphasis
  - Two differential pairs with adj. bias currents
  - Programmable delay

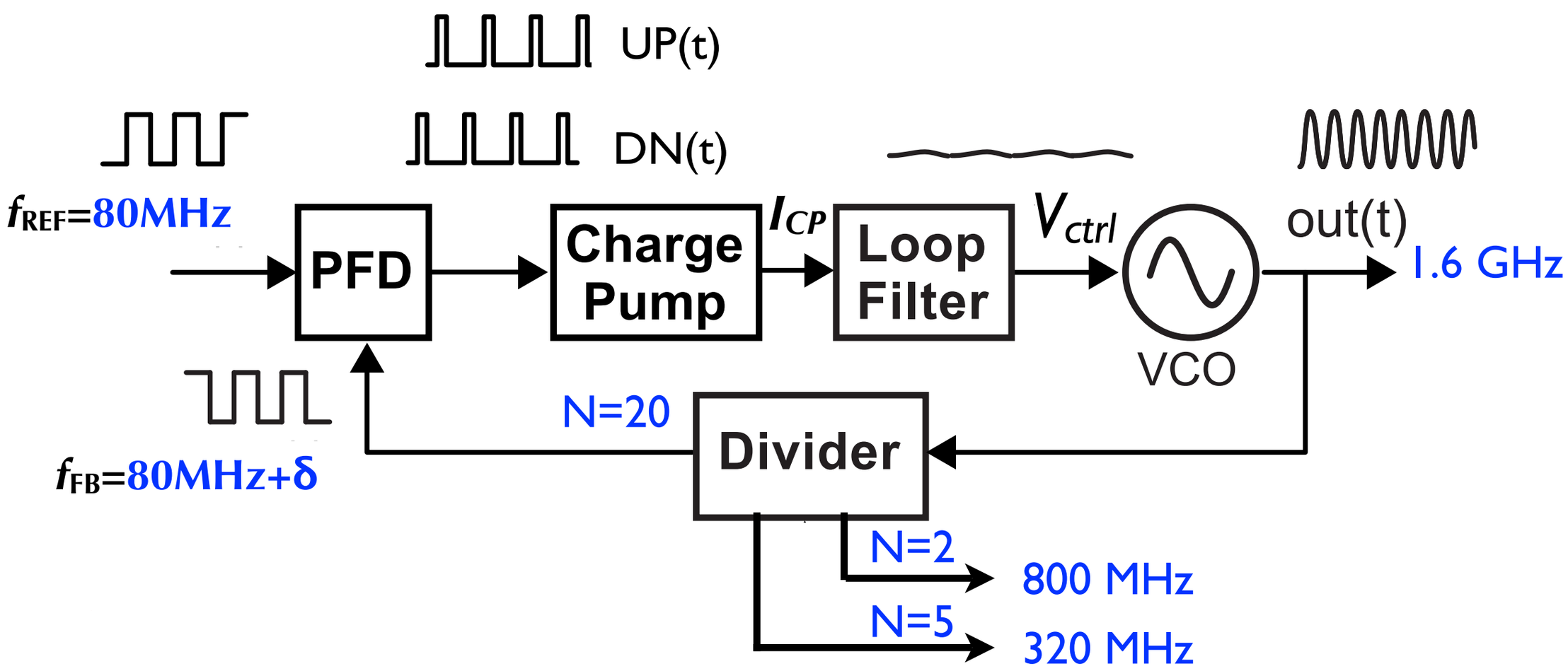


- 9 metal layers
- V_{core}=1.2 V
- V_{IO}=1.8 V
- MIM option

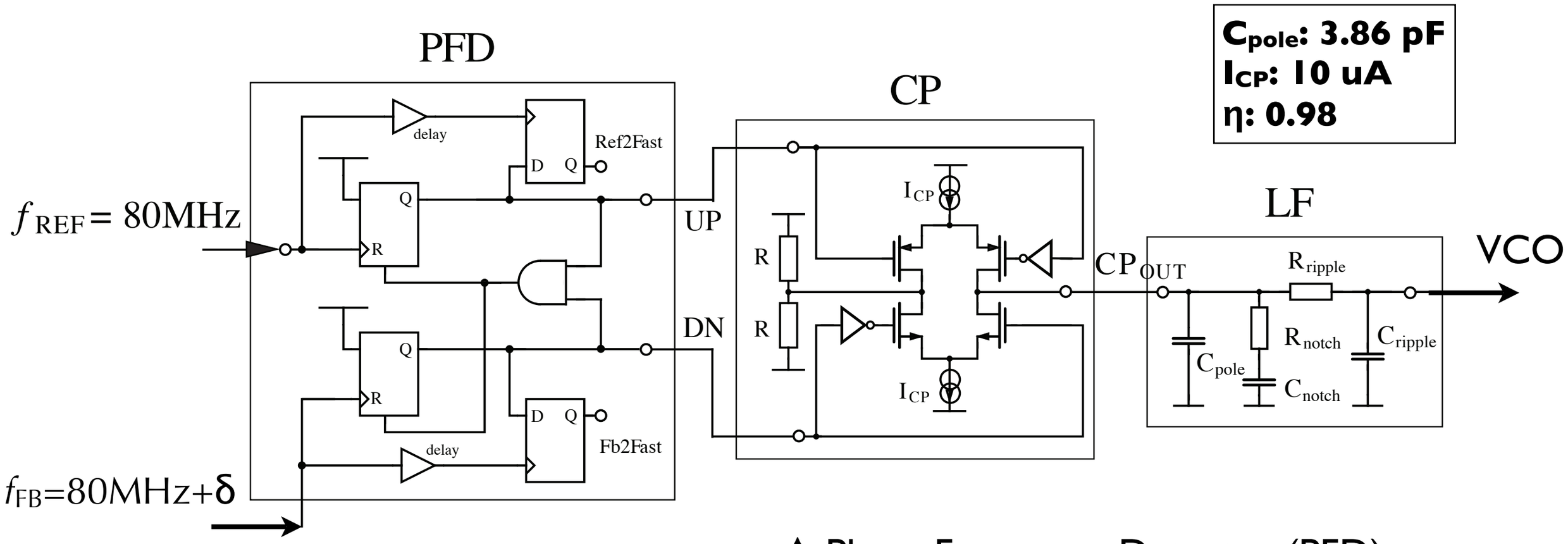


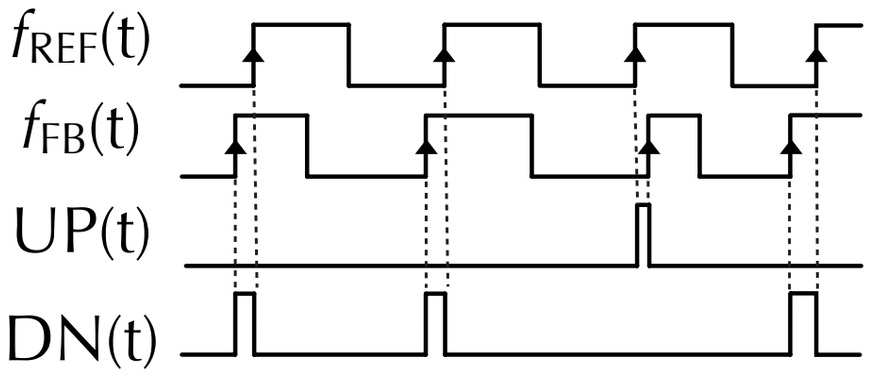
Charge-pump PLL

- ✦ Voltage Controlled Oscillator (VCO) provides oscillating waveform with variable frequency
- ✦ PLL synchronizes VCO frequency to input reference freq. through feedback
- ✦ Use digital counter structure to divide VCO frequency



more schematic details...



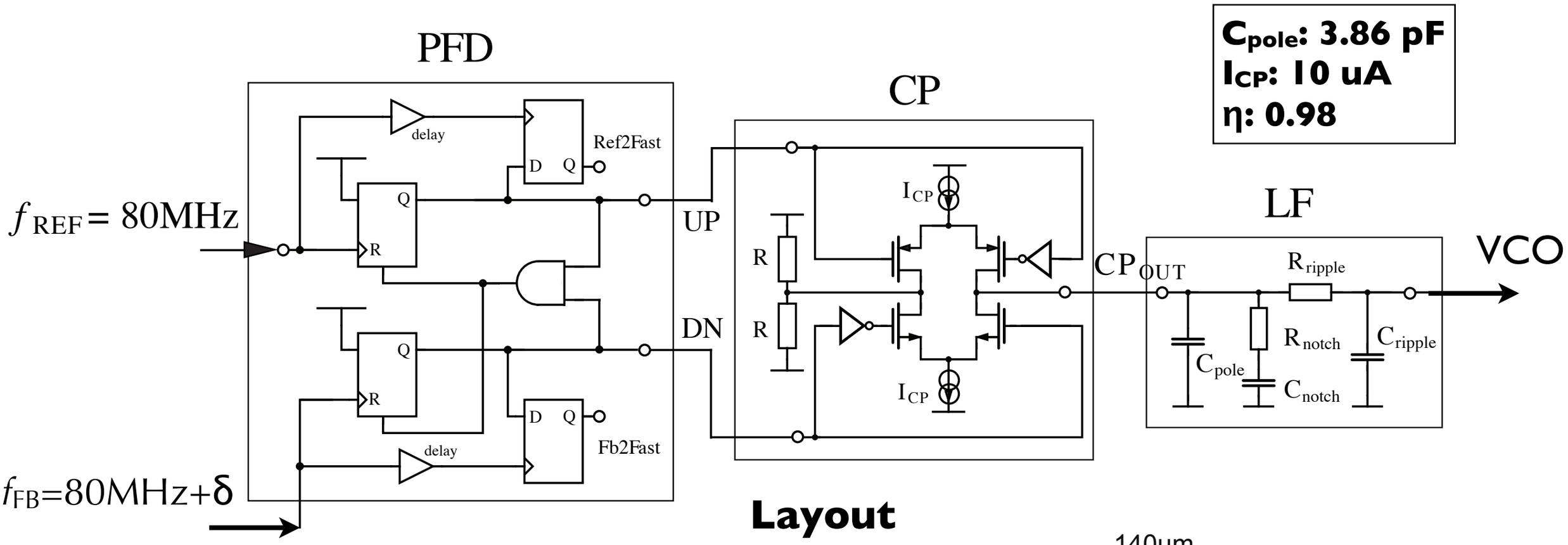


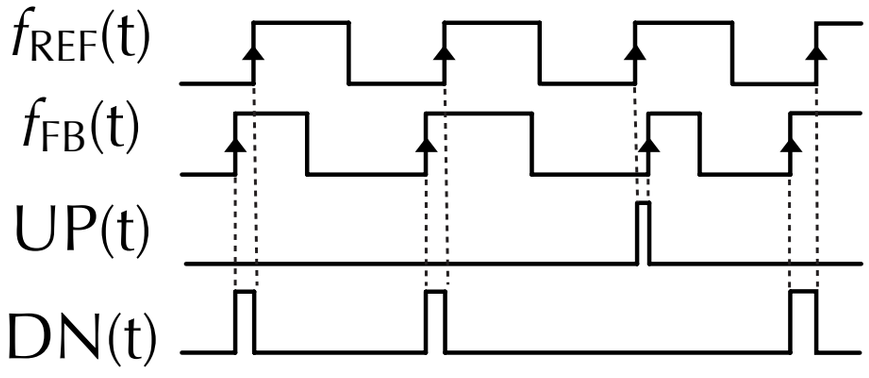
✦ Phase-Frequency Detector (PFD): classical two flipflops structure, additional error detection circuit

✦ Charge-pump (CP): differential structure with dummy branch

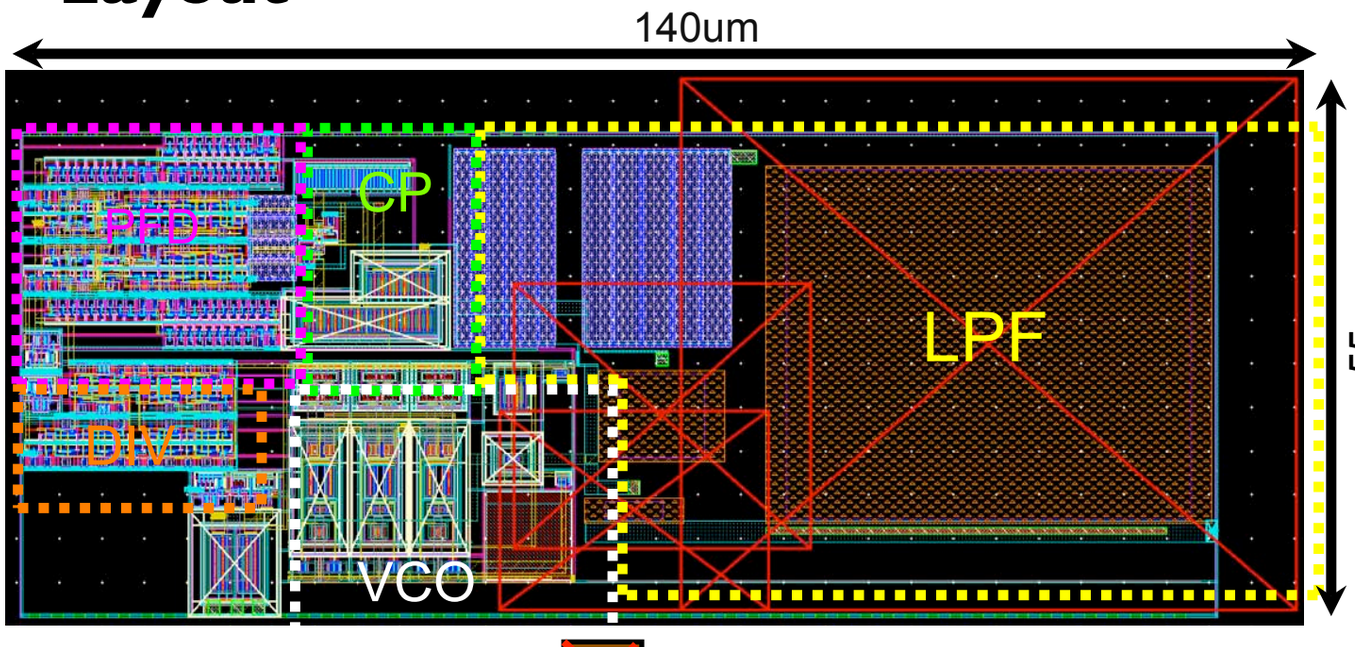
✦ Loop-filter (LPF): MIM structures, well-tuned parameters for PLL stability

more schematic details...





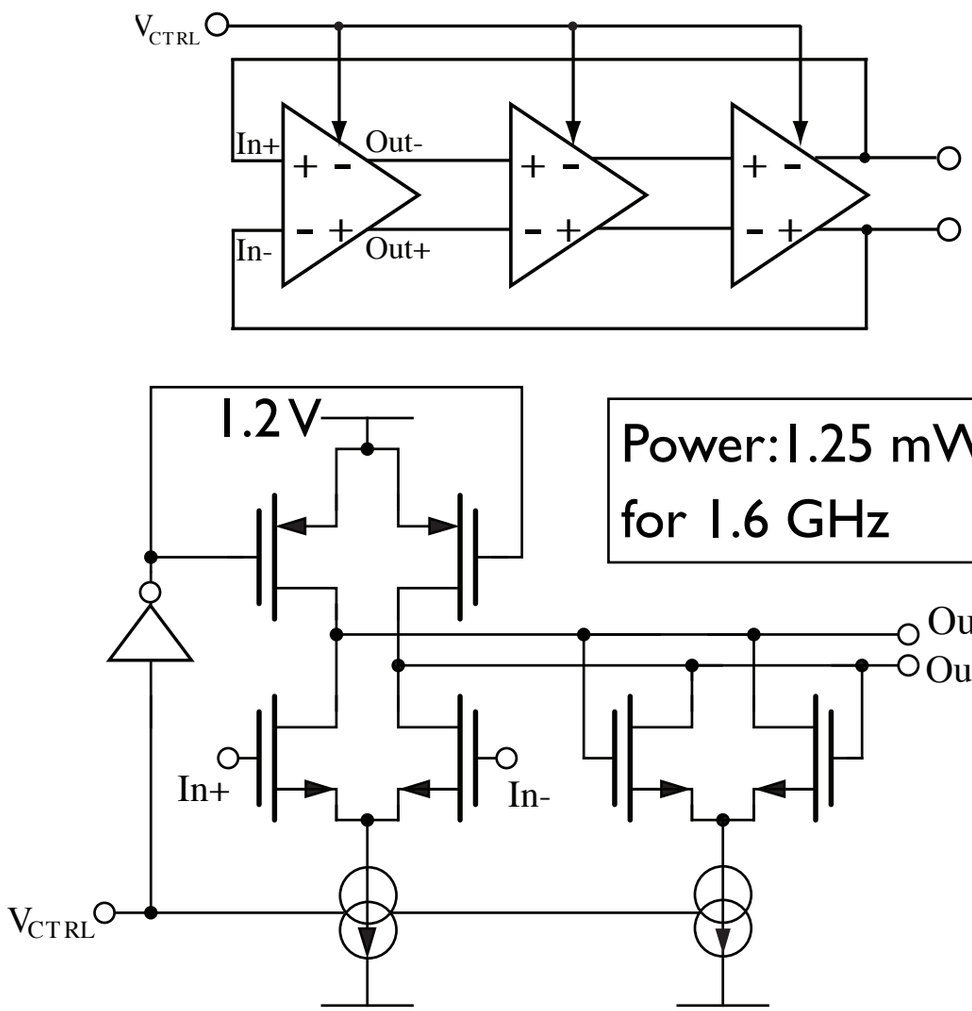
Layout



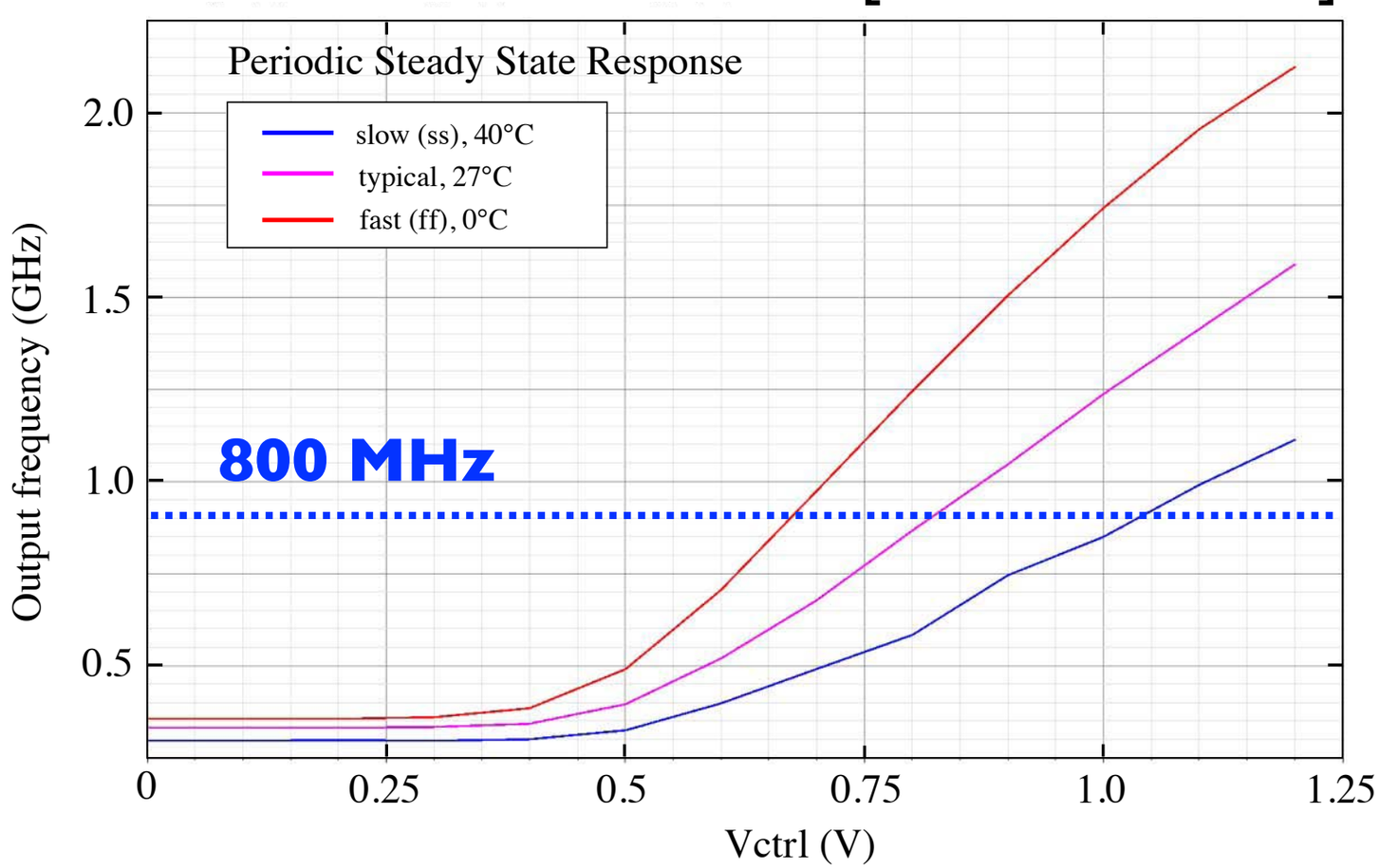
→MIM cap.

Voltage-Controlled Oscillator (VCO)

- ✦ three inverters connected as a ring oscillator
- ✦ differential pairs with PMOS loads with cross-coupled stages for rail-to-rail switching



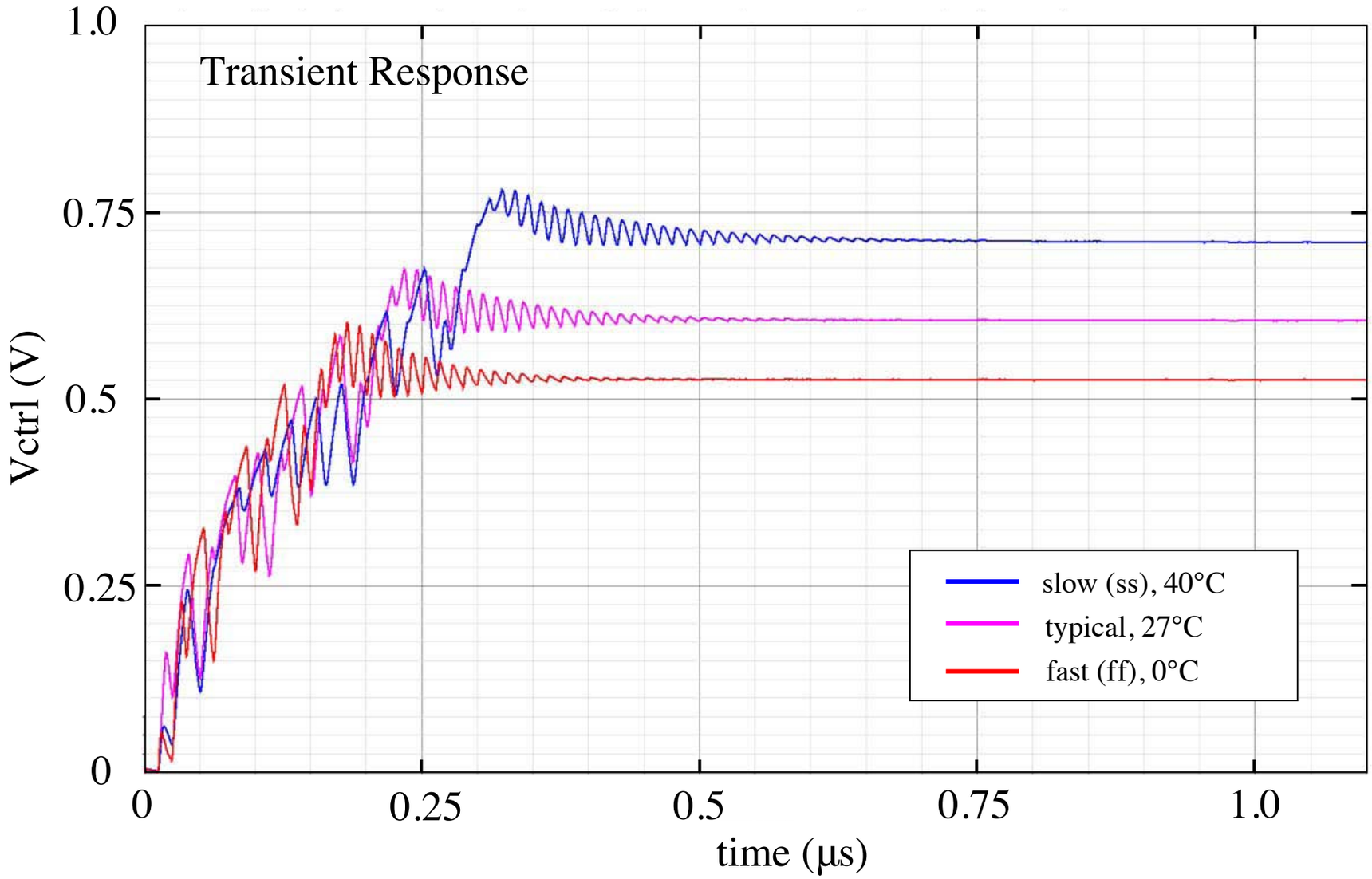
[800 MHz vs. Vctrl]



- ✦ wide tuning range of the output frequency
- ✦ oscillation freq. of 1.6 GHz is secured under 3σ process variations.

PLL Settling Behavior

- The V_{ctrl} settles to the final value in t_{settle}~750 ns within accuracy of 2%.
- Stable behavior for all process corners.
- Layout parasitics are included in the simulation.



CML Driver with pre-emphasis

- Differential current mode logic (CML):

  driver (phase control) + differential pair post driver

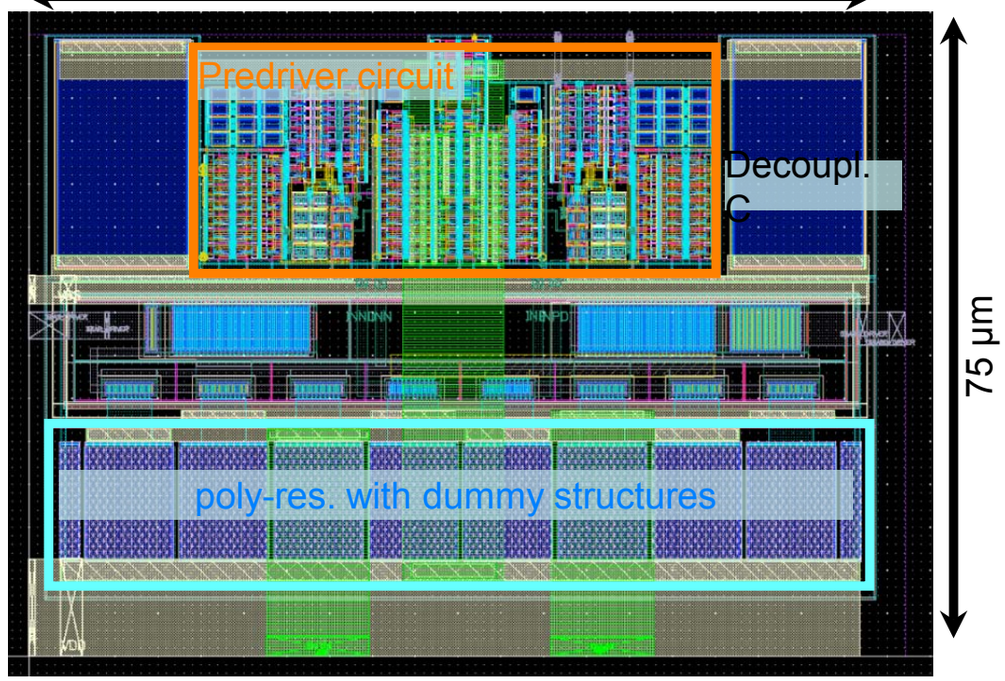
- Two differential pairs: adj. bias currents:

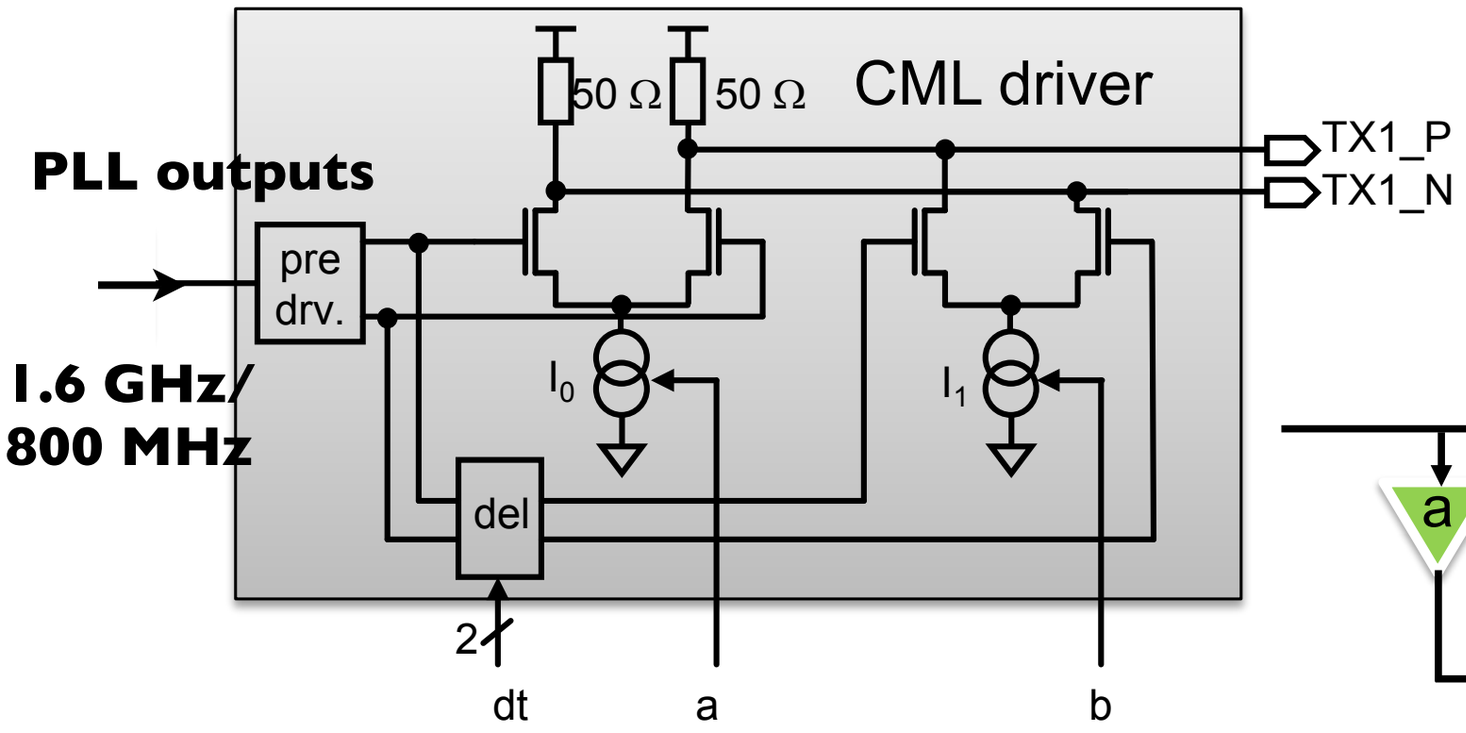
  - tap weights (a & b),

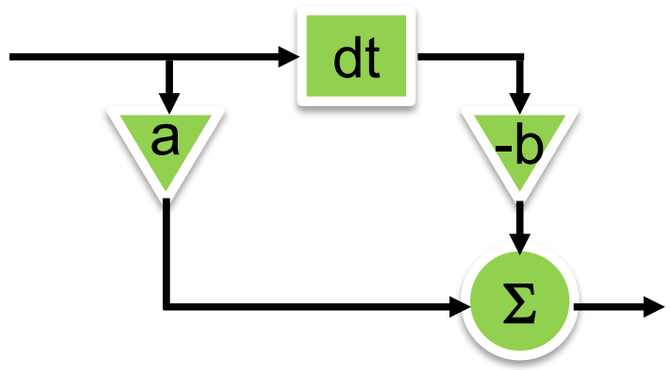
  - delay (dt) upto 600ps with 4 fixed steps

- Dummy poly layout for impedance matching

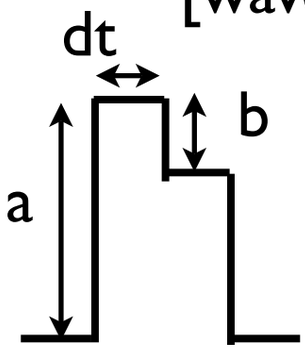
Layout







[waveform]



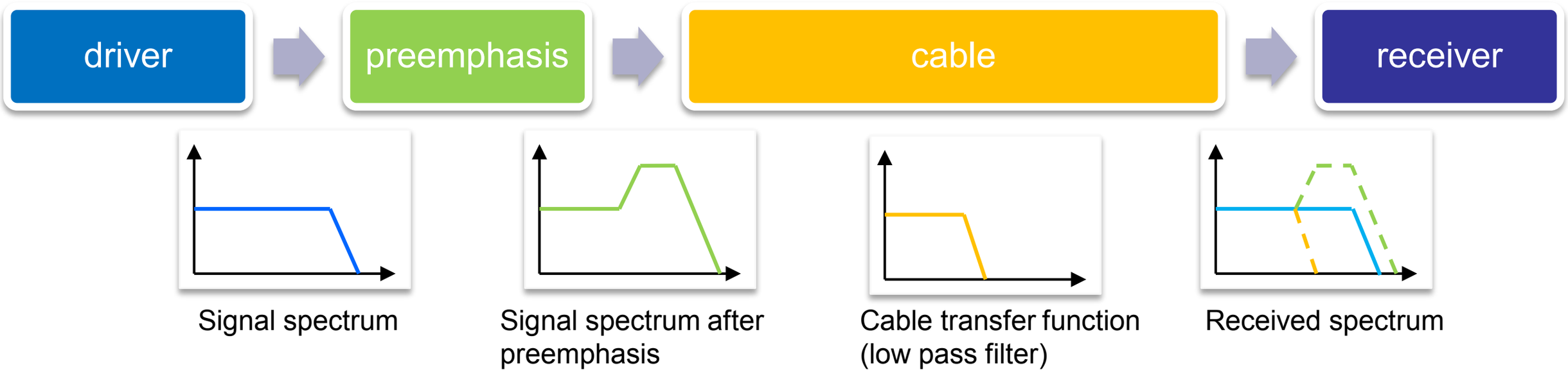
Why pre-emphasis is necessary?

Signal integrity is affected by

✦ Driver
- PLL jitter → phase noise
- signal rise time

✦ Cable (12-15m long → high frequency attenuation)
- resistive loss (skin effect) → large cable diameter
- dielectric loss → low εr

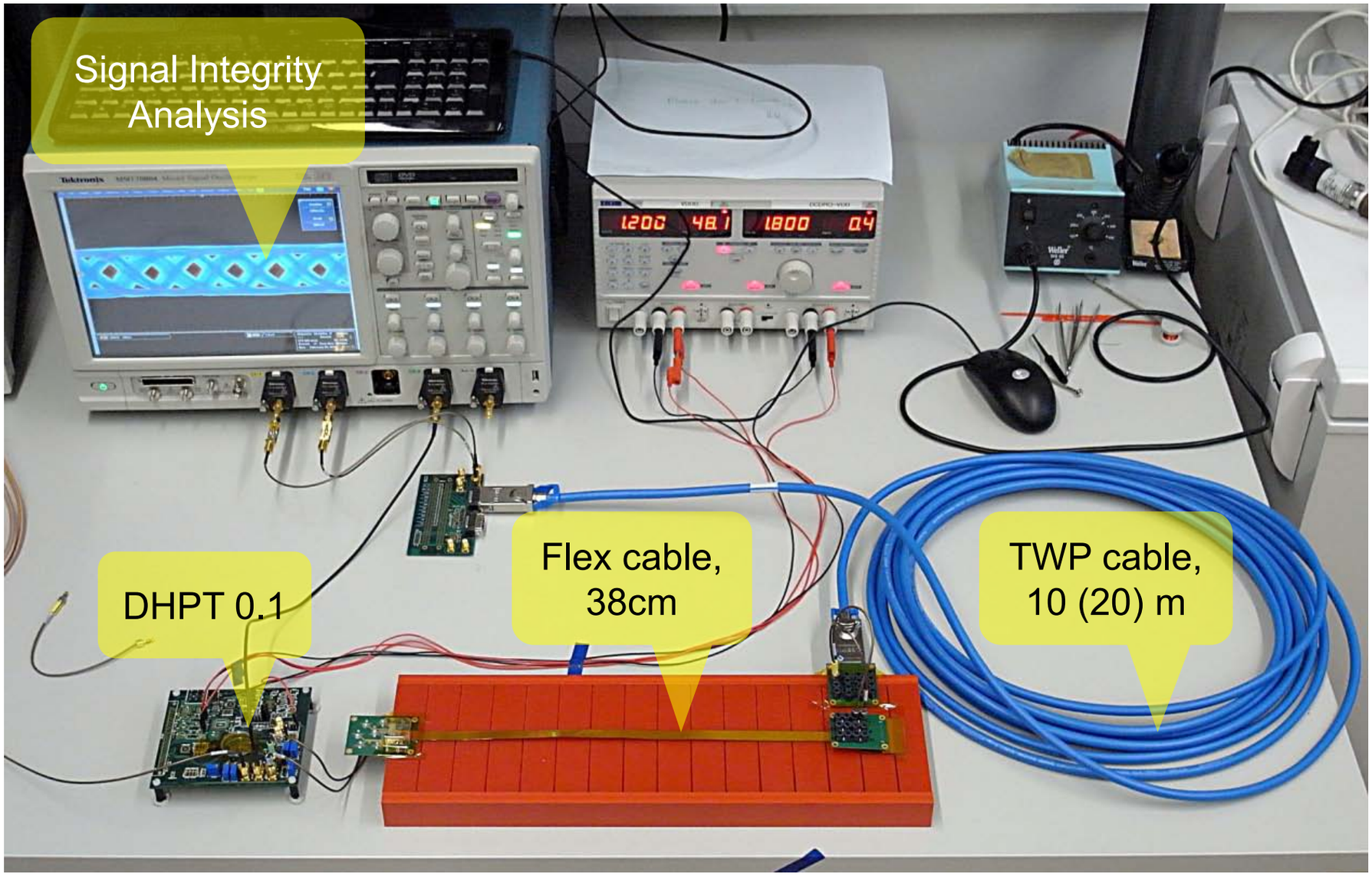
✦ Cross-talk → shielding



Compensate signal losses by shaping the transmitted pulse response (boosting high frequency component) **→necessary for Gbit driver**

Measurement setup

800 MHz output connected to the oscilloscope
1.6 GHz LFSR output connected with flex & twisted cables



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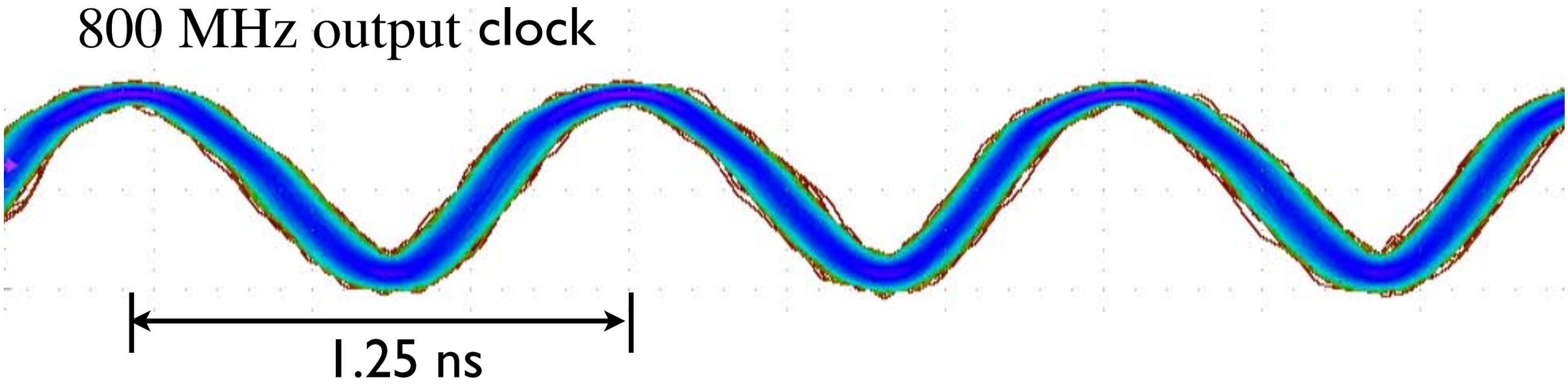
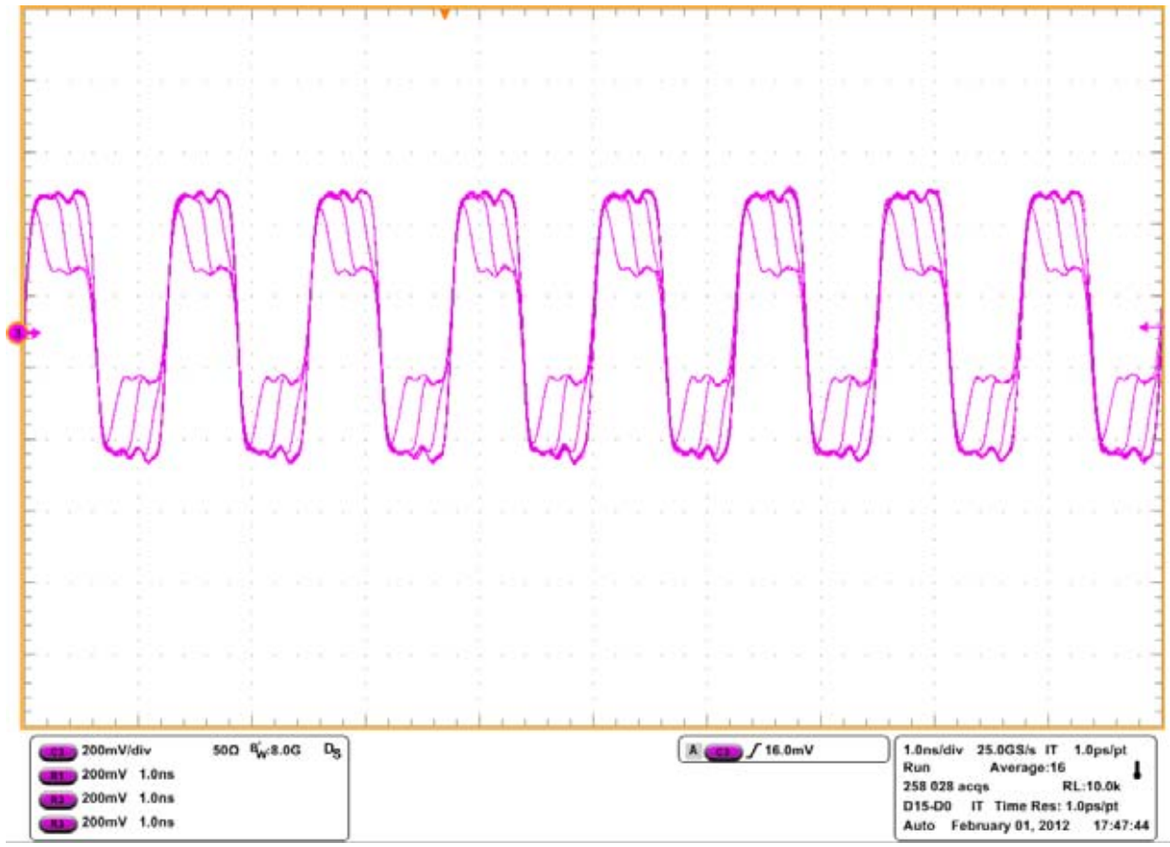


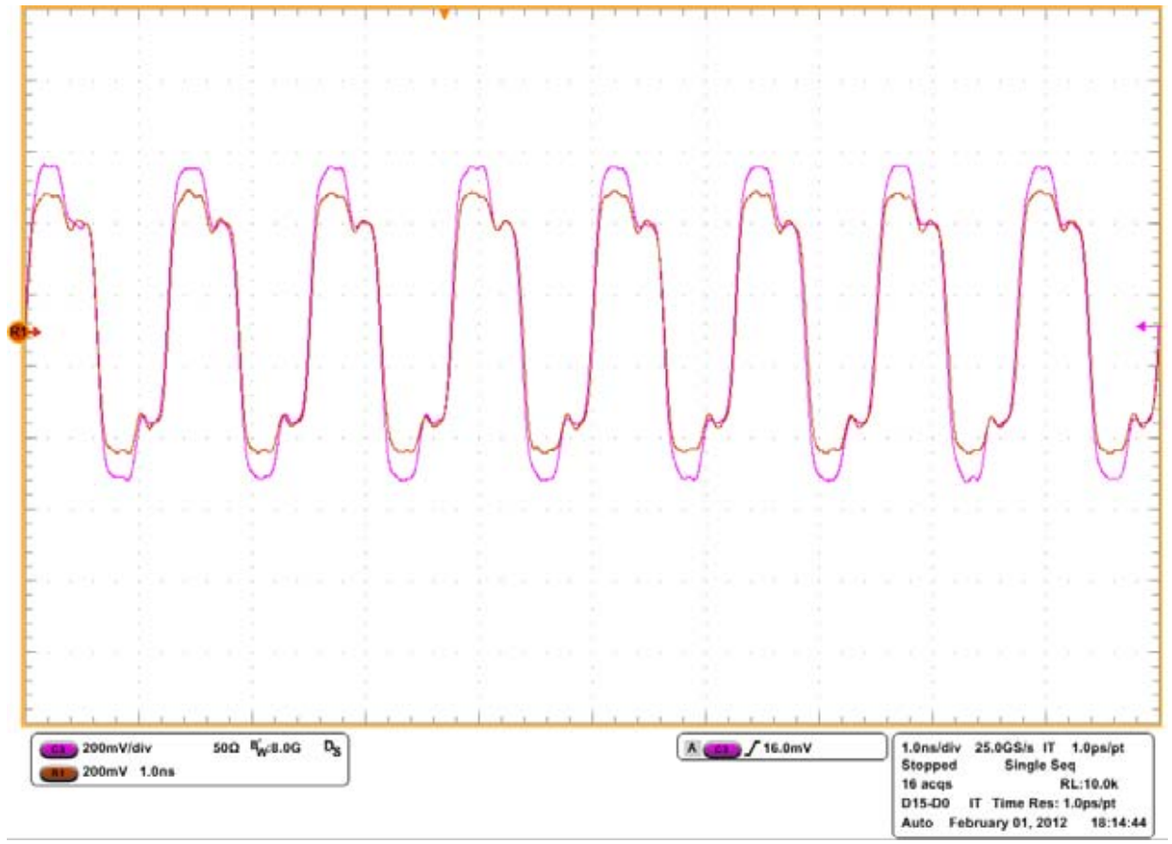
→precise clock generation

Pre-emphasis Measurements

Check 800 MHz output with CML pre-emphasis on
(directly connected to the oscilloscope) →pre-emphasis works as expected



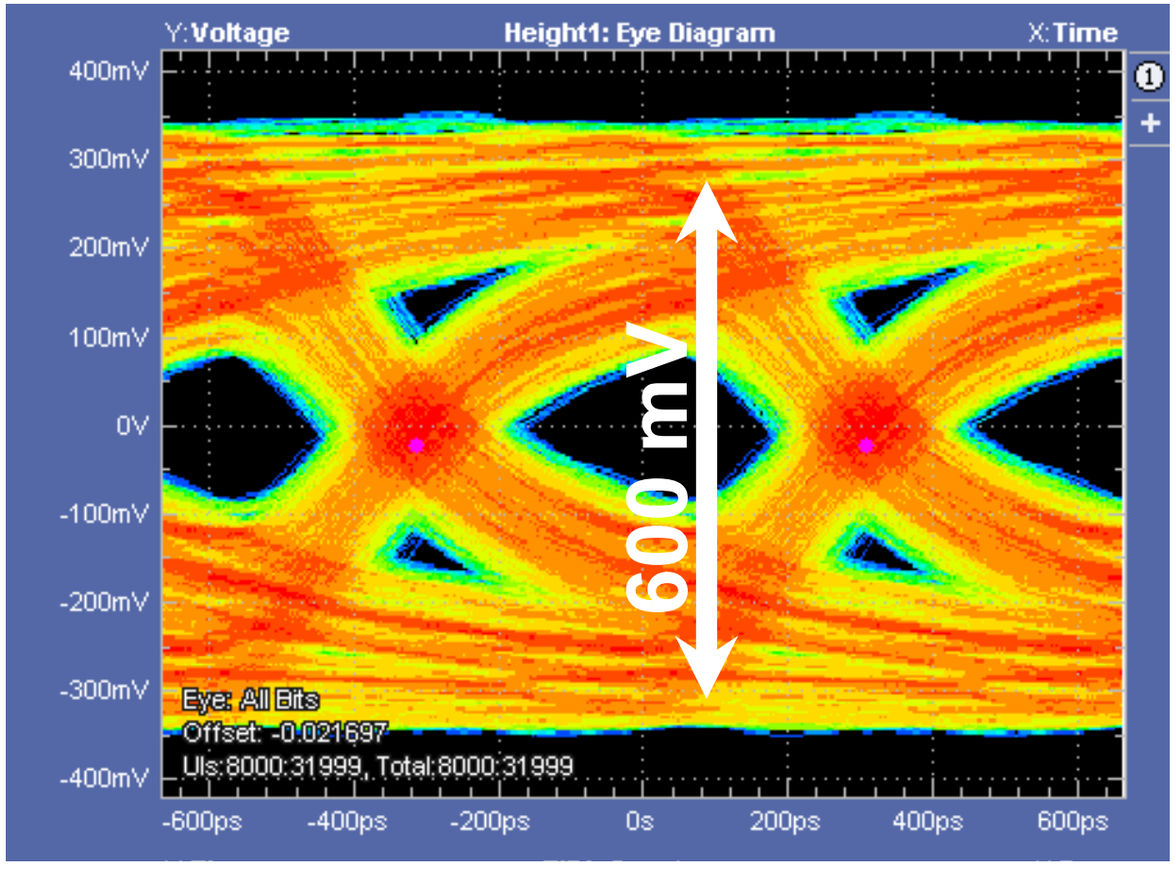
variable delay settings



variable tap weight settings

Signal Integrity Analysis

- ✦ Measure vertical & horizontal **eye opening**
- ✦ Pseudo random bit sequence as a signal source
- ✦ 1.6 Gbps, 8bit LFSR sequence
- ✦ **10m** Infiniband cable (LEONI, AWG 26)



← **bad eye opening**

Pre-emphasis: off

Signal Integrity Analysis

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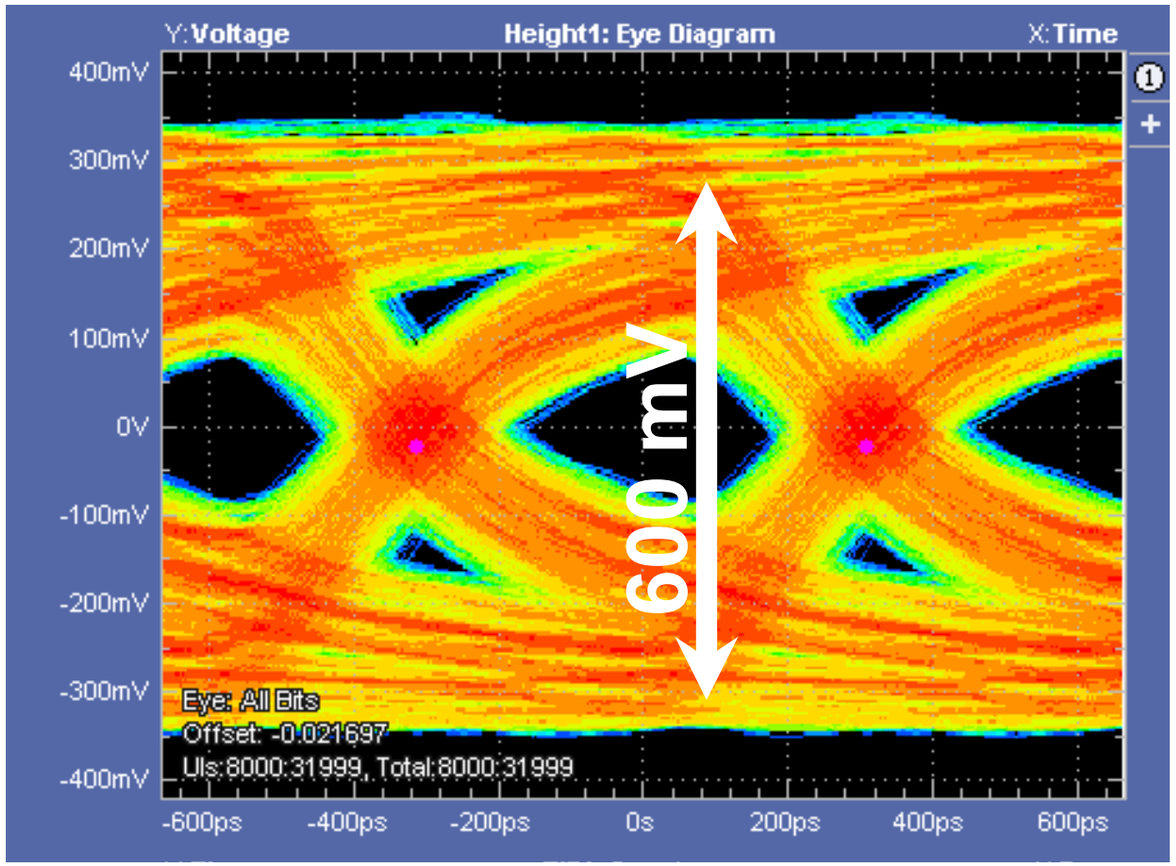
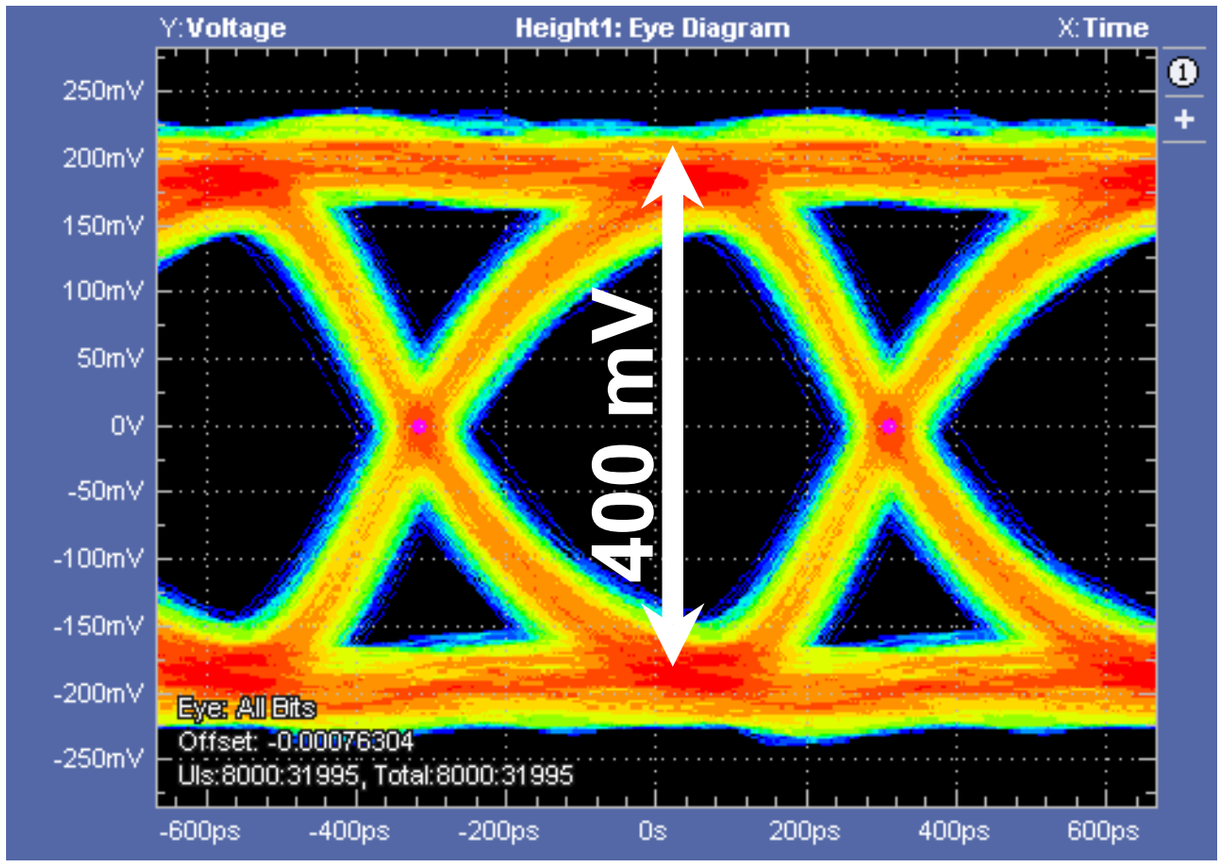


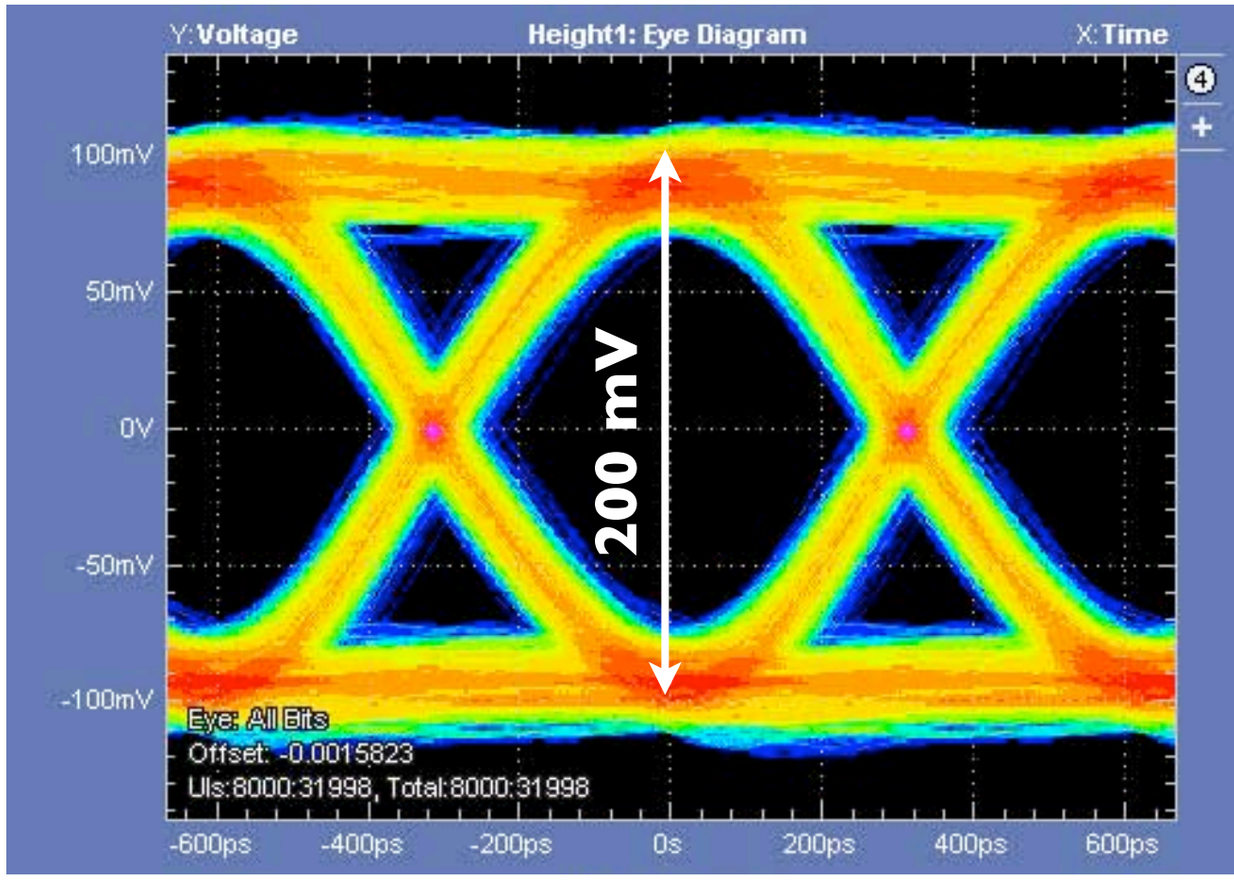
Pre-emphasis: off

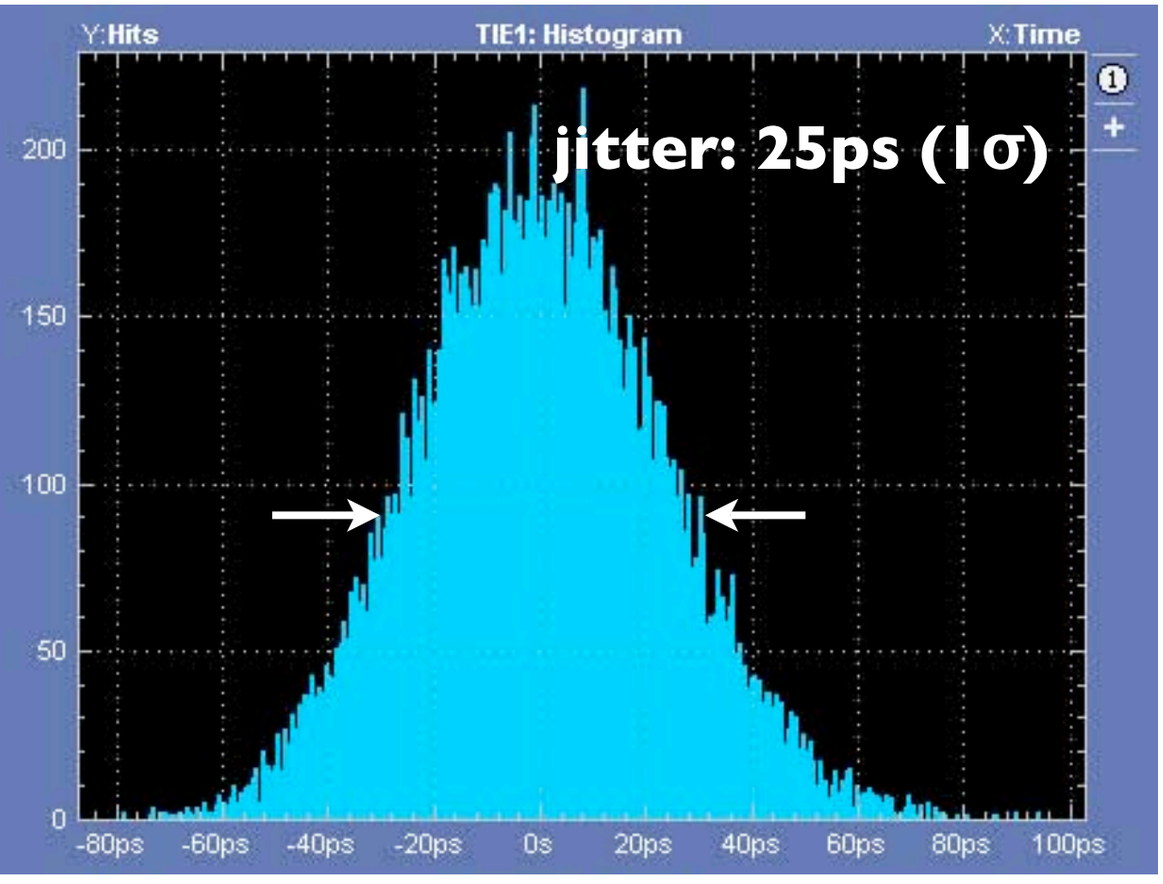


Pre-emphasis: on
(dt=600 ps & max. tap weight)

Signal Integrity Analysis

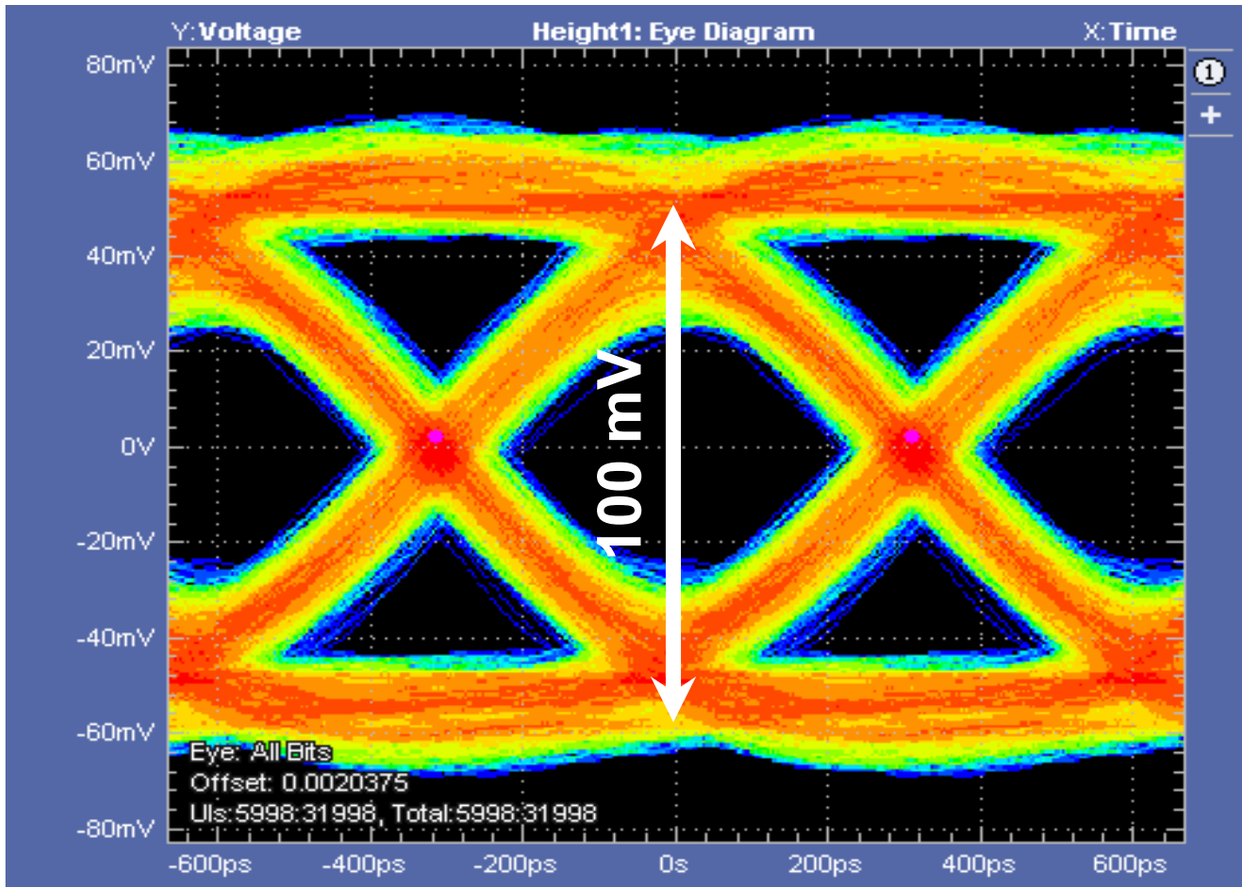
- ✦ 1.6 Gbps, 8bit LFSR sequence **38 cm flex** (I.V.) **+ 10m** Infiniband cable (LEONI, AWG 26)
- ✦ Max. pre-emphasis settings

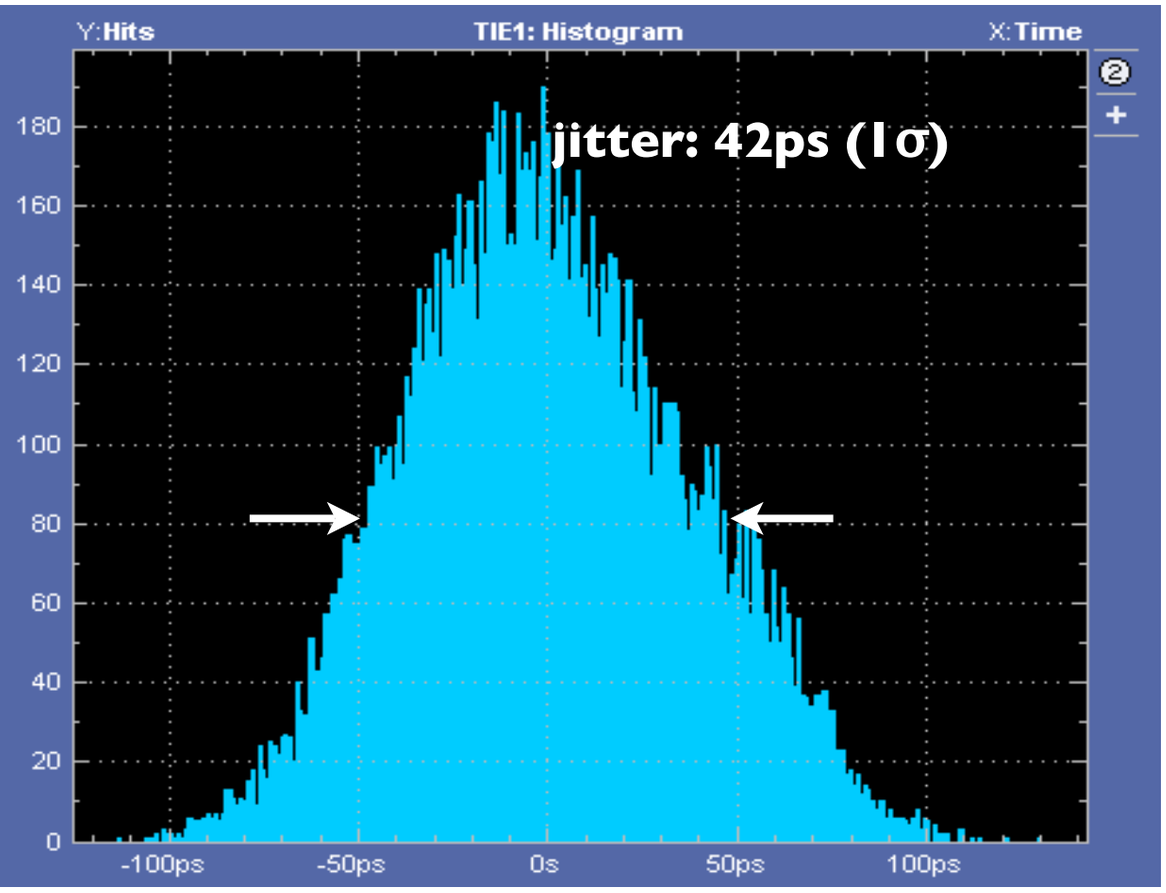




Signal Integrity Analysis

1.6 Gbps, 8bit LFSR sequence **38 cm flex** (I.V.) **+ 20m** Infiniband cable (LEONI, AWG 26)
Max. pre-emphasis settings





Intrinsic rad. hardness (t_{ox}~1-2 nm) is attractive for future high-energy experiments.

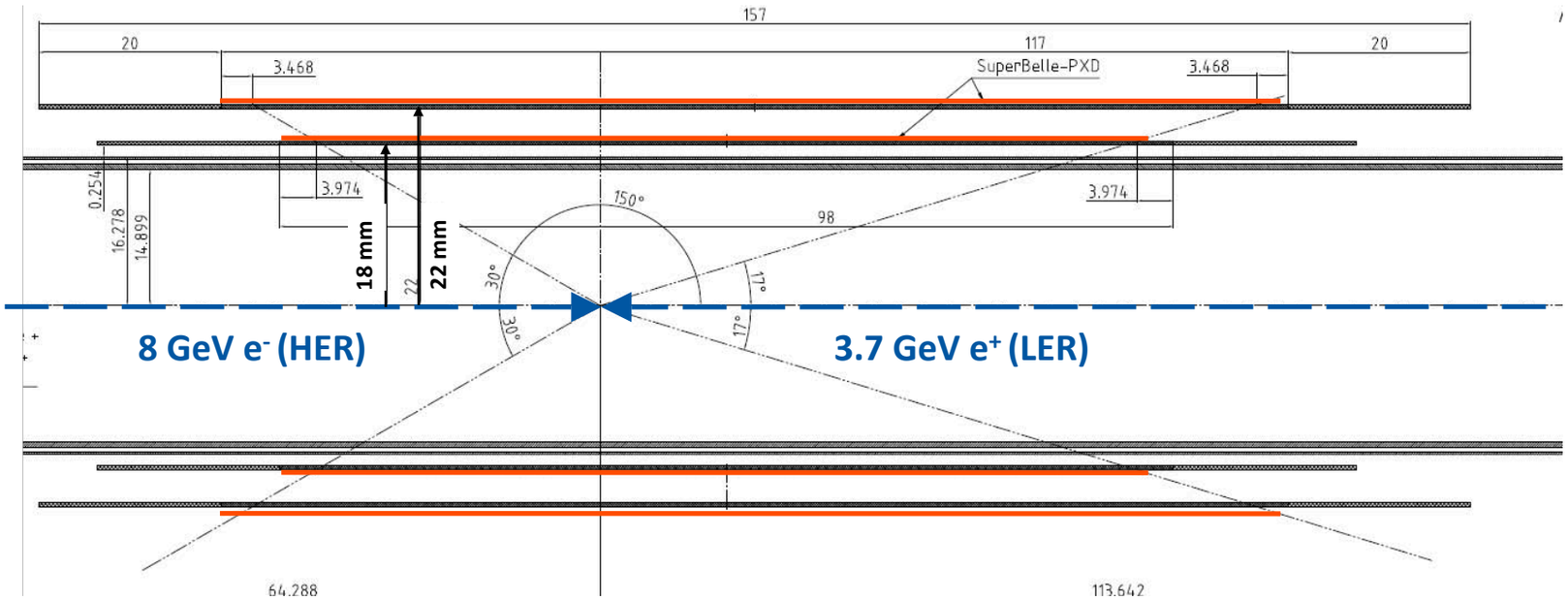
Summary

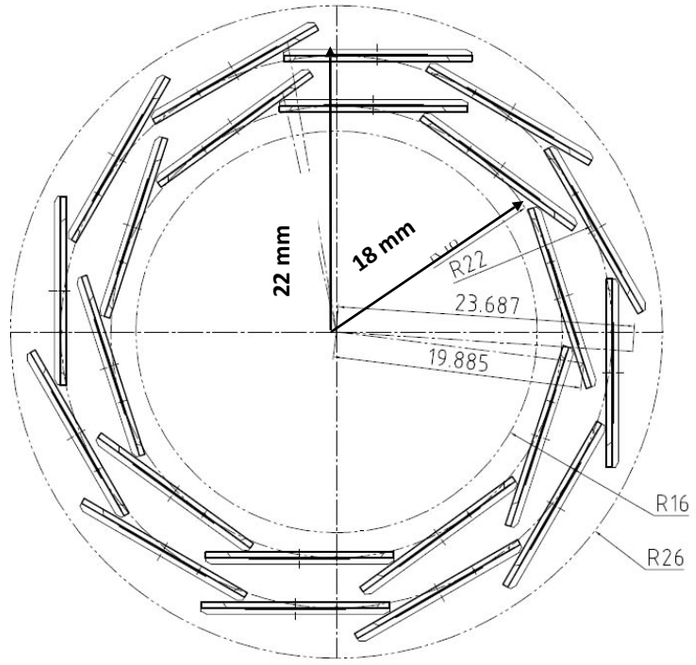
- ✦ DHPT 0.1, test chip, TSMC 65nm, shipped Jan. 2012, full custom blocks
  - good signal integrity for 1.6 Gbps with flex + 10m (20m) Infiniband cables
  - Irradiation tests (TID for PLL & Gbit driver) under way
- ✦ Another 65nm test chip was submitted in Mar. 2012
  - LVDS RX/TX for JTAG
- ✦ Full size chip (DHPT 1.0, TSMC 65nm) to be designed & submitted by fall 2012

Thank you for your attention.

Backup slides

DEPFET Pixel Vertex Detector – PXD





- occupancy: ~0.2 hits/µm^2/sec (estimated for 1x10^{35} cm^{-2}sec^{-1}, @ 1.8cm radius)
- spatial resolution : < 10 µm (r-phi**)** (can be less in z)
- pixel size: 50 µm (r-phi) x ~90 µm (z-axis)
- material budget < **0.15 % X$_0$** per layer
- **read-out time: 10 µs**
- radiation level: ~**1 Mrad per year**

- 17° - 150° acceptance (η = [0.55 .. 0.3])
- layer 1: 10 modules at 1.8 cm radius
- layer 2: 12 modules at 2.2 cm radius
- optional layer 0 at 1.3 cm radius with beam pipe upgrade
- half-module active area: 4.9 cm x 1.2 cm (layer1)
- #pixels: 240 x 512
- r/o channels: 960 x 128 (4-fold parallel)
- **sample (row) rate: 12 MHz**