A CMOS Front-End for MPPC-based detectors aimed to TOF applications with fast discriminator, adjustable arming threshold and constant-fraction functionality

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ABSTRACT: We have designed and realized a Front-End chip for MPPC in standard CMOS 0.35 μm technology. The channel presents a low input impedance in order to reduce as much as possible the recovery time of the sensor. This is achieved using the current domain for processing signals through the current conveyors (CCII) as building blocks of the channel. A current feed-back with low-pass filter has also been used to realize a sensitive improvement of the pile-up problem, in case of high repetition rate events. An independent arming threshold is available for each channel, providing the selection of the event through the peak level (proportional to the number of simultaneously hit pixels) reached by the signal. A constant-fraction functionality is present in order to reduce the well know time-walk problem. The delay in the correspondent branch is obtained by using an additional CCII block. The channel is also equipped with analog output and integrated analog output. The digital output of the discriminator channel has adjustable time width. The pilot chip is made up of five channels. All the values of the independent thresholds are stored in 10-bit registers as well as the values of the trigger output width and the main polarization current of the CCII blocks. All the registers are writable from a standard three-wire SPI. These features make the chip fully self-consistent. In this work we present and discuss the simulation results together with the preliminary test performed.

INTRODUCTION

The Front-End is suitable for direct coupling to a MPPC device. Our main target is to build a discriminator with low jitter.

The entire jitter, including the one introduced by the channel, determines the time resolution of the system.
In order to minimize the recovery time, a low impedance input stage has been chosen.

This choice has as a natural consequence to use a *current amplifier* as preamplifier, supported also from the availability in literature of CMOS implementations of fast zero-crossing current comparators used as discriminators.

We used second generation *current conveyors* (CCII) (1) as building blocks for amplifiers.

In this chip all signals and thresholds are processed in the *current-mode domain*.

THE CCII BUILDING BLOCK AND THE CMOS IMPLEMENTATION

The ideal basic CCII block is a three-terminal device, its main features are depicted in the fig. 1.

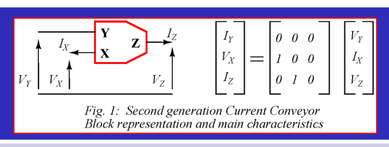


Fig. 1: Second generation Current Conveyor Block representation and main characteristics

The CMOS implementation is represented in the simplified schematics of fig. 2. This is a *modified version* of the *improved version* of the *conventional CCII version based on current mirrors*.
The improvement regards the parasitic input resistance in X (lower resistance). It was proposed in the work (2) with BJT technology and later revised in the work (3) with CMOS.
With respect to the improved version, we added cascode mosfets *Mpc* and *Mnc* in the *X* and *Z* branches. Moreover we optimized all mosfet sizes in order to optimize the coupling with the circuits used to inject the threshold currents.

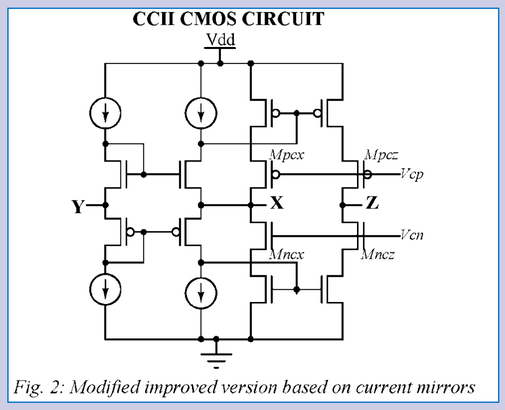


Fig. 2: Modified improved version based on current mirrors

THE CHANNEL AND THE INTERFACE AND CONFIGURATION MODULE

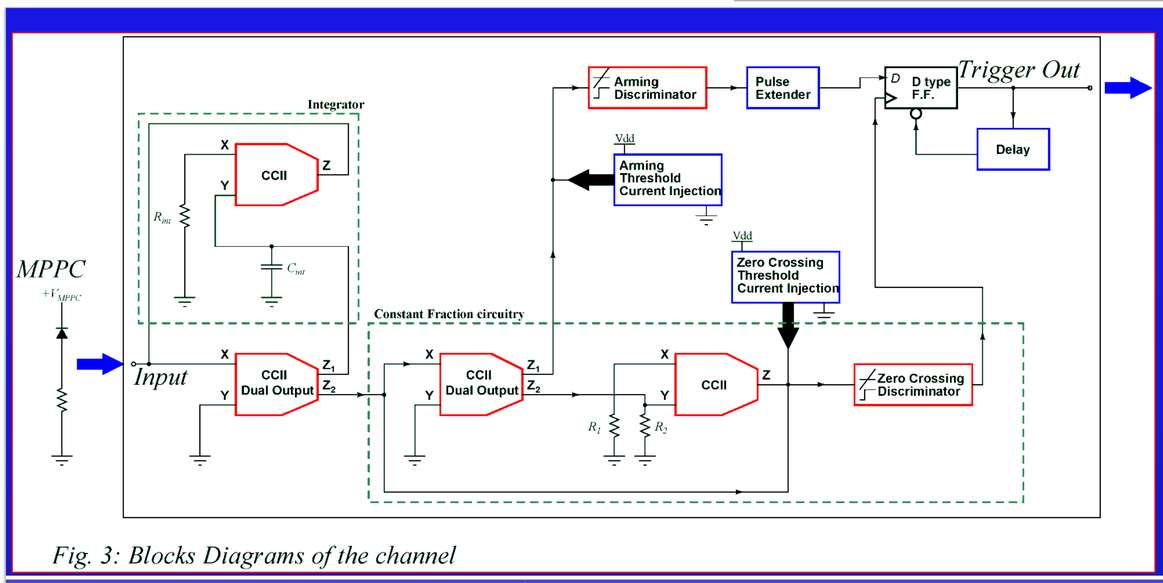


Fig. 3: Blocks Diagrams of the channel

The MPPC sensor is connected to the low impedance input *X* of the first dual-output CCII stage used as current buffer. The CCII on top performs a current integration: it acts as a low-pass filter with current feedback, reducing the pile-up effect in case of high input rate.

The two CCIIs on the right side and the zero crossing discriminator constitute the constant-fraction circuitry.

The *Pulse Extender* block regulates the time width of the arming gate for assuring the synchronization of the entire chain.
The *Delay* block determines the time width of the output signal.

The threshold currents as well as the time width of arming gate and of the pulse extender are programmable within a 10-bit dynamical range.

The discriminator is a low-power high-speed CMOS Current Comparator presented in (4).

Respect to the circuit proposed by the authors, we made only slight modifications regarding the size of some mosfets in order to optimize coupling with our CCII's output and to match the technology used.

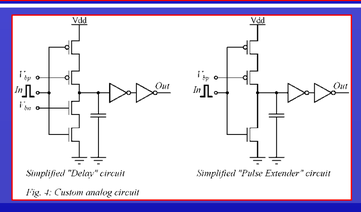


Fig. 4: Custom analog circuit

We also designed the *Pulse Extender* and the *Delay* blocks.
The simplified schematic is depicted in fig. 4.

A three-wire serial interface (Clock, Data, Latch) has been chosen to load threshold values, time widths and current polarization value for the CCIIs. This serial interface acts as SIPO (serial input-parallel output), by means of a shift-register.
The produced reference current flows in a master mosfet producing the voltage biasing.
The architecture of this fully programmable bias current generator is taken by the work presented in (5).
We have completely re-defined the sizes of the all mosfets since the currents we needed were remarkably bigger.

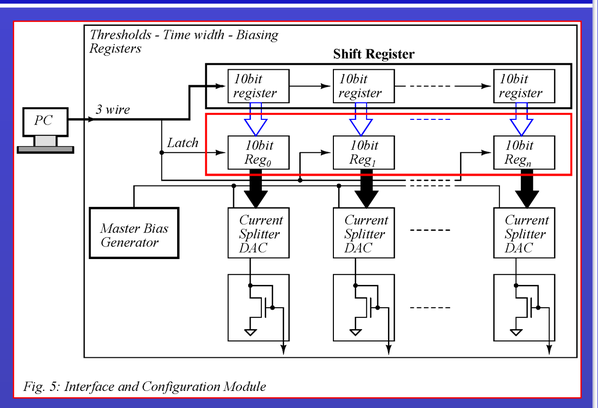
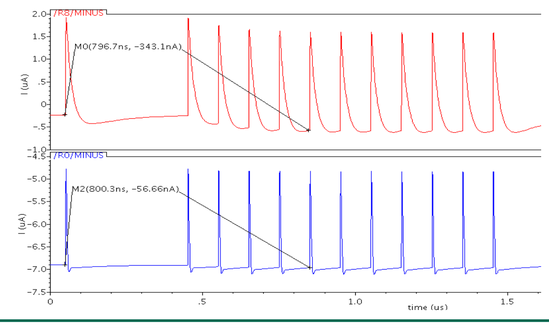
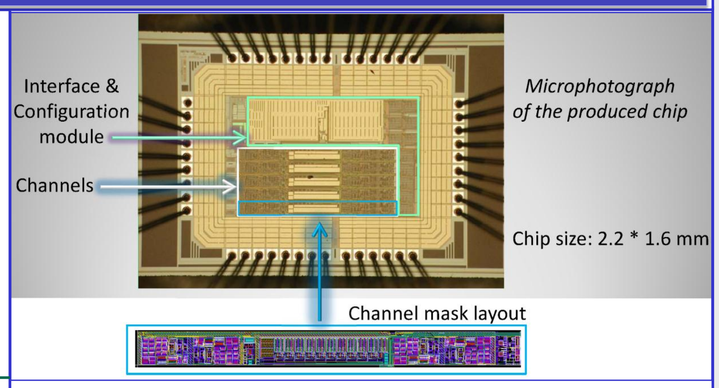


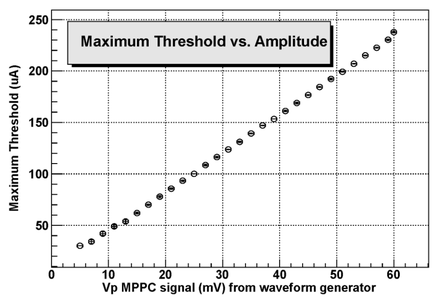
Fig. 5: Interface and Configuration Module

SIMULATION AND PRELIMINARY TEST RESULTS

The simulation results show the effect of the current feedback filter. A series of stimulus signals, equivalent to one photo-electron amplitude, are generated from a MPPC simulation model (6), (7). The signal flowing out from the first stage with feedback (bottom) reveals a strong reduction of the level shift caused by the high rate repetition events, with respect to the signal output of the same stage without this feature (top).

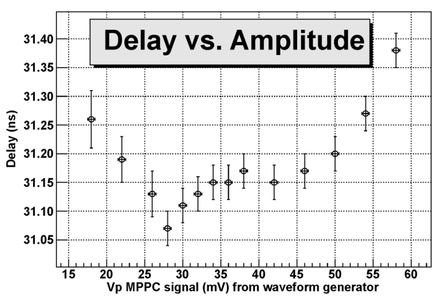




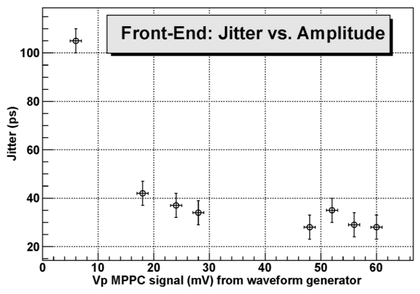


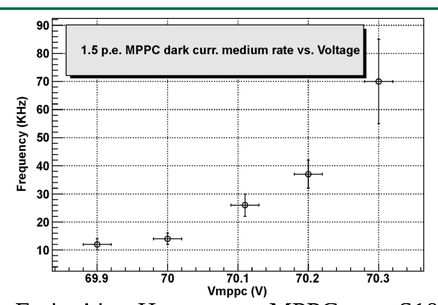
A waveform generator was used to produce a signal similar to a typical MPPC signal. The peak value for 1 p.e. corresponds roughly to 1 mV on the Front-End input. The graph shows a very good **linearity** between the value of the arming threshold and the peak value of the incoming signal.

Time-walk is contained within 200 ps in a large range of signal amplitude.



The measured **Jitter** of the bare front-end as function of the value of the peak value of the signal





The Front-End with a Hamamatsu MPPC type S10362-11-050C has been used to measure the **dark current** rate as a function of the operating voltage of the MPPC. The arming threshold was adjusted to 1.5 p.e. The measured value, at the nominal operating voltage (69.9 V), matches perfectly the declared value of 12.1 KHz of the used sample.

CONCLUSIONS

We have designed and produced a cmos front-end for MPPC device aimed to TOF applications. The current amplification chain is based on current conveyors adapted for the specific purpose and used as building blocks. This makes easy to realize future improvements and changes. The prototype chip consists of five channels with independent adjustable thresholds and with main biasing circuitry on chip. Preliminary tests show satisfactory performance in terms of dynamic range, threshold adjustment, and timing resolution.

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