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Performance and Upgrade Plans of the LHCb Trigger System

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The LHCb High Level Trigger (HLT) is implemented in a farm of parallel-processing CPUs, and serves to reduce the event rate from an input of 1 MHz to an output rate of around 2 kHz, with a processing time of around 20 ms per event. In order to maximize efficiencies and minimize biases, the trigger is designed around highly inclusive selection algorithms, culminating in a novel boosted decision tree which enables the efficient selection of heavy flavour deca
ys based on a robust partial reconstruction of their decay products. The major bottleneck in LHCb's trigger efficiencies is the hardware trigger which reduces the event rate to the 1MHz detector readout speed. In order to improve performance, the LHCb upgrade aims to significantly increase the speed at which the detector will be read out. As a consequence, the HLT will have to process more than 10MHz of events. We demonstrate that the current HLT architecture will be able to meet this challenge, particularly in the context of running stability and long term reproducibility of the HLT decisions which are crucial to the programme of precision physics measurements for which the LHCb upgrade is being built. We also discuss the expected efficiencies and signal yields per unit luminosity in several key channels for the LHCb upgrade.

for the collaboration

LHCb

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