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Development of the DEPFET Sensor with Signal Compression: a Large Format X-ray Imager with Mega-Frame Readout Capability for the European XFEL

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We present the development of the DSSC: an ultra-high speed detector system for the European XFEL in Hamburg. The DSSC will be able to record X-ray images with a maximum frame rate of 4.5MHz. The system is based on a silicon pixel sensor with a new non-linear DEPFET as a central amplifier structure and has detection efficiency close to 100% for X-rays from 0.5 keV up to 10keV. The sensor will have a size of 210x210 mm^2 composed of 1024x1024 pixels. 256 readout ASICs are bump-bonded to the detector in order to provide full parallel readout. The signals coming from the sensor are processed by an analog filter, digitized by 8-bit ADCs and locally stored in a SRAM. In order to fit the dynamic range of 10^4 photons of 1keV per pixel into a reasonable output signal range, achieving simultaneously single 1keV photon resolution, a strongly non-linear characteristic is required. The proposed DEPFET provides dynamic range compression at the sensor level. The most challenging property is that the single 1keV photon resolution and the high dynamic range are accomplished within the 220ns frame rate. The main building blocks and properties of the system will be discussed. The experimental characterization of first non-linear DEPFET will be presented. New experimental results obtained coupling this newly fabricated DEPFET prototype to an ASIC prototype which comprises the complete readout chain from the analog front-end to the ADC and the memory will be shown.

Optional extended abstract

We present the development of the DSSC system [1]. The aim of this development is to deliver a high speed focal plane detector system, together with the related readout electronics for the new European XFEL in Hamburg [2]. This machine will generate, 27 000 times per second, ultrashort X-ray flashes with a brilliance that is a billion times higher than that of the best conventional X-ray radiation sources. The ultra-short X-ray pulses will not be uniformly distributed in time, but will be concentrated in a time window of about 600µs, followed by a gap of 99.4ms. This means that the flashes will have a temporal distance of 220ns. Therefore the DSSC instrument must be able to record X-ray images with a maximum frame rate of 4.5MHz. In addition it has to achieve a high dynamic range. The concept is based on a silicon pixel sensor with a new non-linear DEPFET [3] as a central amplifier structure. The sensor will have the following key properties: the total size will be approximately 210 × 210 mm^2 composed of 1024 × 1024 pixels with hexagonal shape. The pixel array will be subdivided into 16 ladders with 128 × 512 pixels each. The ladders will be geometrically arranged such that a central hole is left to let the unscattered photons go through. Every detector ladder is bump-bonded to mixed signal readout ASICs. The ASICs are designed in 130nm CMOS technology and provide full parallel readout of the DEPFET pixels. The parallel readout is mandatory in order to cope with the high repetition rate of the XFEL machine. Therefore a separate readout channel is required for each pixel. The signals coming from the individual pixels of the detector are processed by an analog filter, immediately digitized by a series of 8-bit ADCs (9-bit at half of the maximum speed) and locally stored in a custom designed SRAM also integrated in the ASICs. During the 99.4ms time gap of cooling phase of the accelerator, the digital data are sent off the focal plane to a data acquisition electronics that acts as an interface to the back-end of the whole instrument. Our aim is to supply a high speed focal plane camera with high spatial resolution for X-rays from 0.5 keV up to 10 keV with close to 100 % detection efficiency. The dynamic range is designed to be about 10^4 photons of 1 keV per pixel, with an analog compression on the sensor level. The most exciting and challenging property is the 220 ns frame rate of the system. This goes beyond all existing instruments and requires the development of new concepts and technologies. In a first attempt we aim for the local storage of about 700 frames per macro bunch either consecutive or externally triggered.

The pixel sensor has been designed so as to combine high energy resolution at low signal charge with high dynamic range. This has been motivated by the desire to be able to be sensitive to single low energy photons and at the same time to measure at other positions of the detector signals corresponding to up to 10^4 photons of 1keV. In order to fit this dynamic range into a reasonable output signal range, achieving at the same time single photon resolution, a strongly non-linear characteristic is required. The new proposed type of DEPFET [4] provides this non-linear output characteristic. Therefore it implements the required dynamic range compression at the sensor level, considerably facilitating the task of the electronics. In this way the new DEPFET solves the challenge of providing excellent charge resolution for low signals, as required for single photon detection, with very large charge handling capacity for pixels containing the overlap of very many photons.

As the standard DEPFETs, the DSSC-DEPFET collects the signal charge generated by the incoming radiation in an "internal gate"located below the conductive channel. This stored charge modulates the current of the transistor which turns out to be a function of the incident radiation. The peculiarity of the DSSC-DEPFET is that the internal gate extends into the region below the large-area source. Small signal charges assemble below the channel only, being fully effective in steering the transistor current. Large signal charges will spill over into the region below the source and correspondingly be less effective in steering the transistor current.

According to our knowledge the DSSC will be the first instrument able to provide a single photon detection capability in the low energy range at the speed of 4.5 MHz. The high repetition rate foreseen for XFEL requires parallel readout of all pixels. For this reason a separate readout channel is required for each pixel and all pixels have to be powered during the pulse train.

During the talk the key properties, the design and the functionalities of the main building blocks of the system will be discussed. These include the sensor design and simulations, the readout ASIC and the electro-mechanical constructions.

The experimental results on a first front-end prototype ASIC coupled to a standard DEPFET have already proven [5,6] that it is possible to achieve the targeted single photon resolution for 1keV photons at 4.5 MHz and also for 0.5 keV photons, in case the operating speed is reduced of a factor two. In fact noise values of about 13 electrons r.m.s. with a readout speed of 1 MHz and about 45 electrons at 5MHz have been obtained.

The experimental measurement of the non-linear characteristic on a newly produced DSSC-DEPFET prototype will be presented and the layout of the full-format sensor will be shown.

In addition the very first measurements of DSSC-DEPFET coupled to an 8x8 mini-ASIC will be shown. This mini-ASIC comprises the complete readout chain from the analog front-end to the ADC and the memory.

References
[1] M. Porro et al., Nucl. Instr. And Meth. A, vol. 624, Issue 2, pp. 509-519, December 2010; [2] http://www.xfel.eu; [3] J. Kemmer and G.Lutz, Nucl. Instr. And Meth. A, vol. 253, pp. 365-377, 1987; [4] G. Lutz et al., Nucl. Instr. And Meth. A, vol. 624, Issue 2, pp. 528-532, December 2010; [5] G. De Vita et al., "A 5MHz Low-Noise 130nm CMOS Analog Front-End Electronics for the Readout of Non-Linear DEPFET Sensor with Signal Compression for the European XFEL", IEEE NSS Conference Record, Knoxville 2010; [6] S. Facchinetti et al. "Characterization of the Flip-capacitor filter for the XFEL project", accepted for pubblication in Nucl. Instr. And Meth. A.

for the collaboration

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