Contribution ID: **177** Type: **Poster**

Analog Front-end Electronics for the Outer Layers of the SuperB SVT: Design and Expected Performances

Wednesday, 23 May 2012 11:26 (0 minutes)

The Silicon Vertex Tracker (SVT) of the new SuperB collider will be composed of 6 different detector layers. The inner most layer (layer 0) will be composed by striplets or pixels; the other 5 detector layers will be double-sided strip detectors. The strip geometries and the foreseen hit-rates will change according the different layers. As a consequence, different optimization of the analog read-out electronics are needed in order to provide high detection-efficiency and low noise level in the different layers. Two readout ASICs are currently developed, one for layers 0-3, another for layers 4,5; they differ mainly in the analog front-end.
In this work, we present the design and expected performances of the analog front-end for layers 4 and 5. For these layers, the microstrip detectors show a very high stray capacitance and high series resistance. In this condition, the noise optimization is our primary concern. A necessary compromise on the best peaking time to achieve an acceptable noise level together with efficiency and time accuracy has been found. We will present the design of preamplifier and shaper and the results of simulation of noise performance and efficiency (with the expected background rates). In addition, the design of the Time-over-threshold (TOT) and its use to correct the time-walk of the event trigger is discussed as well as the achievable timing accuracy of the circuit.

for the collaboration

on behalf of the SVT-SuperB Group

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Session Classification: Front End, Trigger, DAQ and Data Management - Poster Session

Track Classification: P4 - Front End, Trigger, DAQ and Data Management