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A Fast Readout Algorithm for Cluster Counting/Timing Drift Chambers on a FPGA Board

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A fast readout algorithm for Cluster Counting and Timing purposes has been implemented and tested on a Virtex 6 core FPGA board. The algorithm analyzes and stores data coming from Helium based drift tube instrumented with a 1 GSa/s ADC and represents the outcome of balancing between efficiency and high speed performance, resulting in high efficiency peak data extraction on simulated signals as well as on experimental ones.
A relative efficiency evaluation with respect to commercial sophisticated peak finding software (i.e. PeakFit) will be reported.
Based on these results, the developed algorithm could be adopted in order to build an electronics VME board serving multiple fADC channels and be used as an on-line preprocessing stage for signals coming from drift chambers making use of Cluster Counting/Timing techniques.

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