The electronics for the FDIRC can be seen as an upgrade of the electronics of the BABAR DIRC. The new high luminosity-driven requirements of the experiment (trigger rate, background, radiation environment) and FDIRC specific requirements (resolution, number of channels and topology) have led to a new design of the electronics chain associated with a new design of its mechanical support. The electronics for the barrel will equip the 12,432 channels of the 12 sectors of the FDIRC.

The electronics chain is based on:
- a high resolution low count rate TDC (SCATS chip),
- charge measurement over 5 bits (iPF chip),
- event data packing sending data frames to data acquisition system (DAQ).

The requirements for the complete electronics chain are:
- a time resolution of 100 ps rms.
- a count rate capability of 500 KHz per channel (background-driven).
- trigger rate up to 250 KHz.
- a minimum distance between triggers of about 50 ns.

**Electronics design**

The mother board is a long blade PCB which integrates 6 HVM8R16M 8 Megbits/64bits flash memory on the FFE boards, a single PMT mother board prototype was designed to test connectivity and performances.

The FFE boards are based on 4-channel processing boards. Each board includes:
- 5 SCATS TDCs
- 5 ADCs
- 1 ACTEL FPGA
- 1 AD9759 DAC

Upon reception of the L1 trigger command, the FFE board copies the selected events in the deadtime, formats data and pack the events.

**ASICS design**

The first version of SCATS TDC will embed both analog and TDC blocks. For this reason, each part is developed separately for test purpose. Both parts will be assembled in the final version end of 2013.

The SAMLONG chip has been designed in AMS 0.35 μm technology. It delivers 16 channels covered by 8 SAMLONG chips and equipped with 8192 photoelectrons of 1.25 kloppm resolution. Each channel can be readout by two FFE boards. In horizontal direction, the resolution is reduced by connecting 2 adjacent pixels to get 16 channels per PMT.

A 16-channel waveform digitizer has been designed [2]. It houses 8 SAMLONG chips and many possibilities of triggering. The board can be readout by USB or via a dedicated backplane for high scale implementations. The sampling time precision remains below 10 ps rms.

**SuperB FDIRC**

SuperB forward region is not covered by the FDIRC. A dedicated detector would improve the PID coverage.

**SuperB PID group**

SuperB FDIRC, successor of the BABAR DIRC, a focusing detector of Internally Reflected Cherenkov light (FDIRC) will be used for low energy hadronic jets. The SAMLONG ultra-fast analog memory (commonly developed by LAL, Orsay and CEAM/Tuscanie AMS 0.35 μm) will allow a time precision as good as 10 ps rms noise. Sampling time precision is extracted via digital Constant Fraction Discrimination (CFD) performed by the software.

**FDIRC**

FDIRC (Focusing Detector of Internally Reflected Cherenkov light) and FTOF (Forward Time of Flight)