PID electronics for SuperB

FDIRC (Focusing Detector of Internally Reflected Cherenkov light) and FTOF (Forward Time of Flight)

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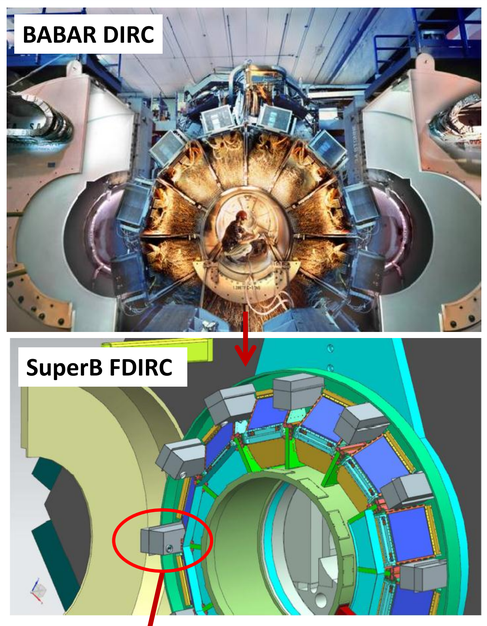
FDIRC

SuperB FDIRC: successor of the BABAR DIRC, a new photon camera to cover the SuperB barrel PID region (**see dedicated talk**).

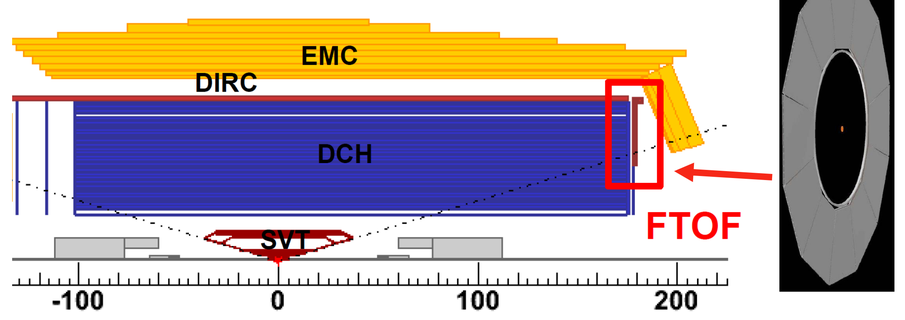
The electronics for the FDIRC can be seen as an upgrade of the electronics of the BABAR DIRC. The new high luminosity-driven requirements of the experiment (Trigger rate, background, radiation environment) and FDIRC specific requirements (resolution, number of channels and topology) have led to a new design of the electronics chain associated with a new design of its mechanical support. The electronics for the barrel will equip the 18,432 channels of the 12 sectors of the FDIRC.

The electronics chain is based on:
- high resolution/ high count rate TDC (SCATS chip),
- charge measurement over 10 bits (PIF chip)
- event data packing sending data frames to data acquisition system (DAQ)

The requirements for the complete electronics chain are:
- a time resolution of 100 ps rms
- a count rate capability of 500 KHz per channel (background-driven)
- a trigger rate up to 150 KHz
- a minimum distance between triggers of about 50 ns.



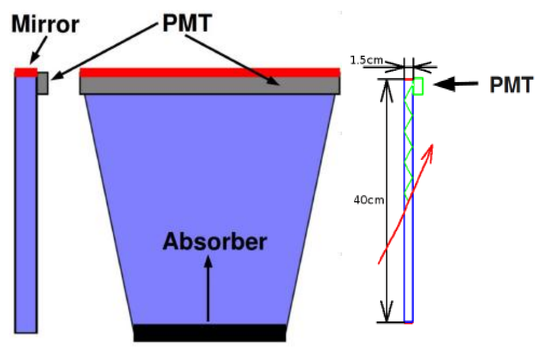
FTOF



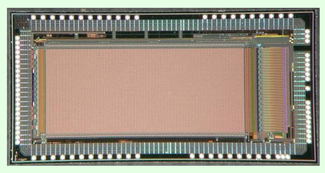
SuperB forward region is not covered by the FDIRC. A dedicated detector would improve the PID coverage =>

Forward Time-Of-Flight

(**see dedicated poster**)
- 12 thin quartz tiles equipped with fast **MCPPMTs** to read the Cherenkov photons
- 56 channels per tile
- Flight path 2m => 30ps total accuracy needed to separate π/K => ultra-fast electronics is required (resolution as good as **10 ps rms**).

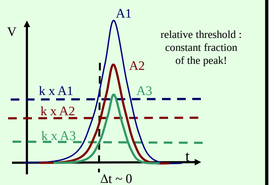


- A prototype of the FTOF has been tested in the SLAC cosmic ray telescope in 2010 [1]. Electronics was a custom crate filled with 16 2-channel **WaveCatcher** boards running with common 200MHz clock and trigger. These boards are **12-bit 3.2 GS/s low power and low cost waveform digitizers** based on the **SAMLONG ultra-fast analog memory** commonly developped by LAL Orsay and CEA/Irfu Saclay (AMS CMOS 0.35 µm). Sampling time precision is a good as 10 ps rms at the crate level. Photon arrival time is extracted via digital Constant Fraction Discrimination (CFD) performed by the software.



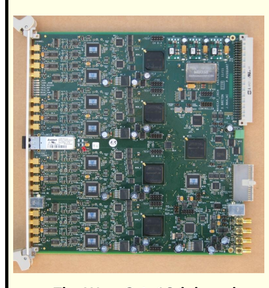
The SAMLONG analog memory

Zoom on the 16-channel crate

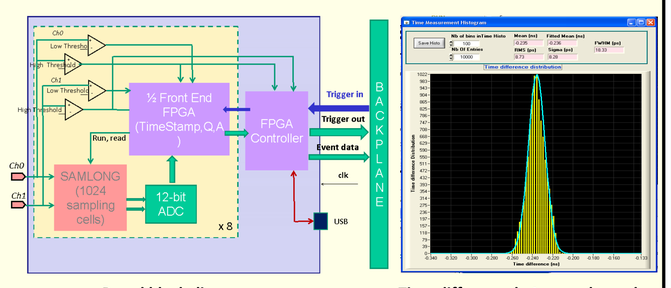


The digital CFD method

- A **new 16-channel waveform digitizer board** has been designed [2]: it houses 8 SAMLONG chips and many possibilities of triggering. The board can be readout by USB or via a dedicated backplane for high scale implementations. The sampling time precision remains below 10 ps rms.



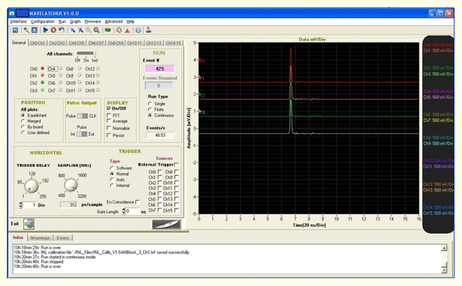
The WaveCat_16ch board



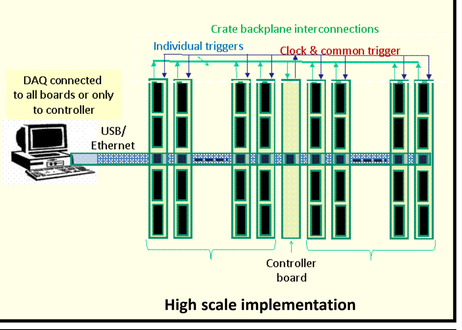
Board block diagram

Time difference between channels

- 4 Wavecat_16ch boards driven by a controller board (USB/Ethernet) will be used in a synchronous way for the **test of a full size FTOF sector prototype** (56 channels) in the near future.

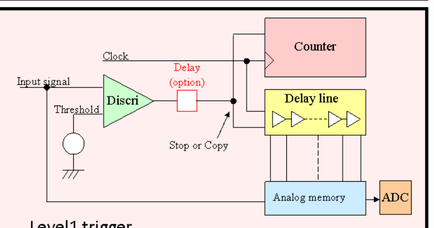


The WaveCat_16ch acquisition software

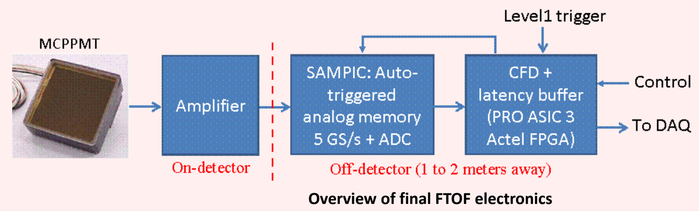


High scale implementation

- The **final electronics for the FTOF** will be highly integrated and based on a **new principle of TDC, called SAMPIC**. The latter, designed in AMS CMOS 0.18µm technology, will be able to tag the arrival time of 16 **analog** signals with a **precision of a few ps** thanks to its **embedded analog memory** (running between 5 and 10 GS/s) and its embedded ADC.



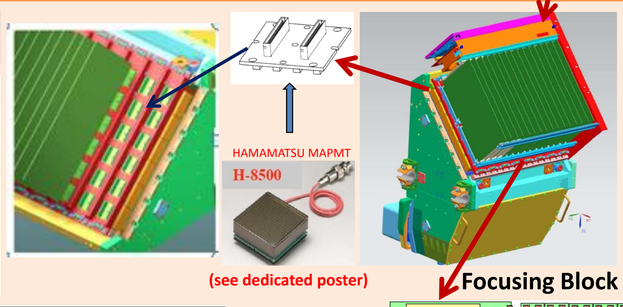
SAMPIC TDC



Overview of final FTOF electronics

Electronics design

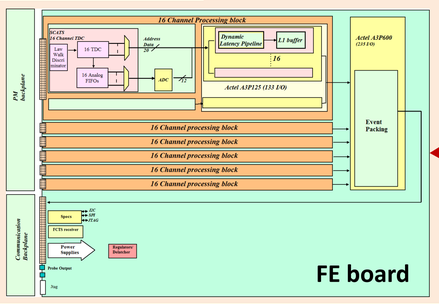
The motherboard is a long blade PCB which interconnects 6 HM8500 MaPMTs to the FE boards. A single PMT motherboard prototype was designed to test connectivity and performances.

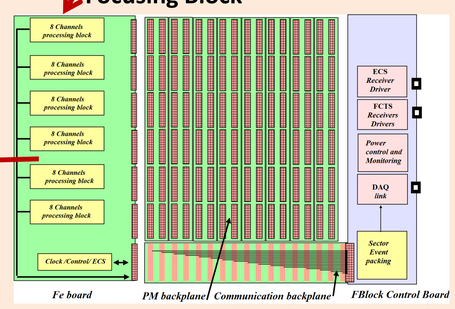


(see dedicated poster)

PMTs are arranged as a matrix of 6 in vertical x 8 in horizontal direction. Each column of 6 PMTs will be readout by two FE boards. In horizontal direction, the resolution is reduced by connecting 2 adjacent pixels to get 32 channels per PMT.

Focusing Block





Focusing Block electronics

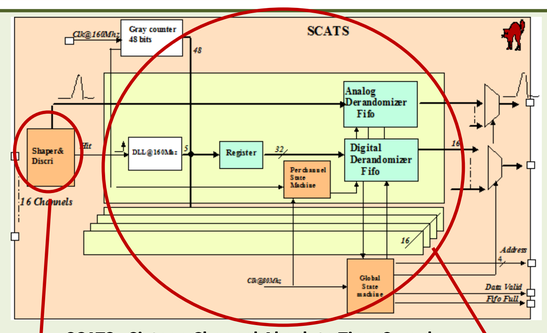
The FE board is based on 6-channel processing blocks. Each block includes:
- 1 SCATS TDC
- 1 ADC
- 1 ACTEL FPGA
- glue logic.

Upon reception of the L1 trigger command, the FE board copies the selected events in the derandomizer, formats data and packs the events.

The FBlock houses:
- 16 FE boards
- 1 Focusing Block control board
- 6 motherboards
- 1 communication backplane
- Fan trays

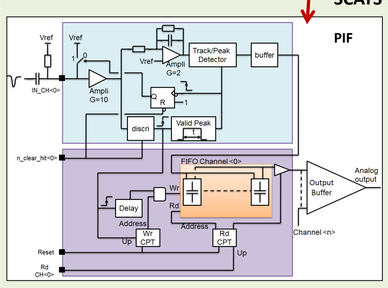
ASICs design

The final version of SCATS will embed both analog and TDC blocks.
In a first step, each part is developed separately for test purpose.
Both parts will be assembled in the final version end of 2013.

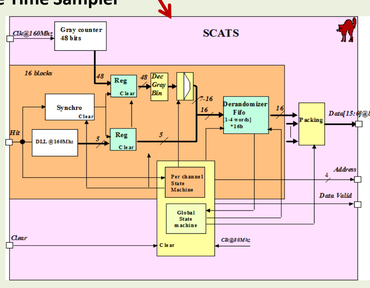


SCATS : Sixteen Channel Absolute Time Sampler

We have designed the first prototype of the SCATS TDC. The chip main requirements are:
- 200ps step & 100ps rms resolution
- data-push architecture
- dead time ~ 1% with 500kHz input rate on each channel.
- Rad-tolerance (immunity to SEUs & SELs)



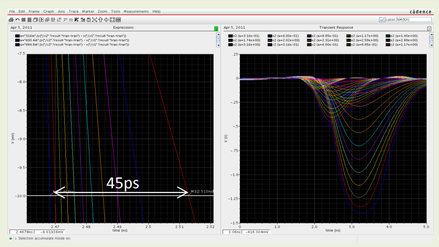
Architecture, designed for single photoelectron detection, is based on the association of a low-walk (< 70ps) discriminator and a charge amplifier



Architecture is based on the association of a time measurement part synchronized @ 160 MHz and a data-push readout part designed to merge the 16 channels into a 16-bit parallel bus at a rate of 80 MHz.

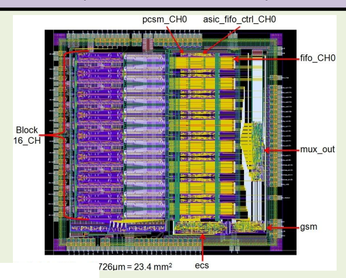
- Charge measurement is performed by an integration with:
  - a dynamic range of 15 over 10 bits
- value is stored in a analog memory which is read:
  - independently during 1rst prototype phase
  - synchronously with time measurement in final version
- Low-walk discrimination is performed with a CFD-like architecture with a minimum threshold of - 2mV

- Data from the DLLs and the coarse counters is transferred into the FIFO memory within two clock cycles thus introducing a dead time limited to 25ns.
- The readout makes use of an individual FIFO memory per channel in order to derandomize the high frequency input bursts up to 500kHz per channel with only 1% dead time.



Discri simulation results: max walk = 45 ps for a dynamics of 10.

- First prototype has just been delivered
- On-board chip characterization will start within the next weeks.



SCATS: AMS CMOS 0.35µm - 4950µm*4726µm = 23.4 mm²

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• References:[1] D.Breton & al, Nuclear Instruments and Methods in Physics Research A 629 (2011) 123–132, "High resolution photon timing with MCP-PMTs: A comparison of a commercial constant fraction discriminator (CFD) with the ASIC-based waveform digitizers TARGET and WaveCatcher »
• [2] D.Breton & al, http://dx.doi.org/10.1016/j.nima.2011.12.007, « Using ultra fast analog memories for fast photo-detector readout »