Contribution ID: **228** Type: **Oral**

Recent developments on CMOS MAPS for the SuperB Silicon Vertex Tracker

Thursday, 24 May 2012 12:40 (20 minutes)

In the design of the Silicon Vertex Tracker for the high luminosity SuperB collider, very challenging requirements are set by physics and background conditions on its innermost Layer0: small radius (about 1.5 cm), resolution of 10-15 μm in both coordinates, low material budget <1% X_0, and the ability to withstand a background hit rate of several tens of MHz/cm^2.
Thanks to an intense R&D program the development of Deep NWell CMOS MAPS (with the ST Microelectronics 130 nm process) has reached a good level of maturity and allowed for the first time the implementation of thin CMOS sensors with similar functionalities as in hybrid pixels, such as pixel-level sparsification and fast time stamping.
Further MAPS performance improvements are currently under investigation with two different approaches: the INMAPS CMOS process, featuring a quadruple well and an high resistivity substrate, and 3D CMOS MAPS, realized with vertical integration technology.
In both cases specific features of the processes chosen can improve charge collection efficiency, with respect to a standard DNW MAPS design, and allow to implement a more complex in-pixel logic in order to develop a faster readout architecture.
Prototypes of MAPS matrix, suitable for application in the SuperB Layer0, have been realized with the INMAPS 180 nm process and the 130 nm Chartered/Tezzaron 3D process and results of their characterization will be presented in this paper.

Optional extended abstract

In the design of the Silicon Vertex Tracker for the high luminosity SuperB collider, very challenging requirements are set by physics and background conditions on its innermost Layer0: small radius (about 1.5 cm), resolution of 10-15 um in both coordinates, low material budget <1% X0, and the ability to withstand a background hit rate of several tens of MHz/cm2.
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Further performance improvements are currently under investigation with two different approaches: the INMAPS CMOS process, featuring a quadruple well, and 3D CMOS MAPS, realized with vertical integration technology.
A limiting factor for the DNW MAPS is the presence of competitive N-Wells in the pixel-cell that can subtract charge to the DNW sensor.
The use of the INMAPS process, with a deep P-well implant deposited beneath the competitive N-Wells, can reduce their negative effect and improve charge collection efficiency. Moreover with the use of an high resistivity substrate, radiation resistance of these devices is improved with respect to MAPS on a standard CMOS substrate.
In 3D MAPS with vertical integration the sensor and analog front-end are hosted in one CMOS tier, while the other is dedicated to the in-pixel digital front-end and the peripheral readout logic. With this splitting one

can improve the charge collection efficiency, reducing the N-Well competitve area in the sensor layer, and improve the readout performance, thanks to a more complex in-pixel logic.
Prototypes of MAPS matrix, suitable for application in the SuperB Layer0, have been realized with the IN-MAPS 180 nm process and the 130 nm Chartered/Tezzaron 3D process and results of their characterization will be presented in this paper.

for the collaboration

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Session Classification: Solid State Detectors

Track Classification: S5 - Solid State Detectors