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The Pixel Detector Readout ASIC for the Micro Vertex Detector of the PANDA Experiment

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The PANDA experiment at the future FAIR facility under construction near the GSI research center at Darmstadt, Germany, aims to the study of the antiproton-proton and antiproton-nucleus annihilation reactions.

The Micro Vertex Detector (MVD) is the innermost part of the experiment and will consist of silicon pixel and silicon strip detectors. Owing to the high track density (up to 11.4 MHz/cm^2) and the absence of an hardware trigger signal, an ASIC based custom solution for the electronic readout of the pixel detector has been chosen. The ASIC, named ToPiX, will provide the time position of each hit and a measure of the charge released with the Time over Threshold (ToT) technique.

A reduced scale prototype in a CMOS $0.13 \mu\text{m}$ technology has been designed and tested. The prototype includes four columns made of 128 pixel cells, four columns of 32 cells and and the end of column readout with a 32 cells deep FIFO for each double column. Each cell embeds a charge amplifier with constant current feedback capacitor discharge, a comparator with per cell adjustable threshold, 12-bits leading and trailing edge register for time and ToT measurement and an 8 bits bit configuration register. All the readout logic has been SEU-hardened by design using either Hamming encoding or triple redundancy.

The chip has been tested both electrically via a test pulse input and connected to a detector in a beam test. Radiation test for both TID and SEU tests have been performed.

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