Characterization of the first prototypes of Silicon Photomultipliers with bulk-integrated quench resistor fabricated at MPI semiconductor laboratory

12th Pisa Meeting on Advanced Detectors
Isola d'Elba, 2012

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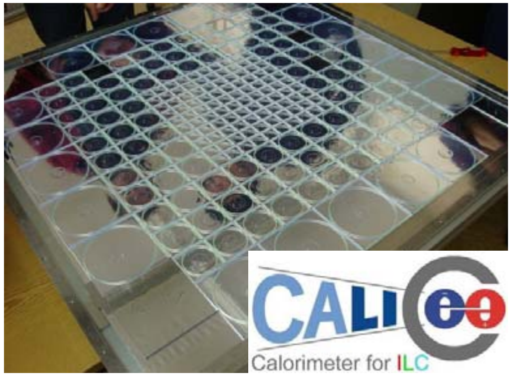
Outline

- motivation & introduction to silicon photomultipliers
- SiMPl concept: **S**ilicon **M**ulti**P**ixel **l**ight detector
- results of SiMPl characterization
- next SiMPl generation
- summary & outlook

Motivation for novel photon detectors

Low light level → High Detection Efficiency
Large detector area → low costs & power consumption

Large number of detectors → low costs & power consumption
Single tile readout → compact devices



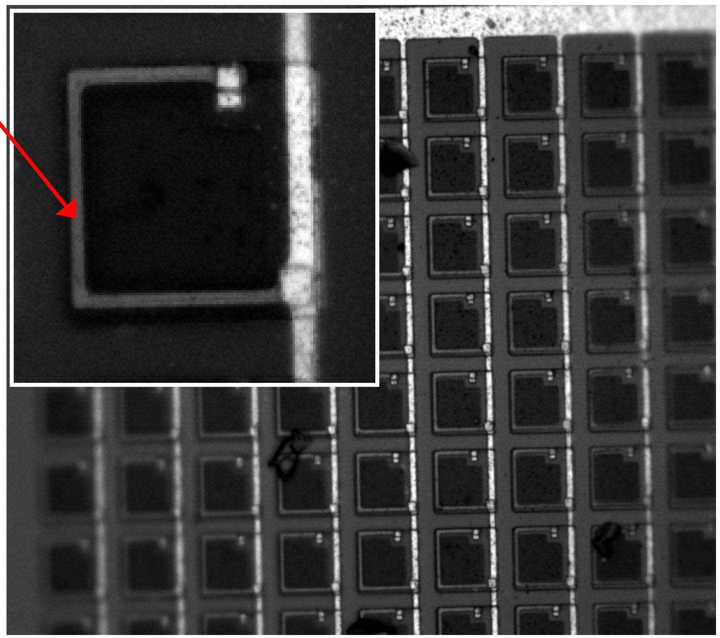
Other requirements:
fast timing & insensitivity to magnetic fields

Silicon Photomultiplier promising candidate

Conventional Silicon Photomultiplier – SiPM

- an array of avalanche photodiodes
  - operated in Geiger mode
  - passive quenching by integrated resistor
  - read out in parallel → signal is sum of all fired cells

polysilicon



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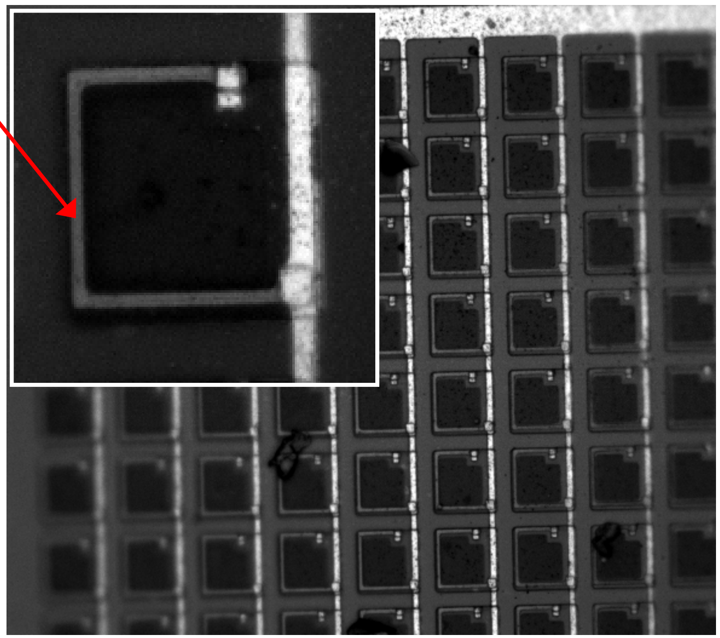

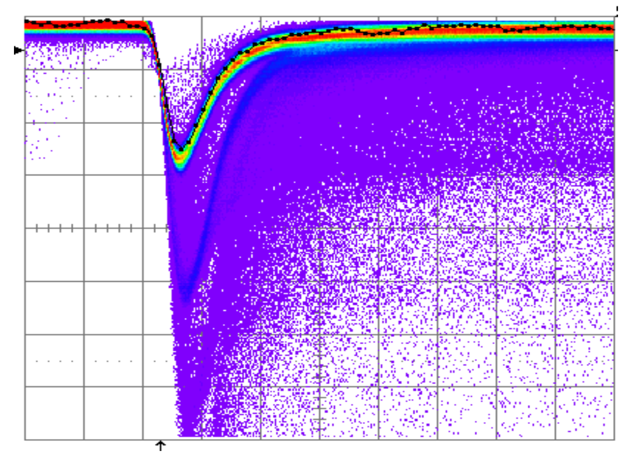

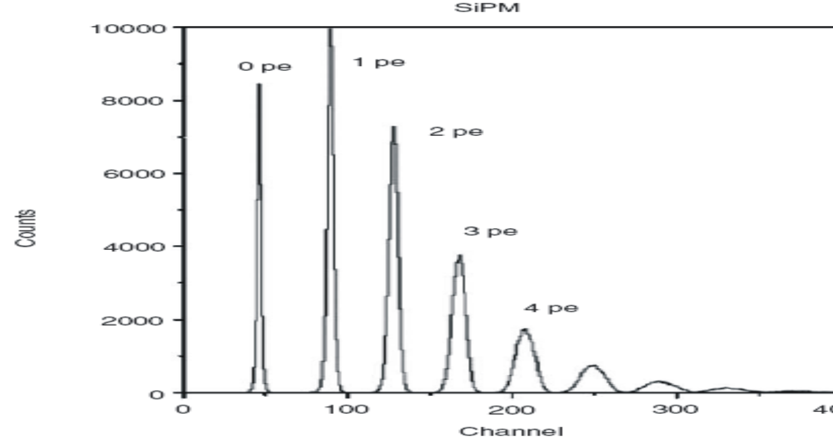

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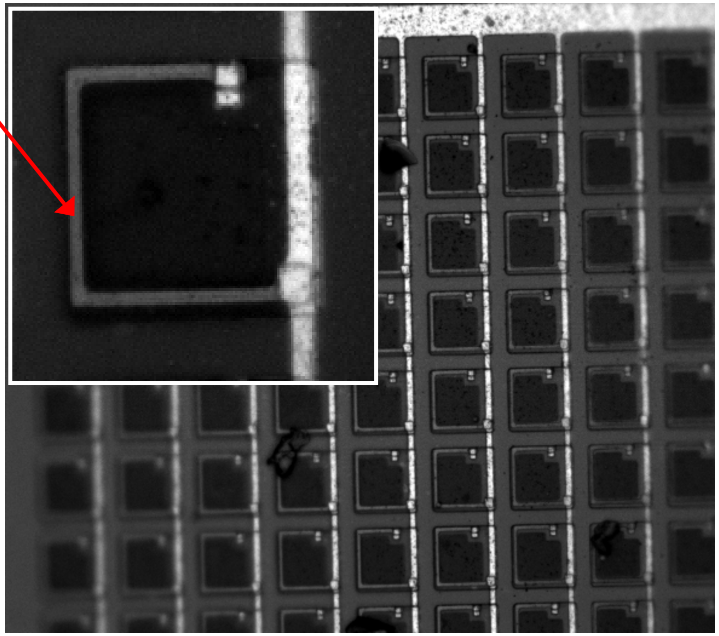
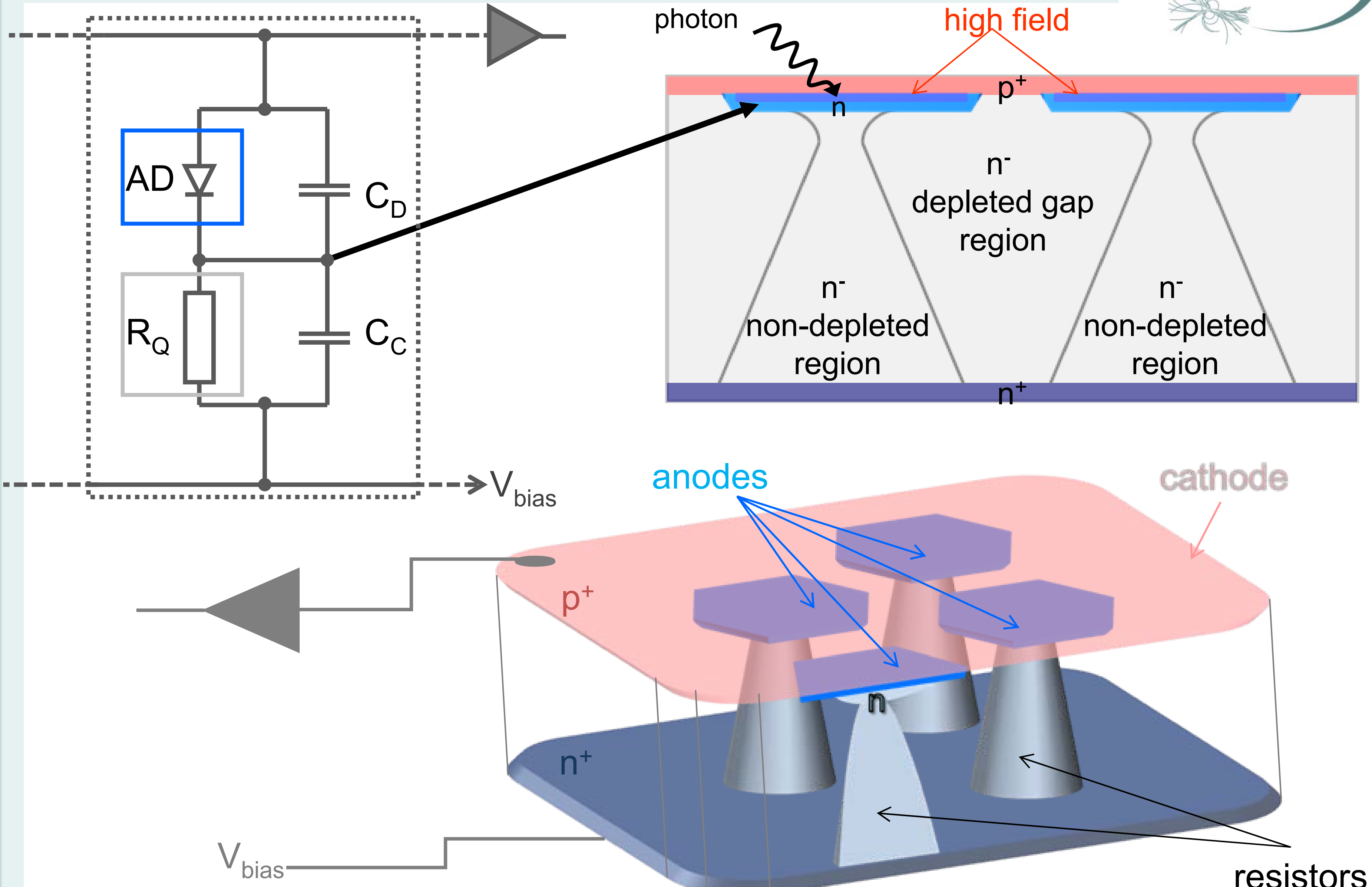


polysilicon resistor:

→ obstacle for light

→ limitation of PDE

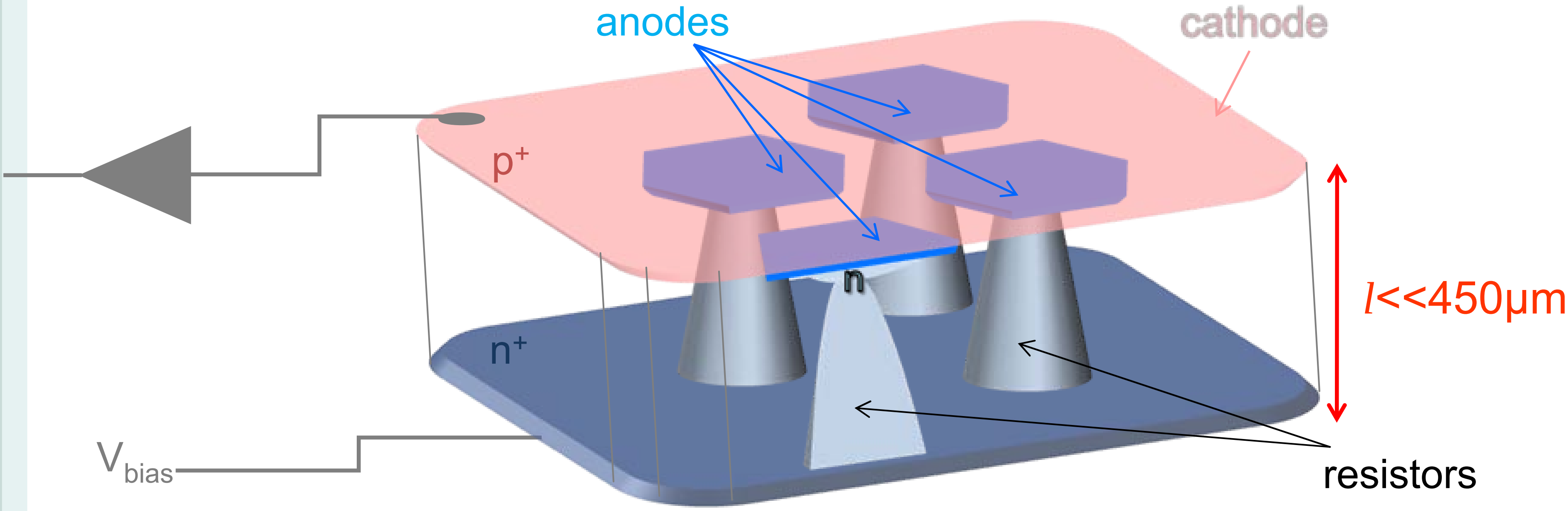
SiPM cell components → SiMPI approach



SiPM cell components → SiMPI approach

Resistor matching
requires thin wafers !

→ wafer bonding

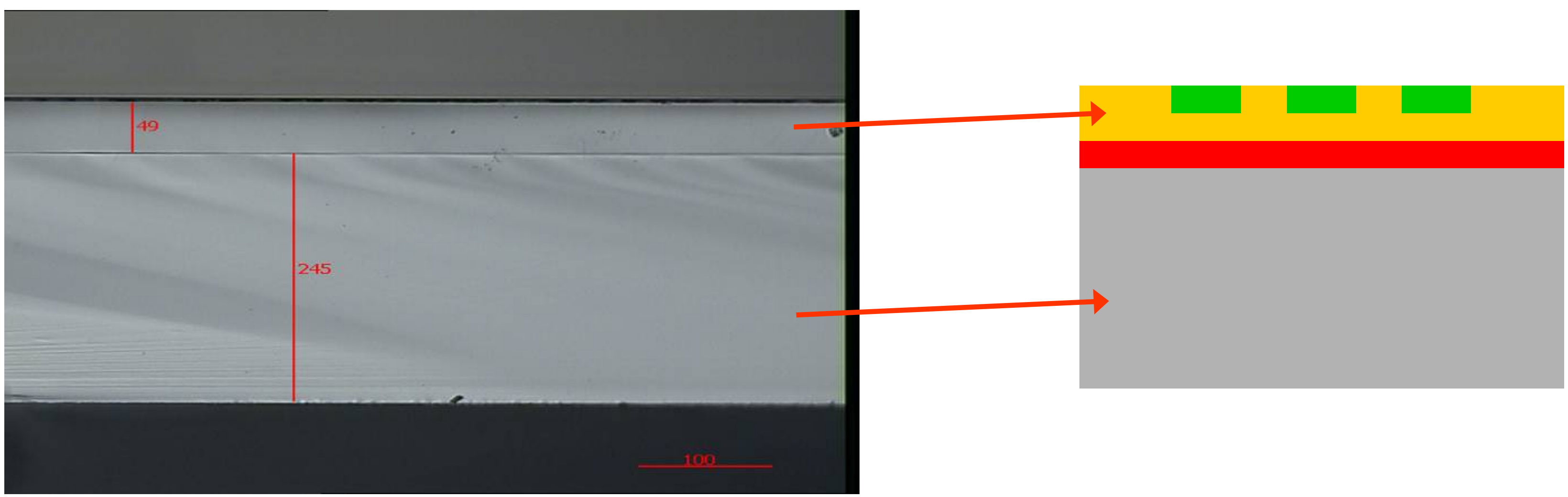


$$R = \rho \frac{l}{A}$$

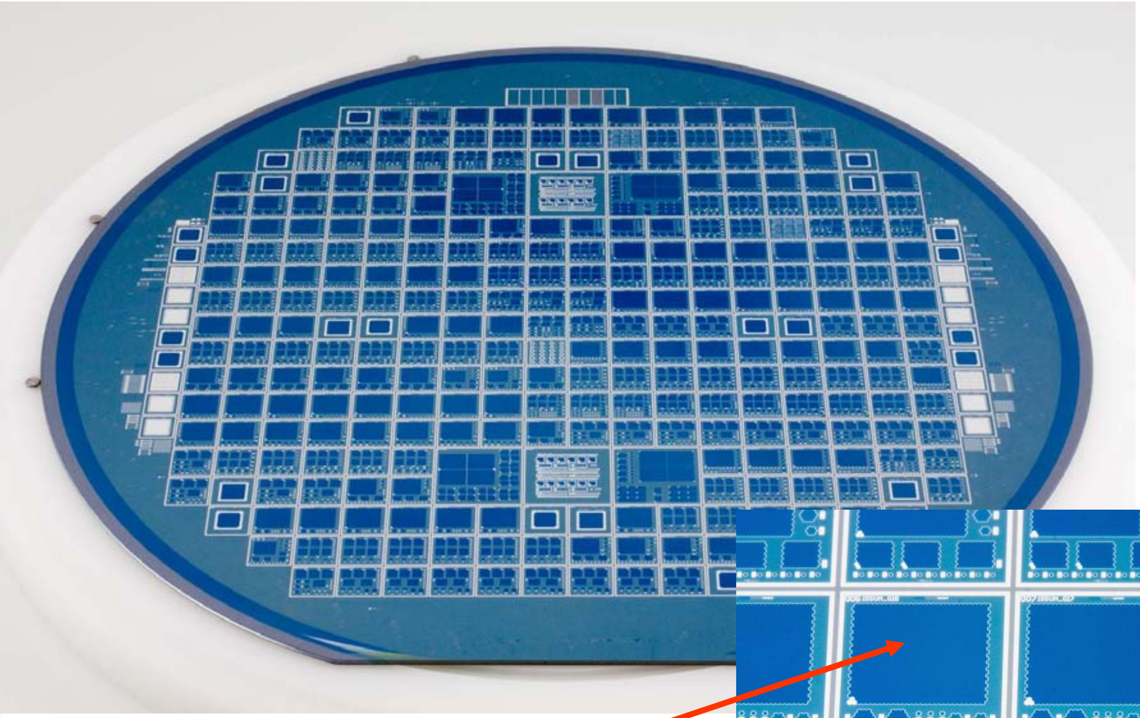
Wafer bonding – Silicon On Insulator wafers

1. implant backside on sensor wafer
2. bond sensor wafer to handle wafer
3. thin sensor side to desired thickness
4. fabricate SiMPI arrays on top side

Industrial partners → MPI HLL



SiMPI prototype

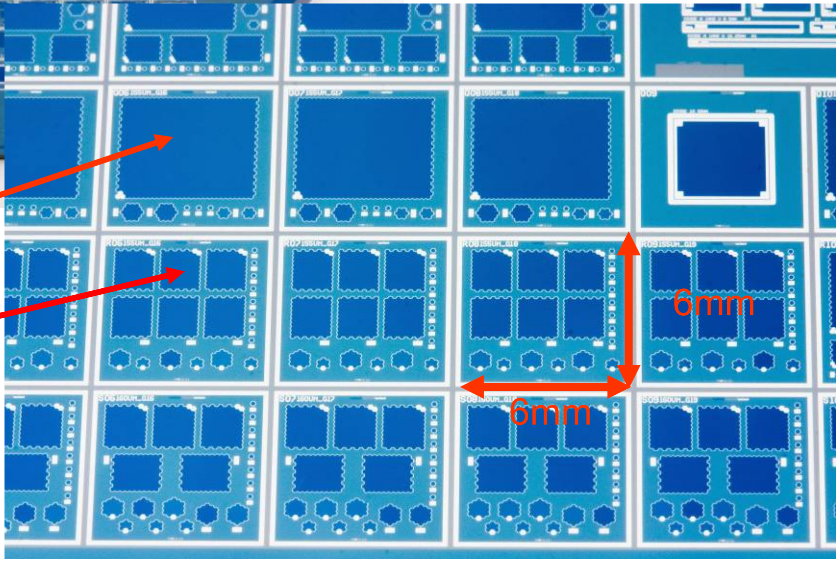


Wide range of
geometrical variations

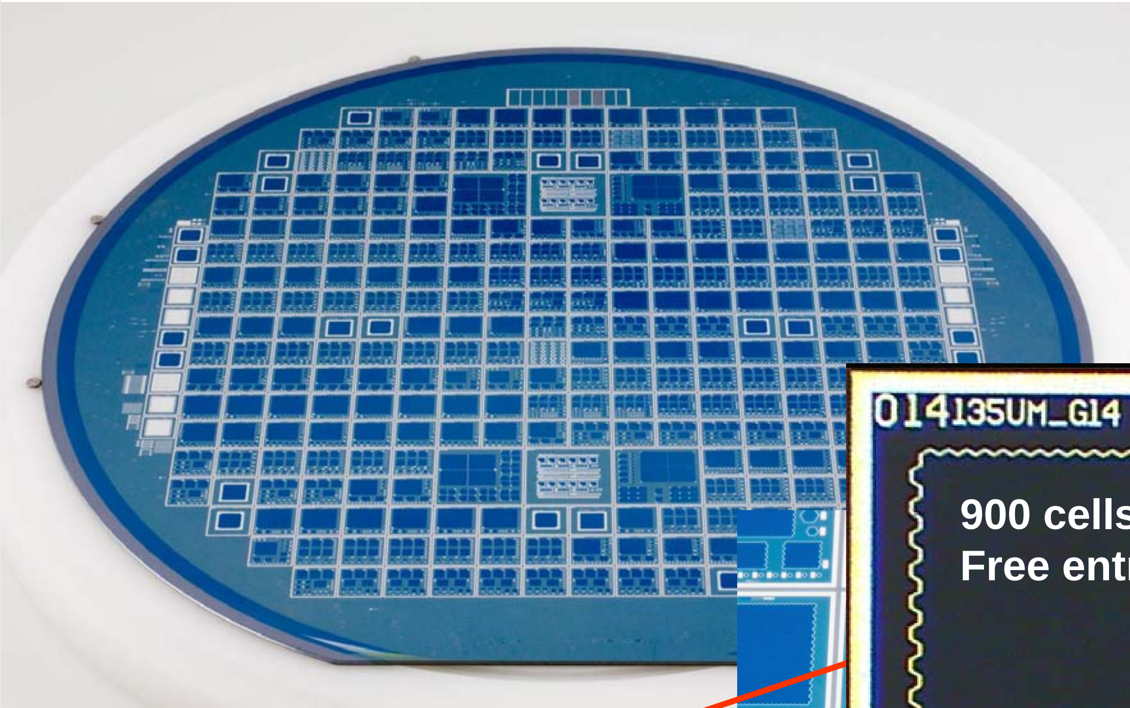
pitch: 90 -160 µm
different gap size

30x30 arrays

10x10 arrays



SiMPI prototype



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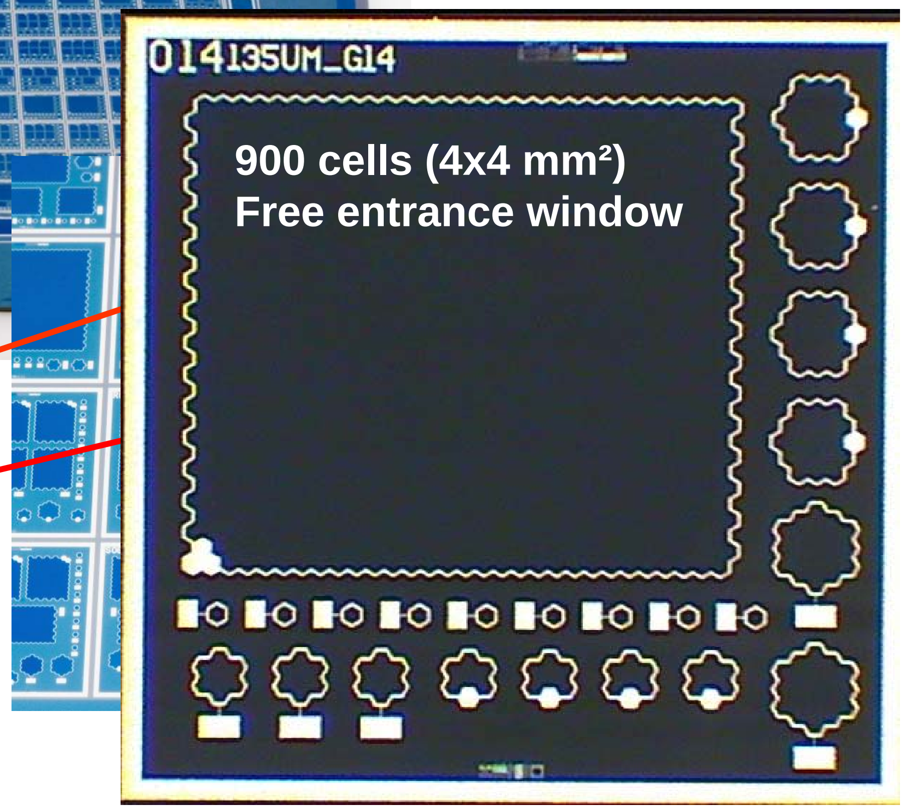

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SiMPI prototype

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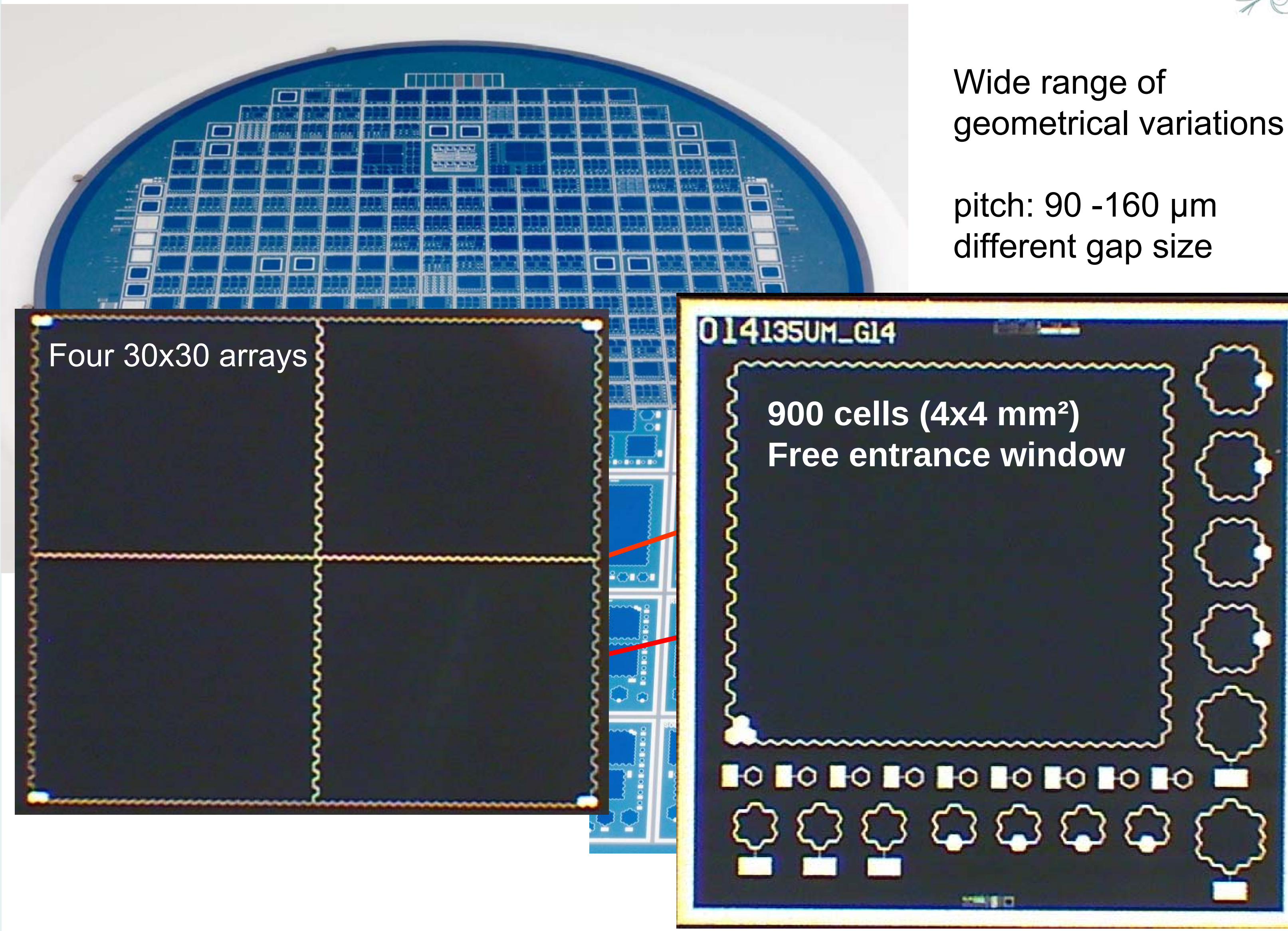

Advantages and Disadvantages

Advantages:

- no need of polysilicon
- no metal necessary within the array → free entrance window for light
- simple technology → lower costs
- inherent diffusion barrier against minorities in the bulk → less optical cross talk

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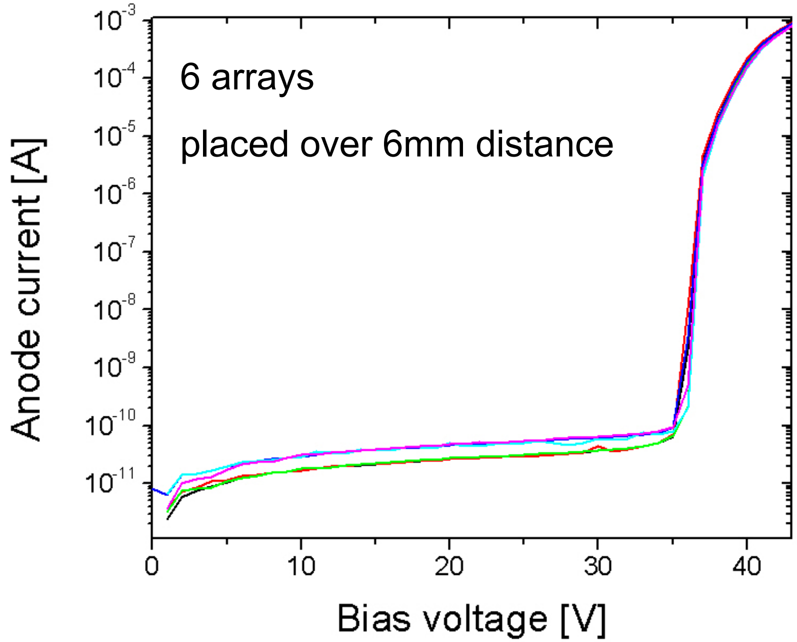
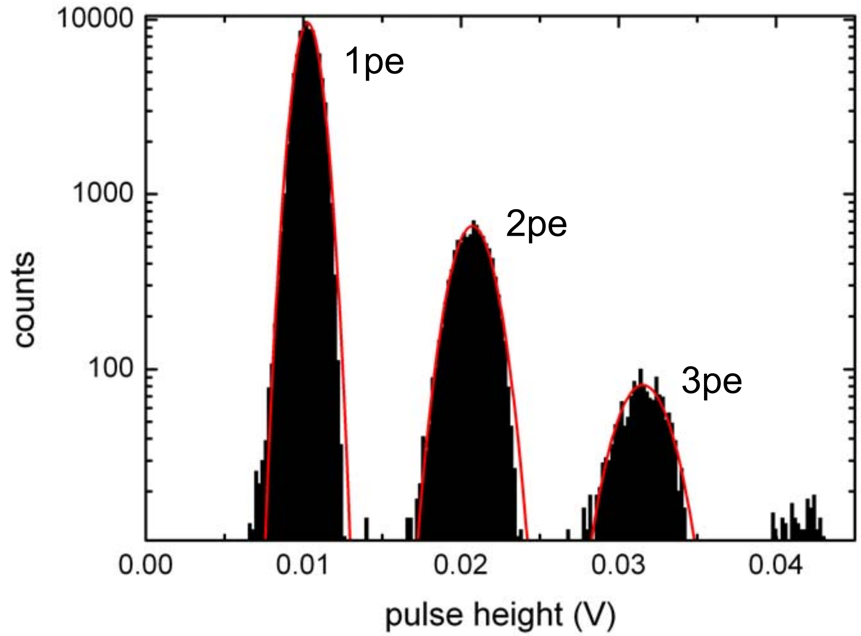
Drawbacks:

- required depth for vertical resistors does not match wafer thickness
- wafer bonding is necessary for big pixel sizes
- significant changes of cell size requires change of the material
- vertical ‘resistor‘ is a JFET → non-linear IV → longer recovery times

IV-measurement & amplitude spectrum



homogeneous breakdown voltage



10x10 array of 135µm pitch @ 253K

(only dark count spectrum)

Dark counts

due to non-optimized process sequence
~10MHz/mm² @300K for 4V overbias

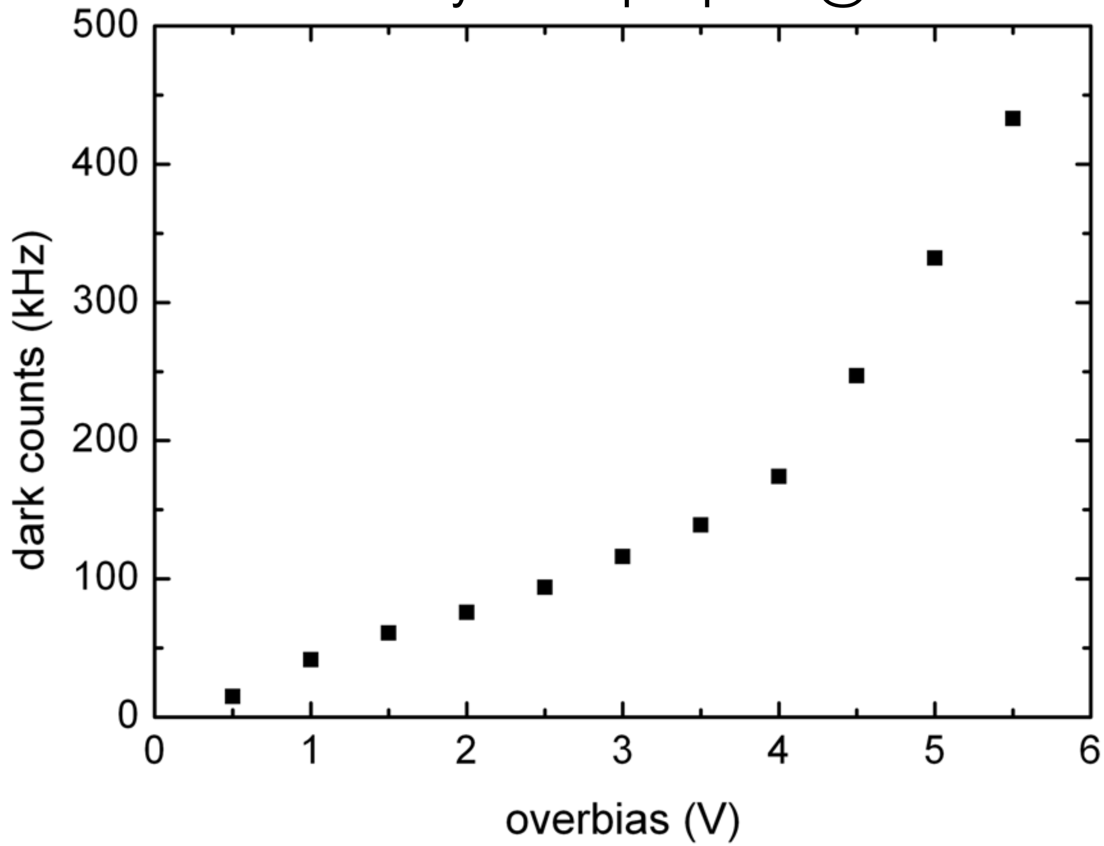
Thermal generation

→ cooling helps

normal operation up to
4V overbias @233K

overbias > 4V
→ non-quench condition

10x10 array of 130µm pitch @ 233K



Temperature dependence of quench resistor

Resistors designed for room temperature operation

→ limitation of operation voltage (non-quenching)

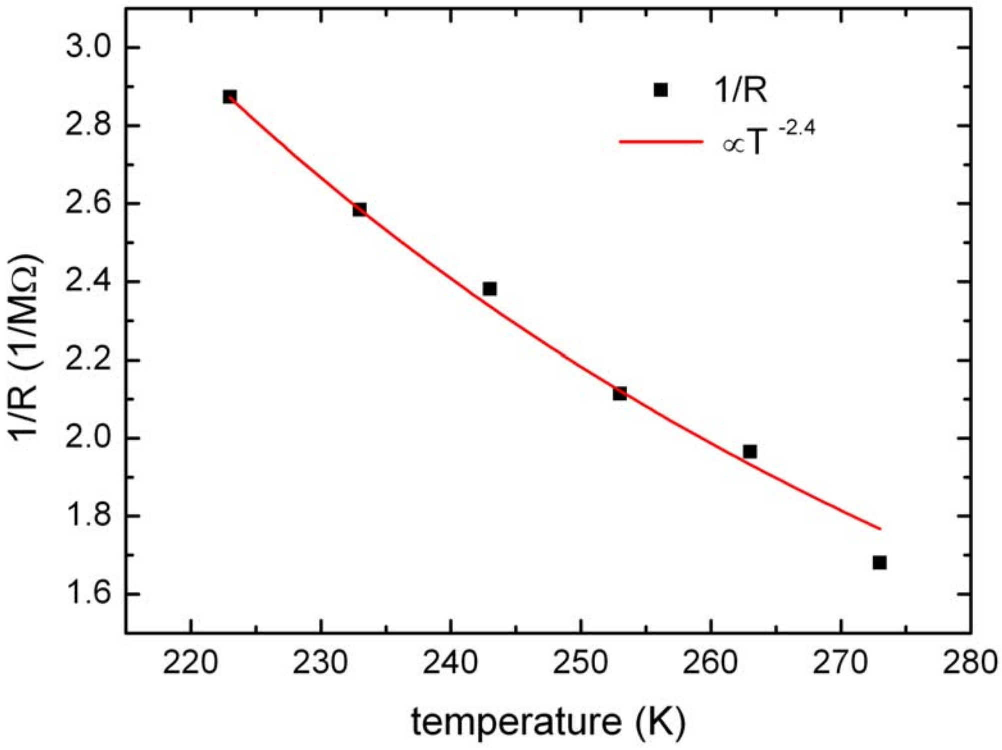
S. Cova et al., Appl. Opt. 35 (1996)

T (°C)	0	-10	-20	-30	-40	-50
R (kΩ)	595	509	473	420	387	348

$\tau = R_Q \cdot C_D$

mobility:

$\mu_n(\mathrm{Si}) \propto T^{-2.4}$



Optical cross talk

hot-carrier luminescence:

in an avalanche breakdown 10^5 carriers emit in average
1 photon with E > 1.12 eV
→ Trigger of neighbouring cells (fast & slow component)

A. Lacaita et al, IEEE Trans. Elec. Dev.,Vol. 4, 1993

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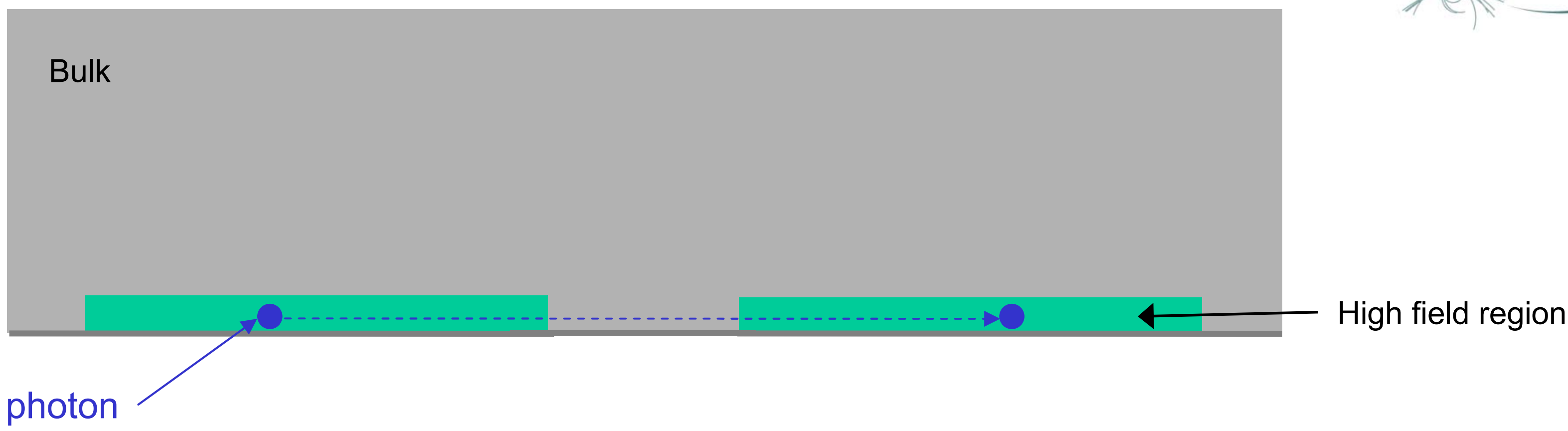

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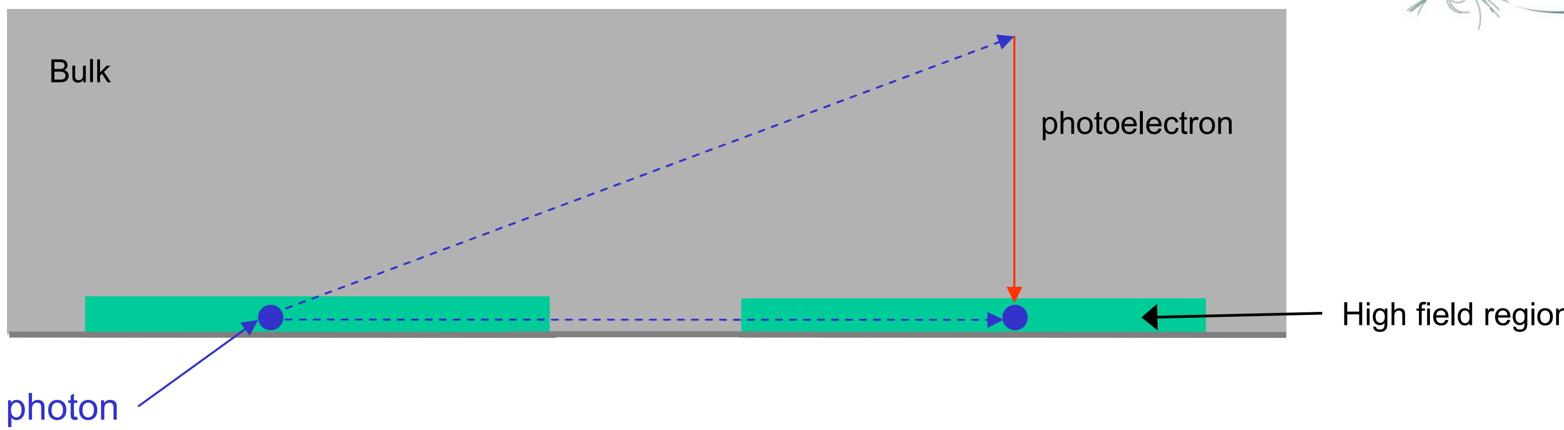

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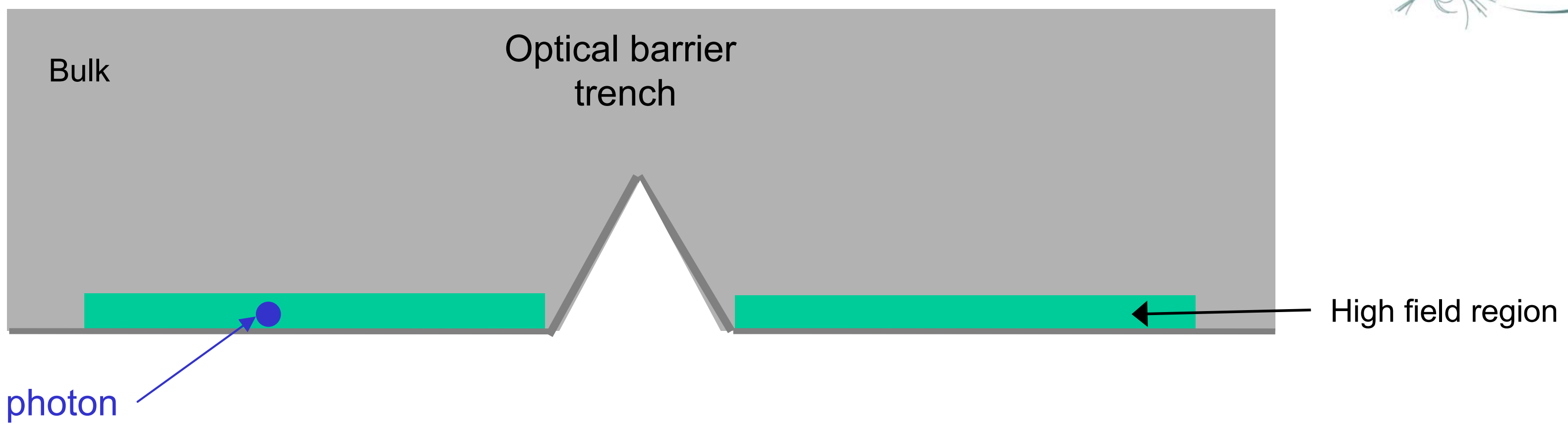

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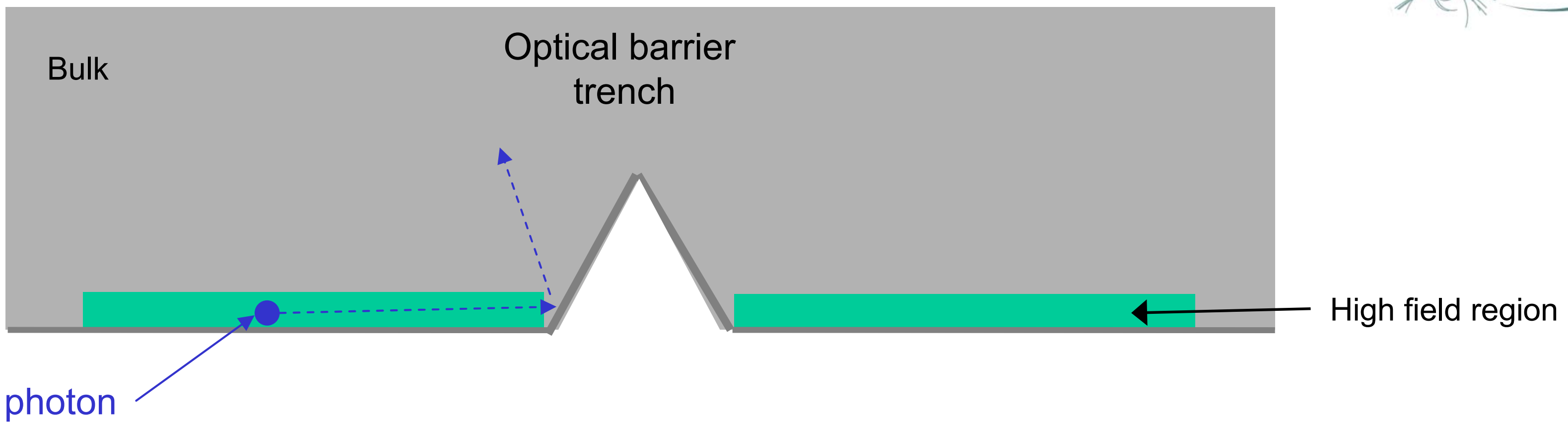

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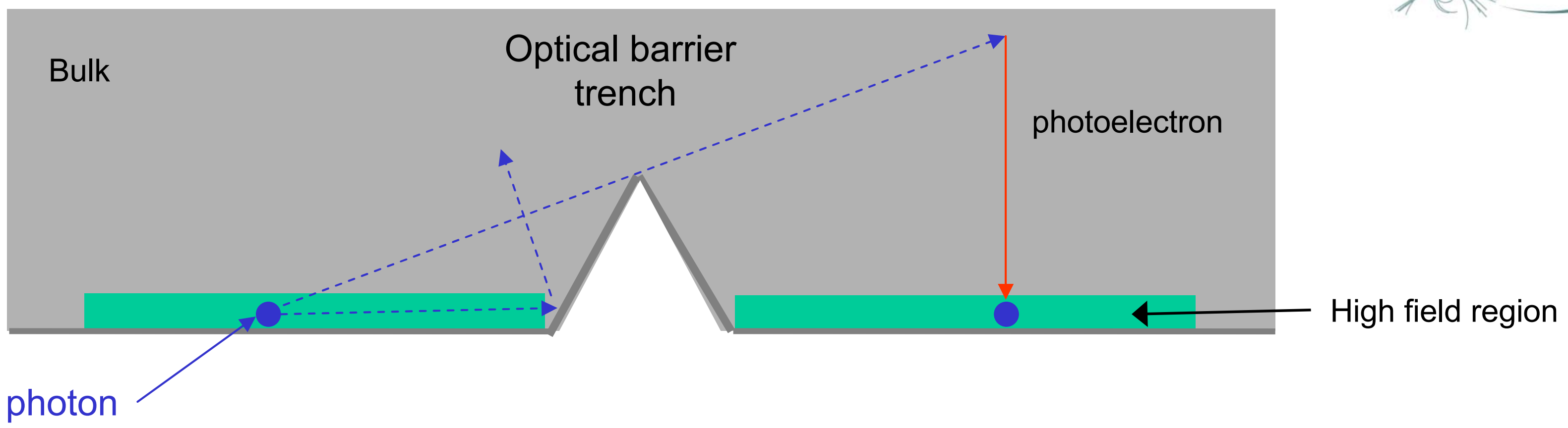

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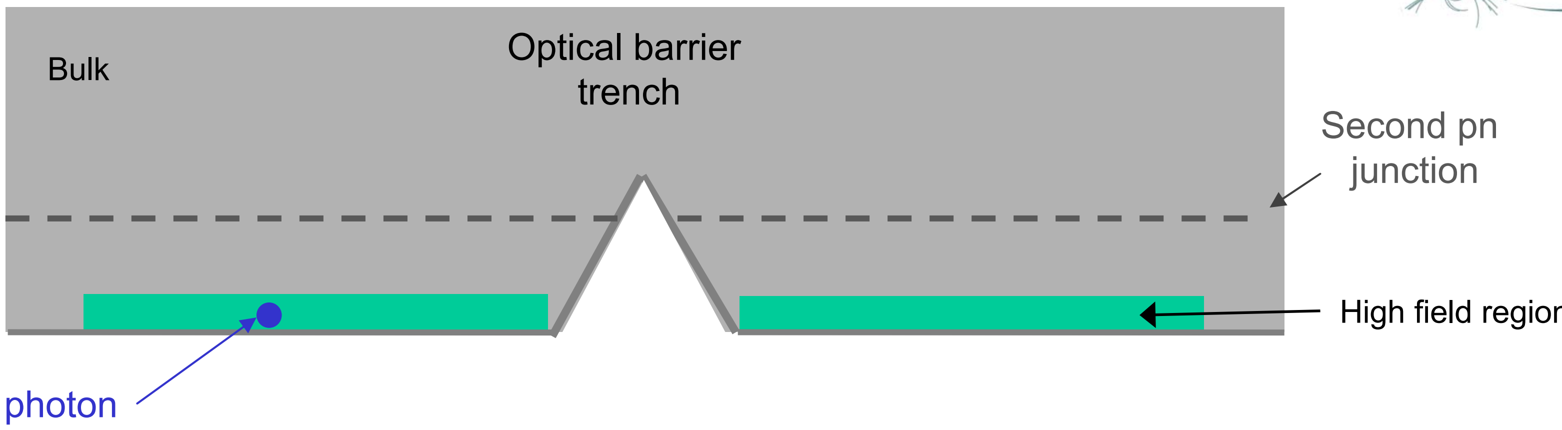

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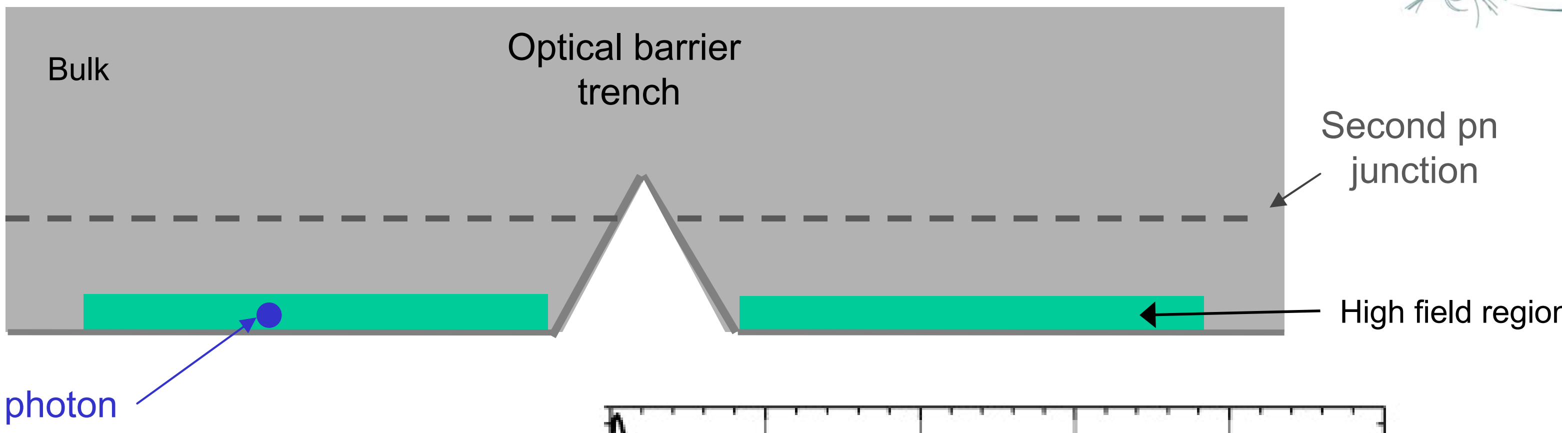
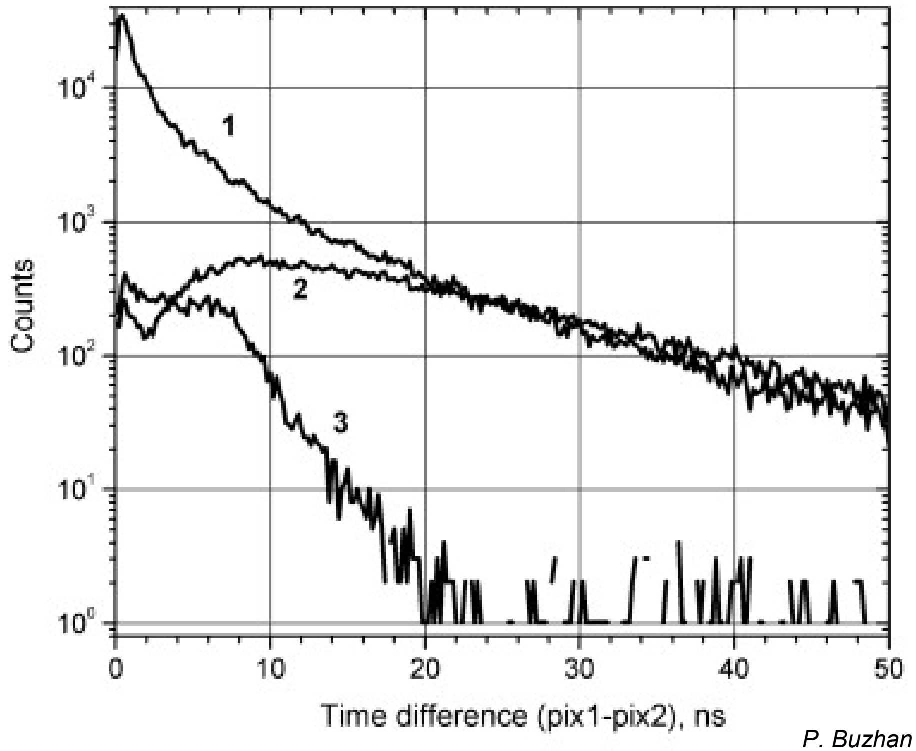


<ins>Distribution of time difference between two neighboring cells:</ins>

1: without optical crosstalk suppression

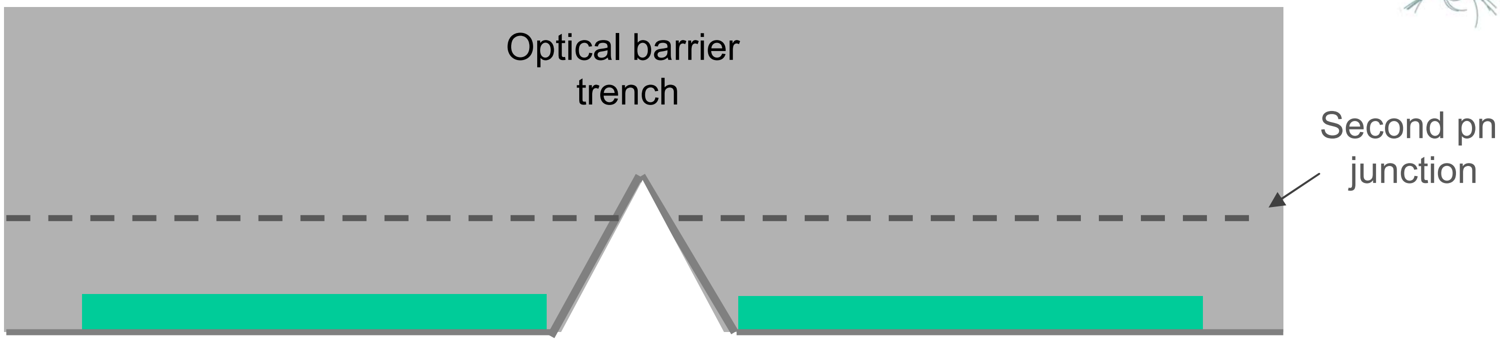
2: suppression by optical barrier

3: suppression by optical barrier and second *pn*-junction



P. Buzhan et al., NIM A 610 (2009)

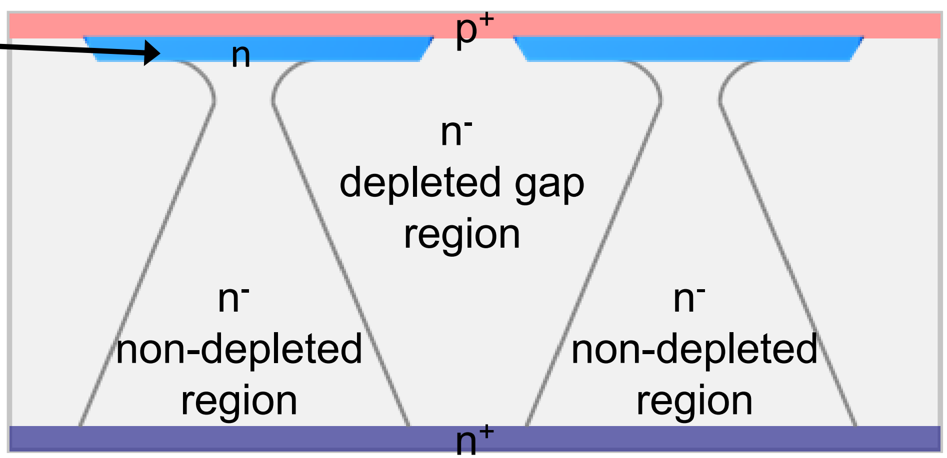
Optical cross talk



Internal anode as diffusion barrier:

Corresponds to second pn-junction

Inherent for SiMPl



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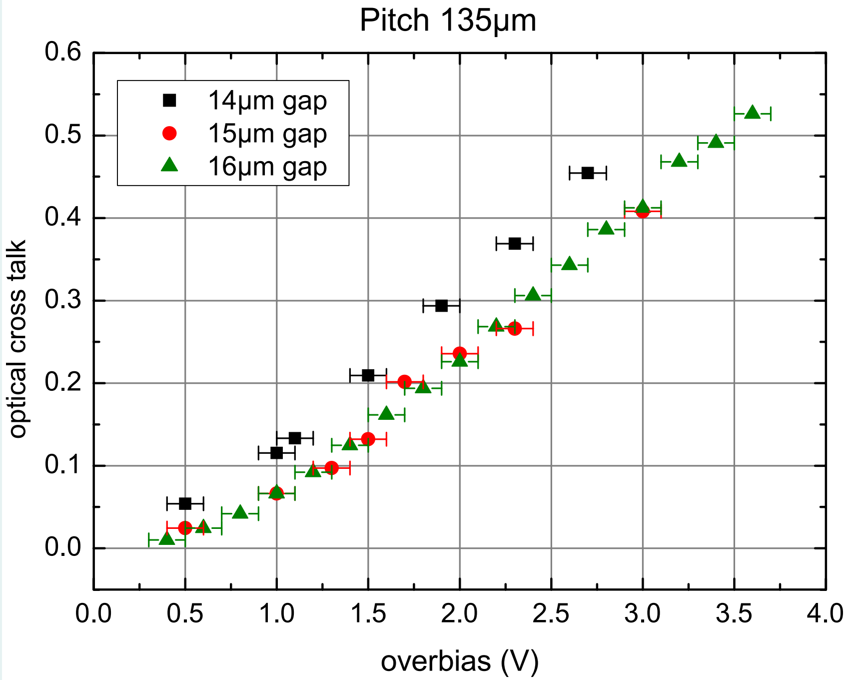
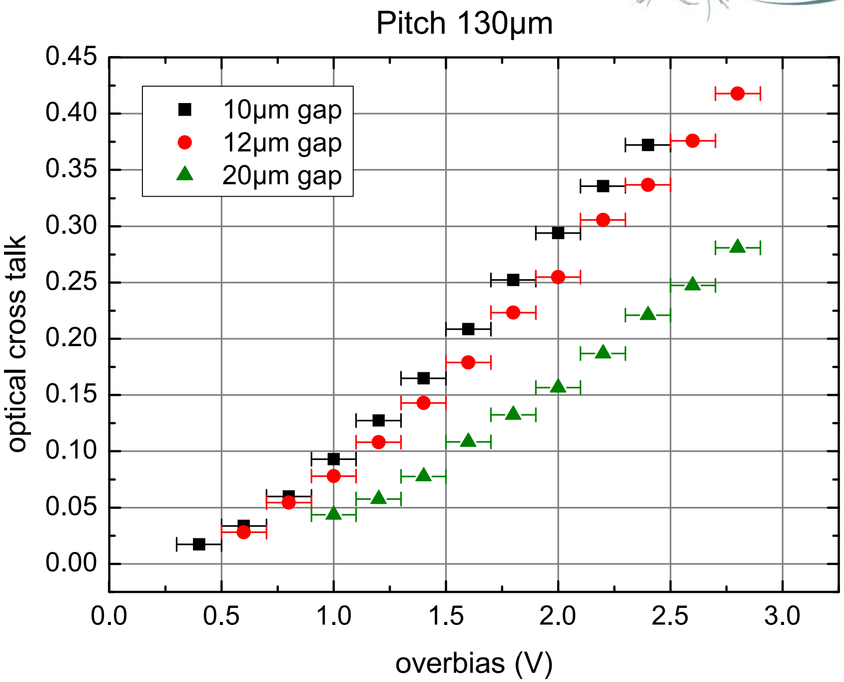




Increasing overbias

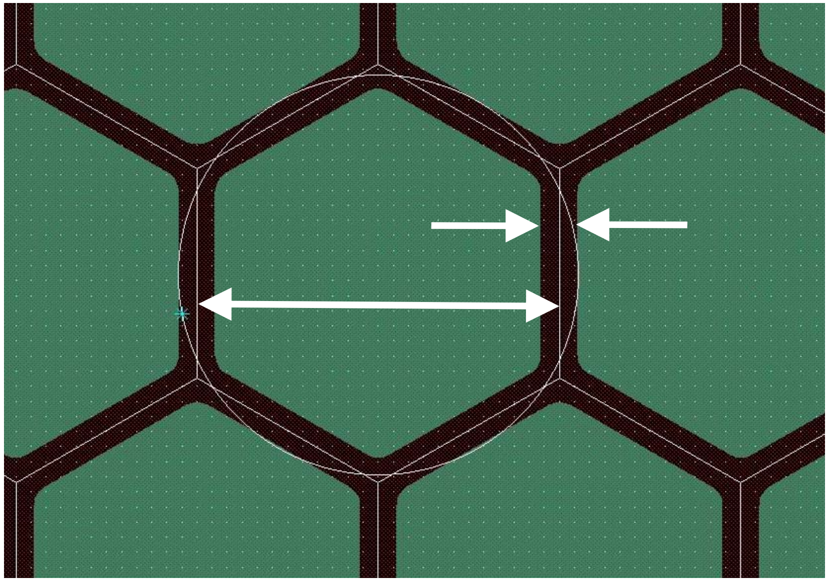
~ increasing gain

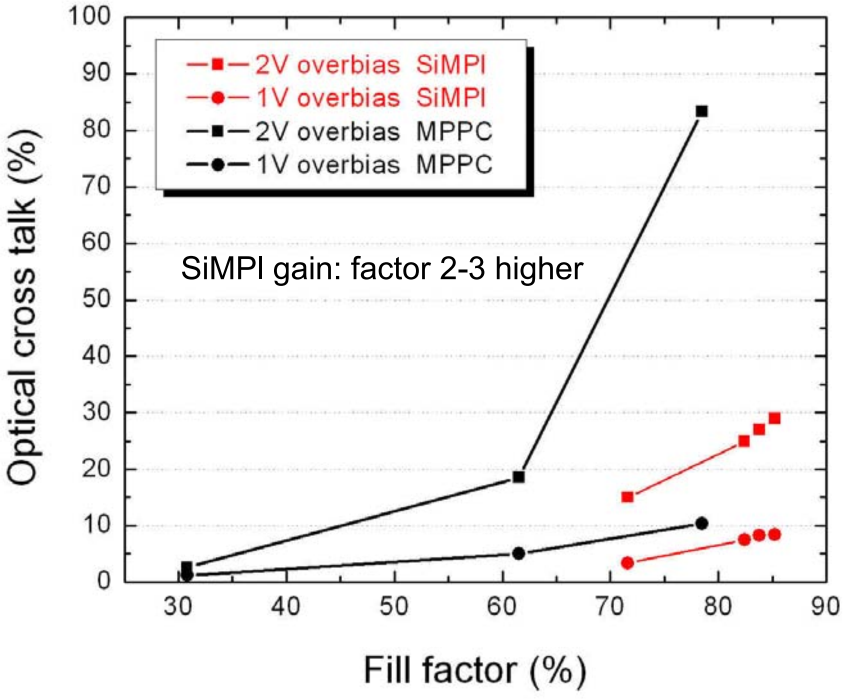
~ increasing trigger efficiency

Non-linear dependency on overbias

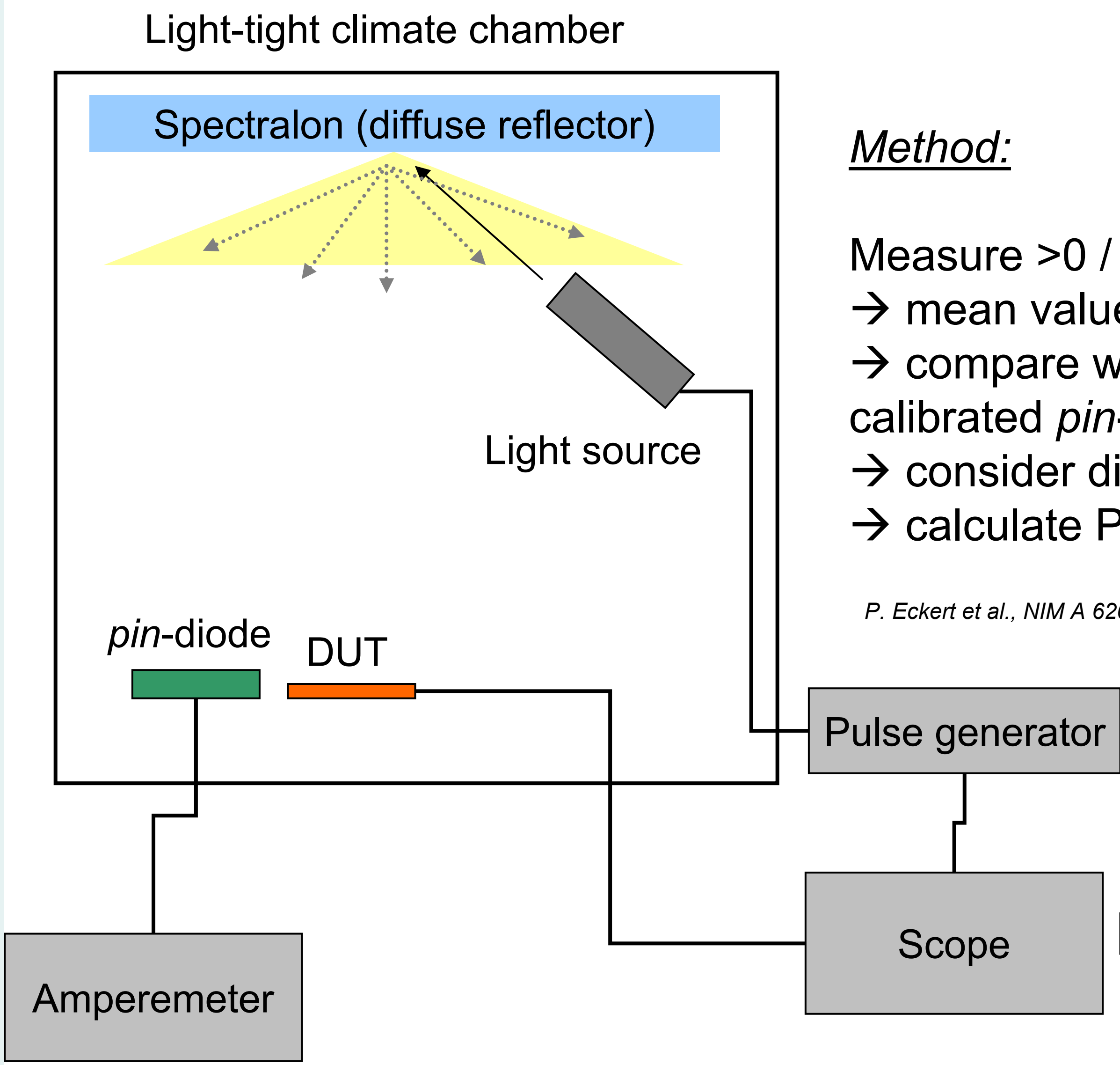
Optical cross talk

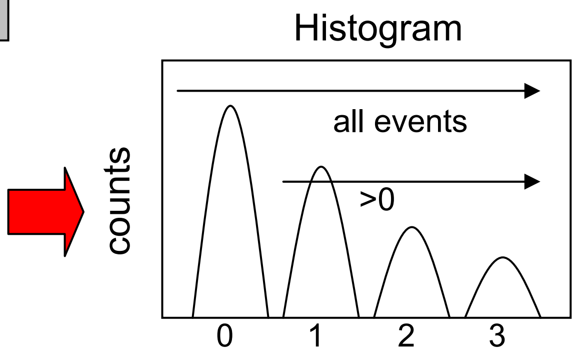
Pitch / Gap	Fill factor	Cross talk (2V V_{ob})
130µm / 10µm	85.2%	29%
130µm / 11µm	83.8%	27%
130µm / 12µm	82.4%	25%
130µm / 20µm	71.6%	15%





PDE measurements - setup





Method:

Measure >0 / all events
→ mean value (Poisson distribution)
→ compare with current from calibrated *pin*-diode
→ consider different areas
→ calculate PDE

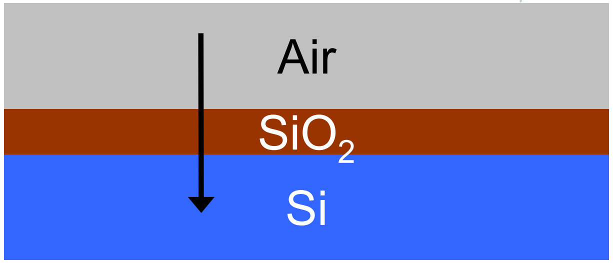
P. Eckert et al., NIM A 620 (2010)

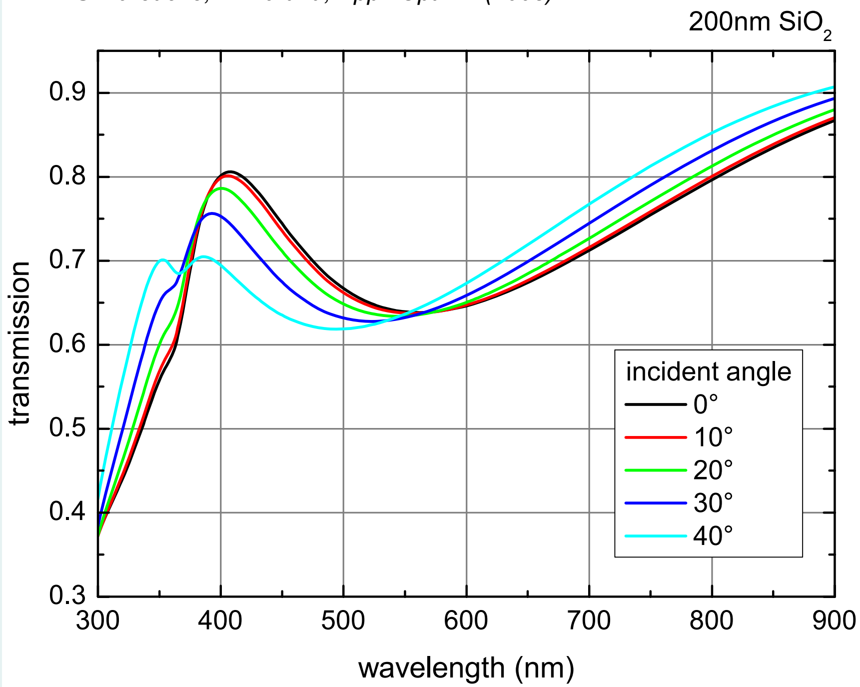
Transmission to silicon

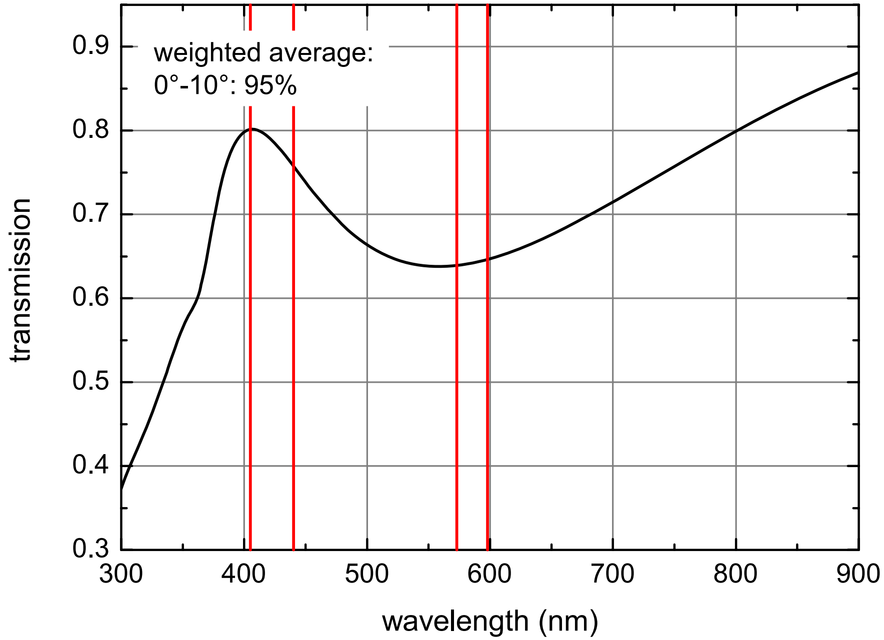
200nm SiO_2
Prototype: no optimized entrance window

Simulations with OpenFilters* for transmission into silicon

*S. Larouche, L. Martinu, Appl. Opt. 47 (2008)

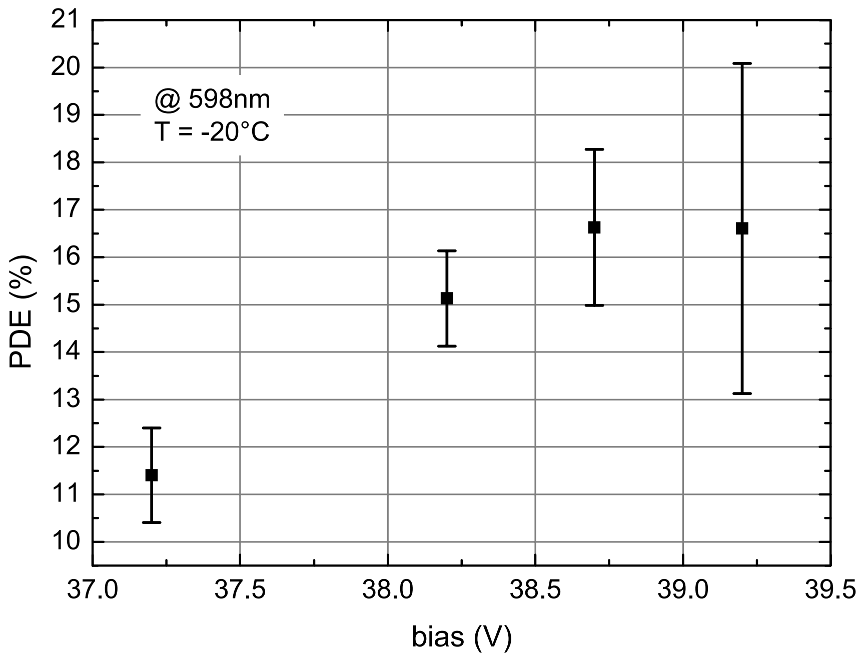


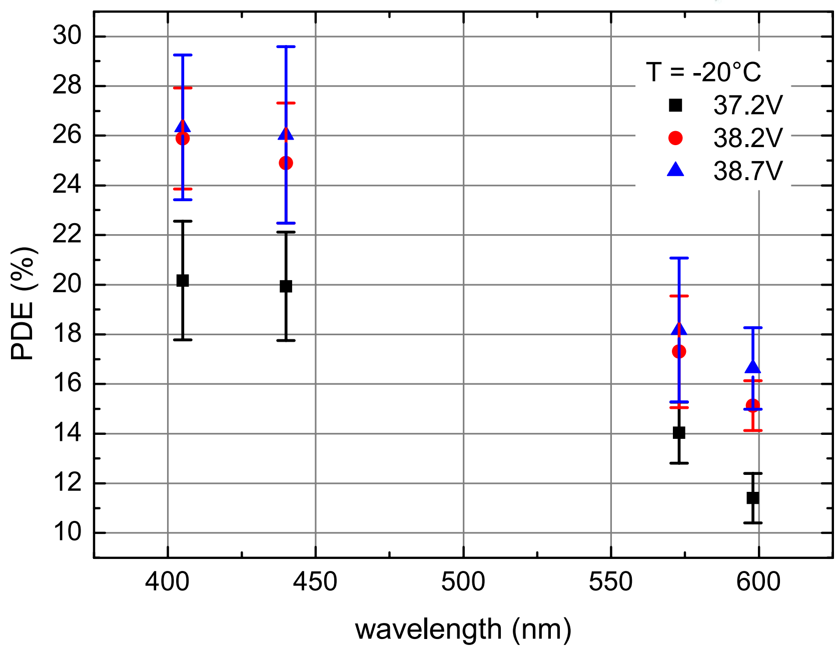




PDE measurements @ 405nm, 440nm, 573nm, 598nm

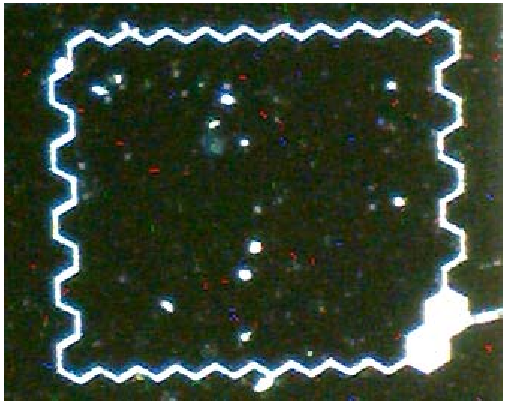
PDE: 130µm pitch, 20µm gap





Breakdown voltage: 35.2V
Fill factor: 0.716
Laser repetition rate: 0.5MHz
→ Max. recovery 2µs

Quenching limit → PDE not in saturation



Comparison: theoretical estimation - measurement

Theoretical estimation of PDE:
Geiger-Efficiency (GE) @ 2V overbias: ca. 50%

wavelength	405nm	440nm	573nm	598nm
transmission	0.80	0.76	0.64	0.65

Pitch/gap	Fill Factor	405nm		440nm		573nm		598nm	
		theo	meas	theo	meas	theo	meas	theo	meas
130/10	0.852	34%		32%		27%		28%	
130/11	0.838	34%		32%		27%		27%	
130/12	0.824	33%		31%		26%		27%	
130/20	0.716	29%		27%		23%		23%	

Comparison: theoretical estimation - measurement

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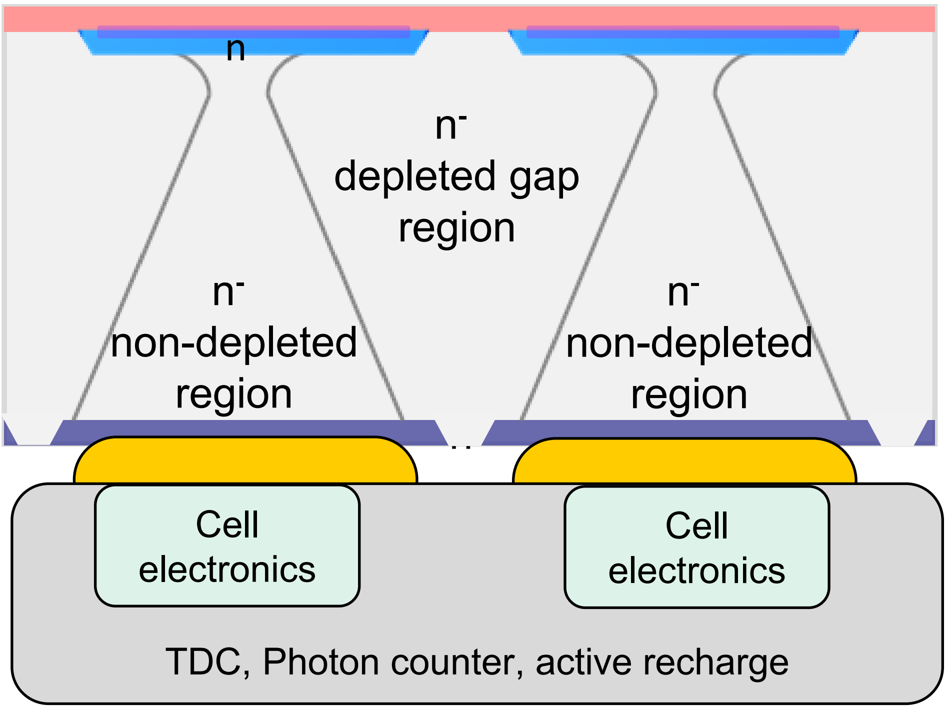
Estimation shows reasonable agreement with measurement results

Not taken into account here:
- Dirt on surface
- Wavelength dependency (depth of absorption → efficiency drops)

With optimization (85% GE & 90% entrance window) PDE of 65% easily achievable

Pitch/gap	Fill Factor	405nm		440nm		573nm		598nm	
		theo	meas	theo	meas	theo	meas	theo	meas
130/10	0.852	34%	26%	32%	24%	27%	14%	28%	12%
130/11	0.838	34%	29%	32%	28%	27%	14%	27%	13%
130/12	0.824	33%	25%	31%	23%	26%	14%	27%	13%
130/20	0.716	29%	20%	27%	20%	23%	14%	23%	11%

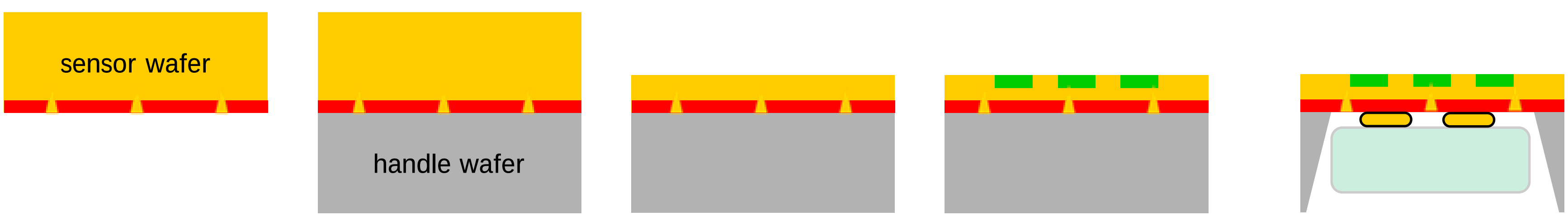
Next SiMPI generation – photon detection



Topologically flat & free surface

High fill factor

Sensitive to light



1. Structured implant on backside on sensor wafer
2. bond sensor wafer to handle wafer
3. thin sensor side to desired thickness
4. process SiMPI arrays on top side

Summary & Outlook

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New detector concept for SiPMs with quench resistors integrated into the silicon bulk

- no polysilicon resistors, no contacts necessary at the entrance window
- geometrical fill factor is given by the need of cross talk suppression only
- very simple process

Prototype production

- quenching works
- first results very promising
- problems encountered → optimization necessary

Further studies of the produced sensors (geometry dependence of the sensor performance, after pulsing, …) are ongoing

New production to reduce dark counts and implement small pixels

First concepts for single cell readout → next SiMPI generation

Thanks

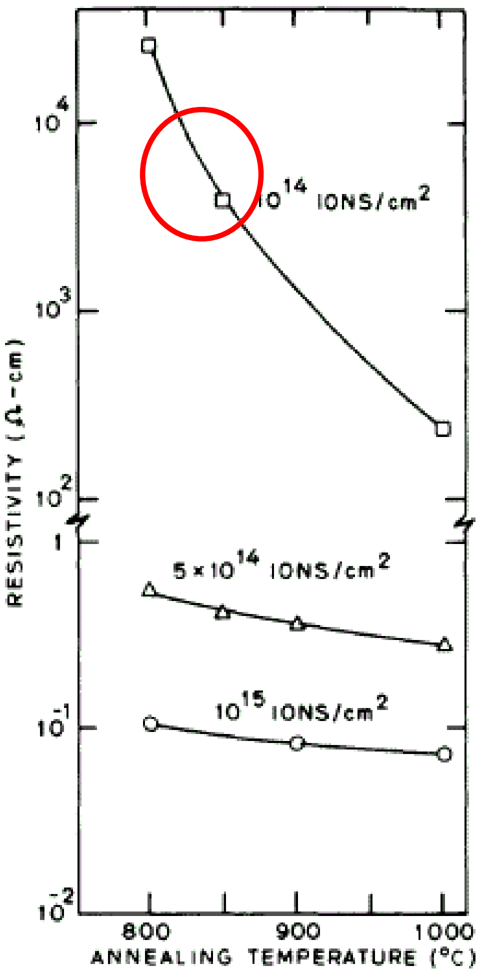
Polysilicon quench resistors

critical resistance range

→ rather unreliable process step

obstacle for incident light

→ fill factor decreased
→ limitation of detection efficiency



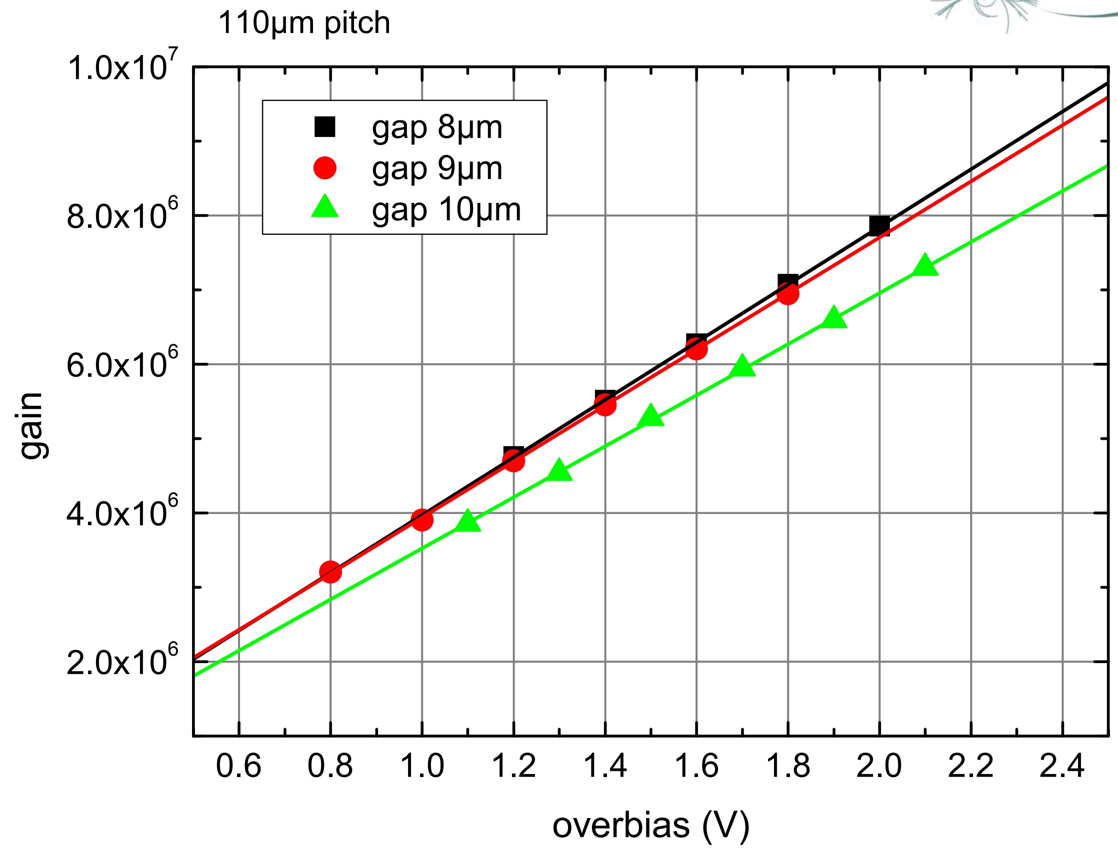
M. Mohammad et al.
'Dopant segragation in polycrystalline silicon',
J. Appl. Physics, Nov.,1980

Gain linearity

Expected:
linear with overbias voltage

Gain at 1V overbias

08 µm: 3.88 * 10^6
09 µm: 3.77 * 10^6
10 µm: 3.43 * 10^6



Gain linearity

pulse height ∝ Q

↓

$Q = e \cdot G = C \cdot \Delta U$

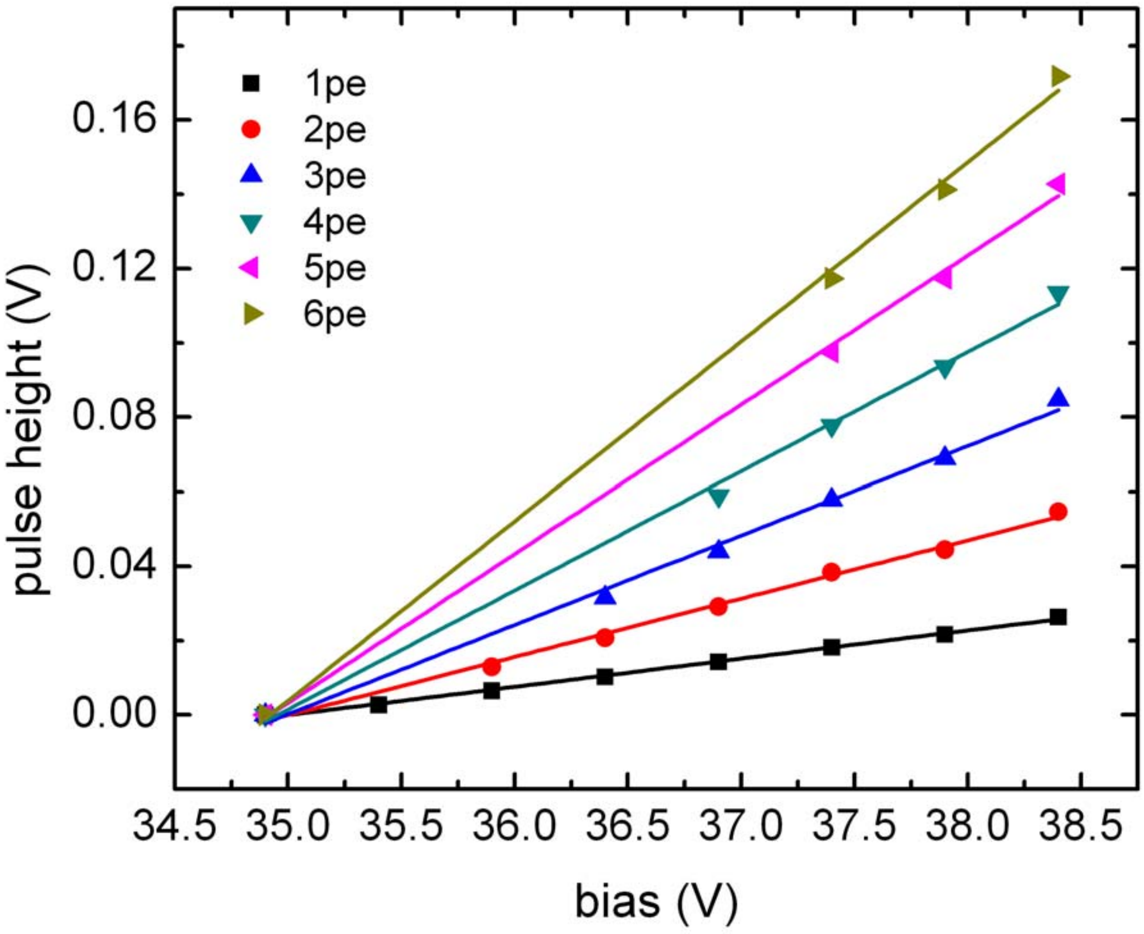
↓

linear

↓

normal operation

10x10 array of 135µm pitch @ 253K



Photon Detection Efficiency

PDE = quantum efficiency · fill factor · Geiger efficiency

- quantum efficiency: e-h pair generated in depletion layer, *QE(λ)*
- fill factor: fraction of active to total area of device
- Geiger efficiency: avalanche triggered by generated carrier, *GE(E)*

Optical cross talk & PDE

Pitch / Gap	Fill factor	Cross talk (2V V_{ob})
130µm / 10µm	85.2%	29%
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Photon Detection Efficiency estimation:

- Optical entrance window: 90% @400nm
- Geiger efficiency : 50% @ 2V overbias 85% @ 6V overbias

Pitch / Gap	Fill factor	PDE	
130µm / 10µm	85.2%	39%	65%
130µm / 11µm	83.8%	38%	64%
130µm / 12µm	82.4%	37%	63%
130µm / 20µm	71.6%	32%	55%

Prototype production - overview

Devices under investigation:

Pitch (µm)	Gap (µm)	Gain (estim)	Fill Factor
160	10	1.069E+07	0.879
135	13	7.074E+06	0.817
135	14	6.958E+06	0.803
135	15	6.844E+06	0.790
135	16	6.730E+06	0.777
130	10	6.844E+06	0.852
130	11	6.730E+06	0.838
130	12	6.617E+06	0.824
130	13	6.506E+06	0.810
130	14	6.395E+06	0.796
130	20	5.750E+06	0.716
125	9	6.395E+06	0.861
125	10	6.285E+06	0.846
120	8	5.961E+06	0.871
120	9	5.855E+06	0.856
110	8	4.944E+06	0.860
110	10	4.752E+06	0.826
110	12	4.564E+06	0.794
100	5	4.289E+06	0.903

Breakdown voltage:

dU/dT = 35.5 mV/K

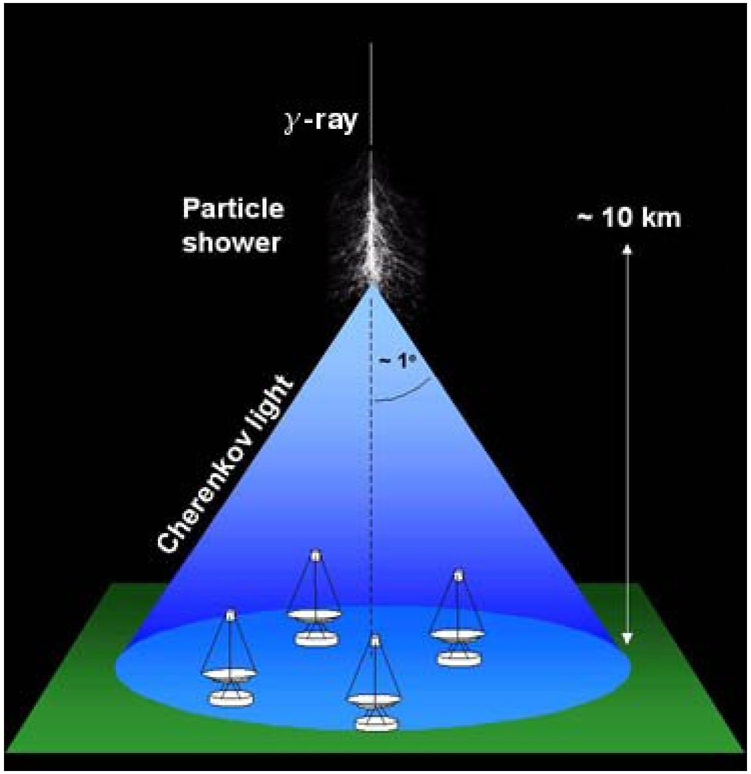
Fill Factor:

0.71 – 0.90

Gain @ 1V:

4.23 – 10.69 $*10^6$
(Estimated)

Cherenkov Telescope Array



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