New Real-time control system R&D for Einstein Telescope

Virgo Pisa internal workshop – May 22-23, 2024, INFN Pisa

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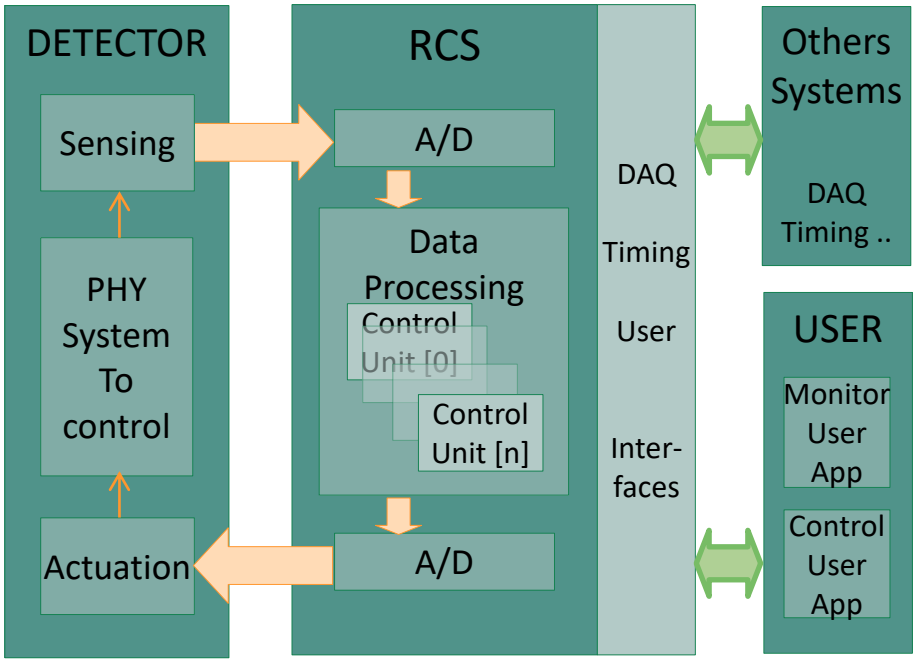
Outline

Many activities involving Electronics/SW design in Pisa :

- New RCS targeting Einstein Telescope requirements
    - HW design – custom boards
    - FW design – protocols for FPGA to other boards communications
    - SW design – HW control low level software, data monitoring and processing
- Development of a low frequency “noise-meter” portable instrument for DAC characterization
- Other activities :
    - Active platform and testbenches in Virgo lab – see Francesca Spada talk
    - New accelerometer with interferometric readout – see Alberto Gennai talk

Real-time Control System (RCS)



Real-time control is the ability of a closed-loop system to:

- Collect data from sensing elements.
- Process that data and extract actuators driving signals.
- Update the system, as wanted, within a defined time window.

RCS is a very complex object which needs to handle multiple control units, usually spread in space, their inter-communications and their communications with users and other systems.

Strong requirements needed for processing loop time (Max bandwidth, System stability).

RCS needs Hardware, Firmware and Software development.

RCS System Definition

Goal : Architecture definition and development of a general-purpose Real-time Control System (RCS) for ET initial phase. Two approaches :

DSP + FPGA data processors – "***Katane***" project

GPU + FPGA data processors – "***Zancle***" project

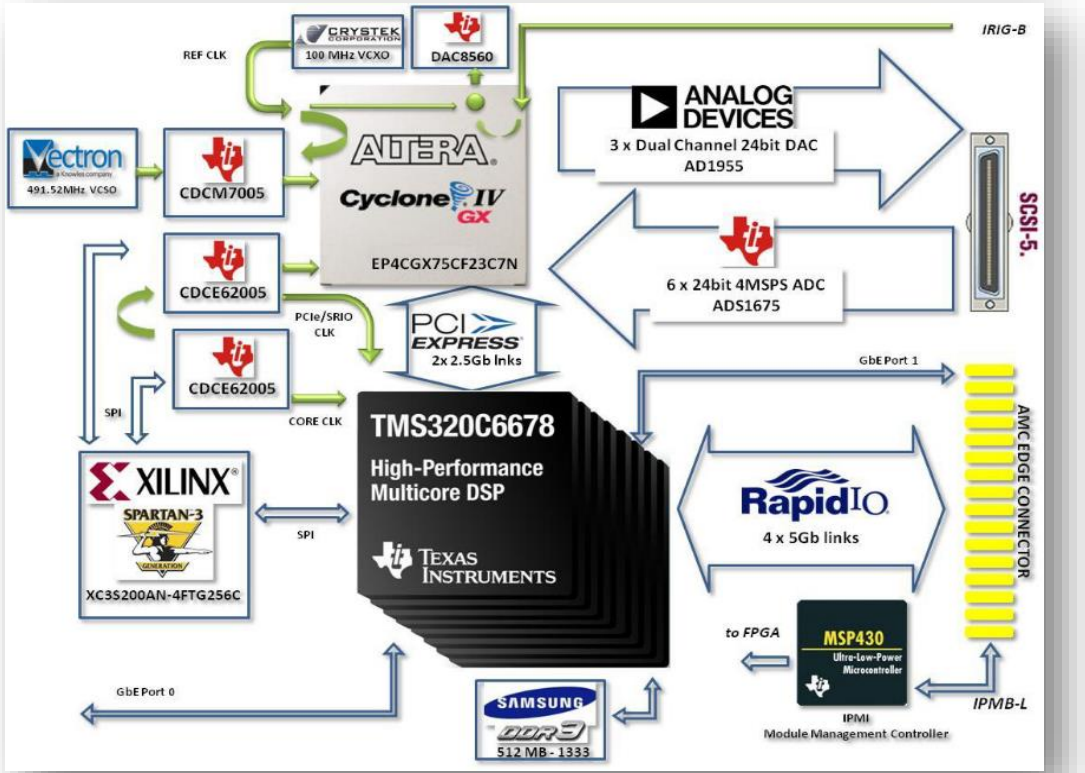
- FPGA devices interface with AD/DA converters in both views. FPGAs are very powerful objects for parallel data processing and high speed and high bandwidth data transfer.
- Need to perform high resources consuming operations on data → Powerful processing core that can implement complex algorithm with low and deterministic latency. Cannot use standard CPUs.

- DSPs are very powerful objects and optimized for high consuming resources calculus.
- Pisa experience with DSP processors. (AdV)

- Research interest in ML for control algorithms.
- Very high computing power in GPUs.

“Katane” – Starting Point (1)

AdV control data processor board



System based on a single type of board with FPGA and DSP.

It receives analog signals from sensors, converts them to digital using high precision ADCs, processes converted data and drive actuators according to results of elaboration.

Each board equipped with:

- 8 core DSP TMS320C6678 (~20 GFLOPS/core)
- 6ch DAC (24bit 320 kSPS)
- 6ch ADC (24bit, 3.84MSPS)
- Altera FPGA

“Katane” – Starting Point (2)

AdV Superattenuators (SA) control system

Boards are organized in crates, which serve for mechanical support, data inter-boards communication, network and power distribution, cooling etc…

Crates :

- Based on a MicroTCA standard but customized. Boards are over-sized, so a modified crate is needed. (No possibility to insert Rear-Transition-Modules inside the crate)
- Contain up to 12 boards (usually 6-8) per crate.

Each SA needs two local control unit (2 crates).

SA are spatially spread along the detector.

Complex interconnections. (135 processors)

“Katane” – HW Architecture

Use of MicroTCA (MTCA) standard, specifically MicroTCA.4. :

- It supports high-speed data communication protocols such as Serial-RapidIO and PCIe, enabling fast and efficient data exchange
- It provides mechanisms for precise timing and synchronization
- Modular division ensuring flexibility, future proofing, easier maintenance, simpler developments of single modules.

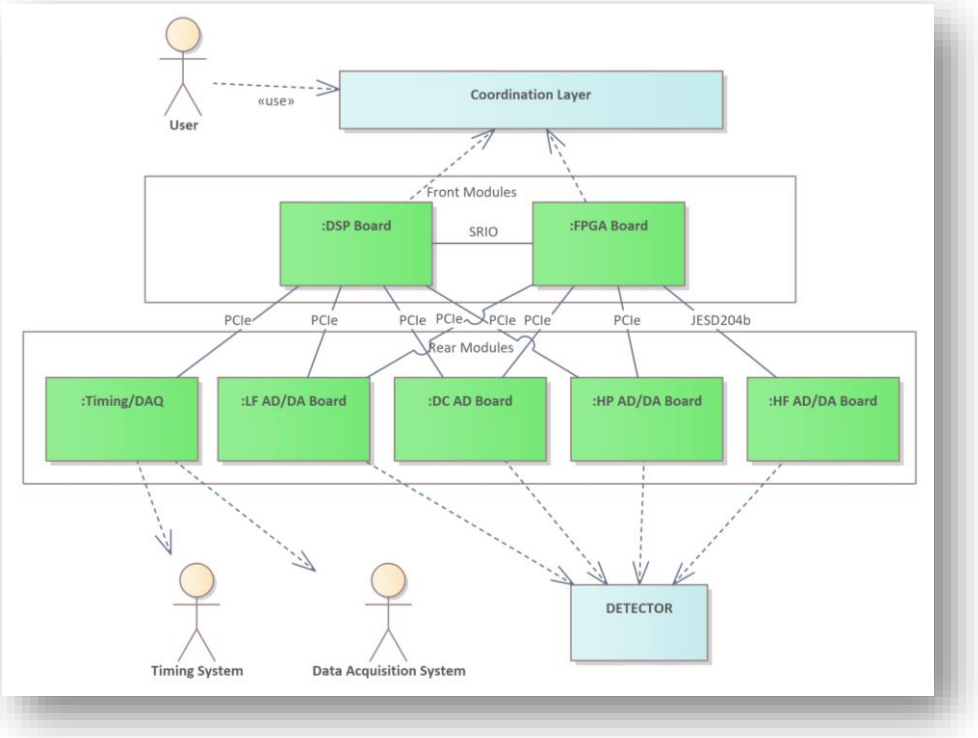
Cards can be inserted both in the front, referred to as Front AMC (FA), and in the rear, known as Rear Transition Module (RTM). Communication through a Back-plane.

Front AMCs :

- FPGA board
- DSP Board

RTMs :

- LF (Low Frequency) AD/DA conversion
- HF (High Frequency) AD/DA conversion
- Timing/DAQ
- Others… (e.g. High-power ADCs/DACs, Monitoring)



“Katane”– HW on-going Activities

HW design :

- Design has started for many boards in the system and progressed at an advantage stage for some of them.

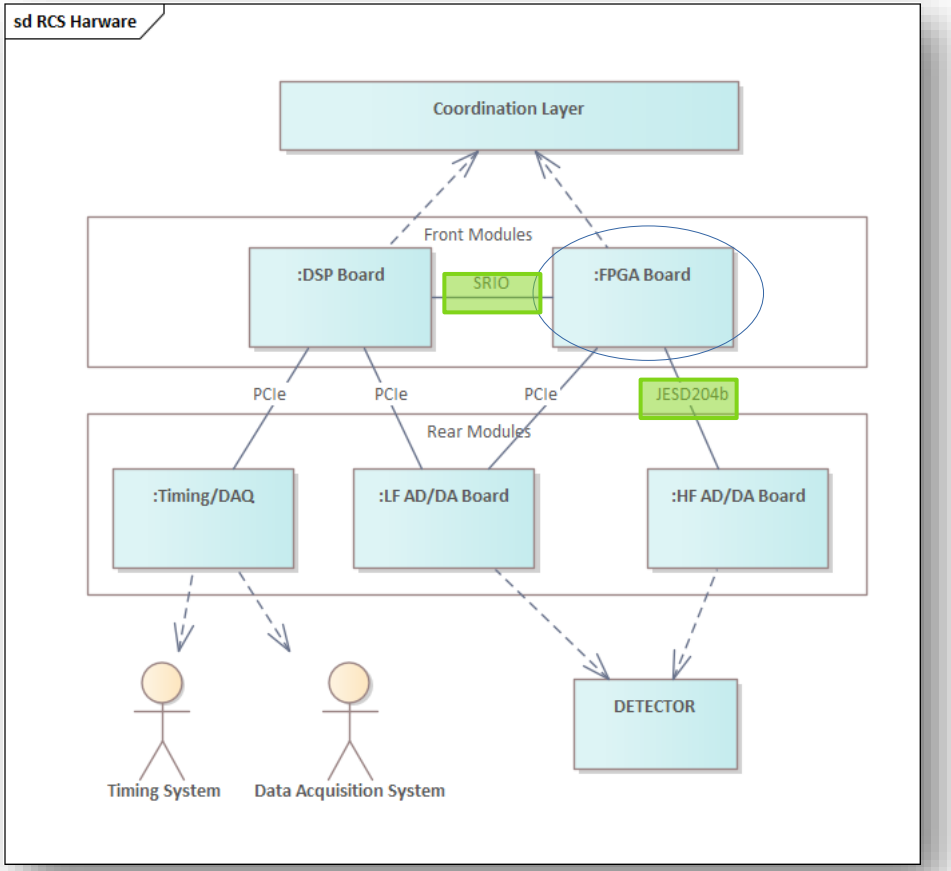
FW design :

Several protocols need to be implemented and tested on the pre-processing FPGA board to interface with other modules in the system. Lot of work has been done :

- Implementation of the firmware needed for the FPGA board to interface HF ADCs and DACs using JESD204B protocol. (Done – Tested using commercial EVMs)

- Implementation of the firmware needed for the FPGA board to interface DSP board using Serial rapid IO protocol. (Done – Tested using commercial EVMs and AdV crate)

And… lot of work still need to be done!



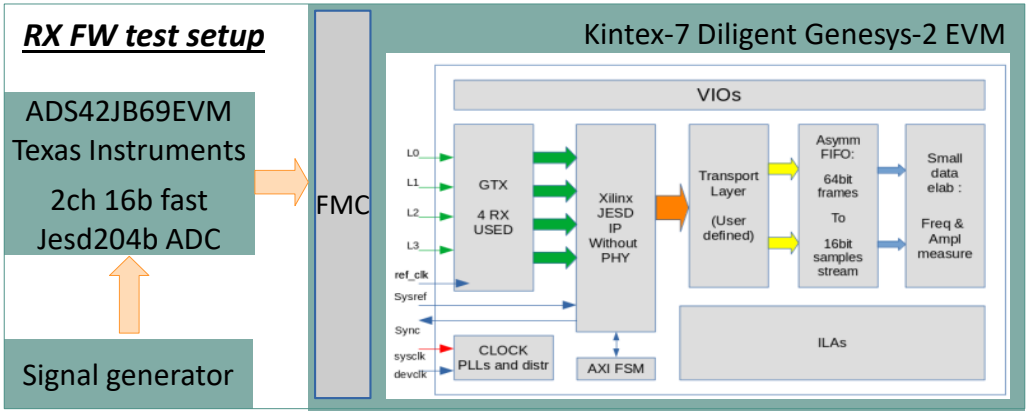
“Katane”– JESD204B protocol FW

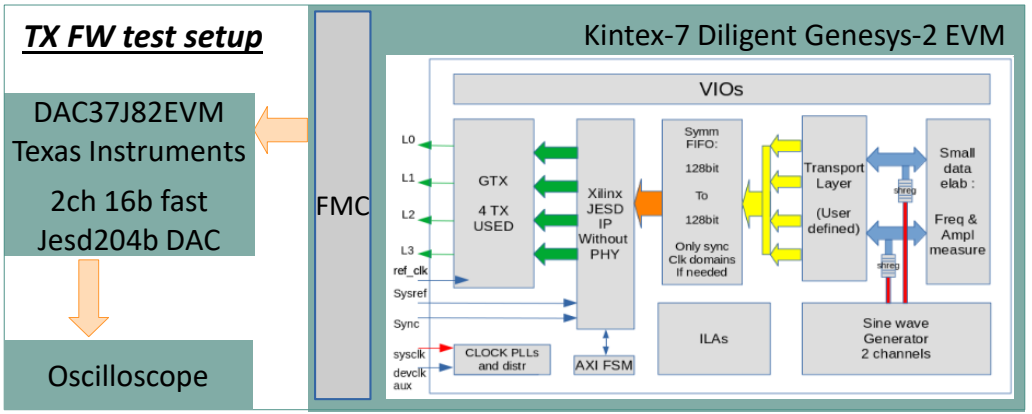
JESD204B is a low level high-speed serial data interface standard to enable efficient and reliable data transfer between ADCs and DACs and digital processing devices. It features:

- **Multi-lane and Multi-device support** : data from a JESD converter is generally divided and mapped across several lanes and a JESD link can manage several devices.
- **Serial data rates up to 12.5Gbps per lane**. Based on 8b/10b encoding (CDR, DC balancing).
- **Multi-lane** and **Multi-device synchronization**
- **Deterministic link latency achievable**

A jesd204b link can consists in several lanes from several devices which have to be managed and synchronized.

JESD204b timing is crucial. RX and TX must use a clock coming from a shared source to work properly.

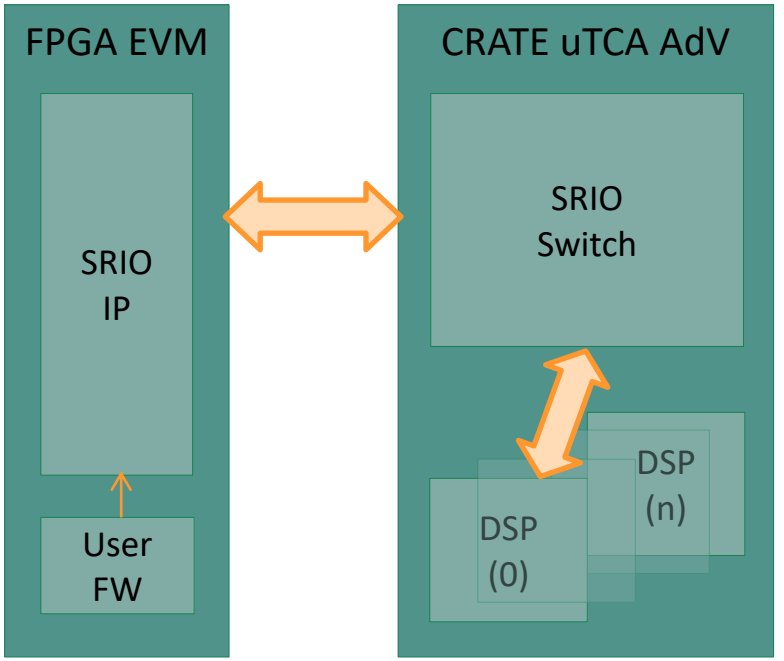




“Katane”– SRIO protocol FW

Serial RapidIO (SRIO) is a high-speed, low-latency, point-to-point, packet based serial interconnect technology designed for communication between processors, memory, and peripheral devices in embedded systems and networking applications.

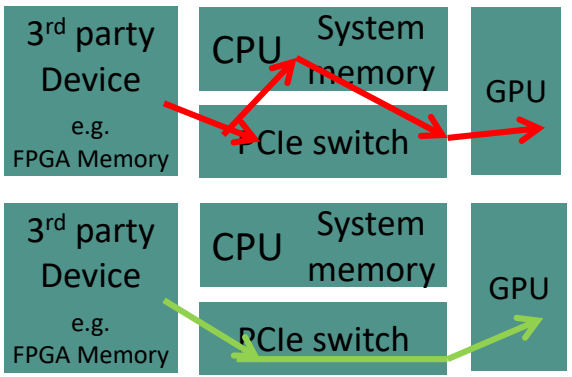
- SRIO typically comes in lane configurations ranging from 1x to 10x or more, with each lane supporting high data rates (e.g., 1.25 Gbps to 25.78125 Gbps).
- Point-to-Point Topology: similar to PCI Express (PCIe), SRIO uses a point-to-point topology, where each link connects two specific endpoints directly.
- Low Latency: Serial RapidIO is designed for low-latency applications, such as those in real-time signal processing, telecommunications, and data-intensive computing. Its point-to-point architecture and packet-based protocol contribute to reducing communication delays.



“Zancle”– Idea and related Activities

MAIN IDEA : Use of GPU based processors in order to take advantage of the high computing power of these objects.

- Complete architecture vision of this second project not yet designed, but the aim is to employ cost-effective PCIe based systems designed for the consumer market.
- Main activity for this project on the recent future will be try to understand the feasibility of the GPU use for real time control systems.
- Computing power could be clearly enormous, but what about total data acquisition and processing ***delay?*** → GPU/CPU interactions and data exchange could be too time consuming for RCS applications.



A **NVIDIA Quadro rtx 4000 and ALVEO Xilinx FPGA module** will be used for testing. First goals**:**

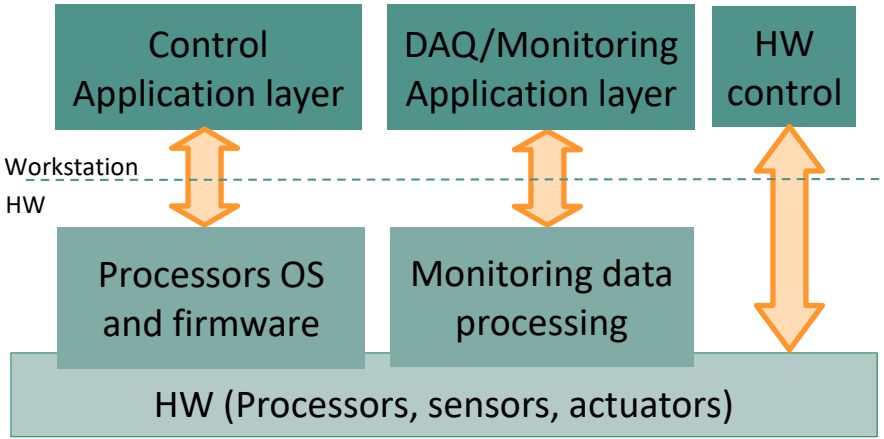
- Implement FPGA/GPU Direct-Memory-Access “DMA” connections and see if data transfer time is suitable for RCS.
- Implement simple control algorithms.

RCS software development

Independently of the HW architecture, a huge time and man-power consuming task is for sure the Software development.

The software needed for a RCS is complex and stratified in several layers :

- A Control application layer, which aim is to permit the user to implement the control algorithm on HW processors. (Control workstation “CW”).
- A DAQ/Monitoring application layer. (CW)
- A middleware layer, which aim is to conceal the HW and digital system's intricacies and facilitates algorithm development and user interactions. (e.g. DSP OS and firmware, monitoring data processing and transfer layer – on Processors).
- Low level software to control board HW configurations. (e.g. FPGA programming, clock synthesizers settings – on CW)

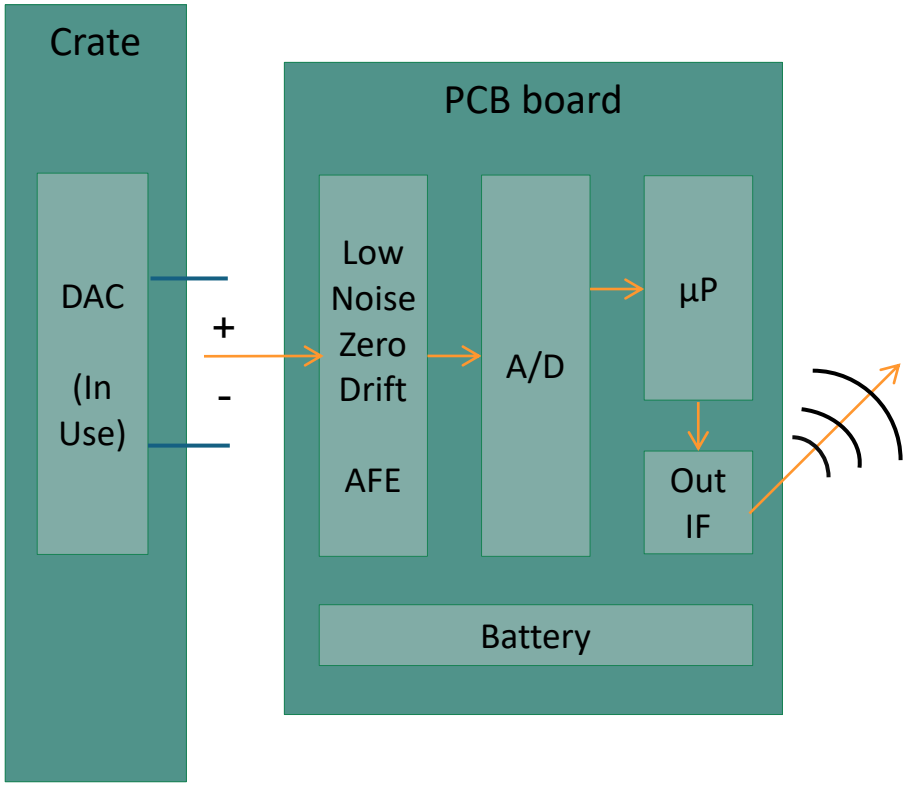


Software final architecture definition is in progress.

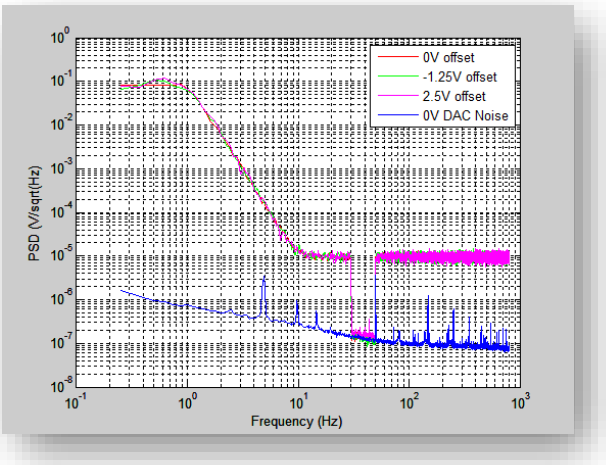
Parts of software are in development and testing :

- Monitoring application layer and its respective middleware part has been testing on DSP boards in Pisa test setups. (Scope and FFT)

TranquiTone Analyzer



GOAL : Development of a PCB able to measure the noise of an electronic device, such as a DAC converter, down to tenths of mHz, to help with R&D for LF enhancements.



Requirements :

- Bandwidth
  [10 mHz – 1KHz]
- Small signal amplitude to measure (see plot)

IDEAs :

- Use of chopper techniques to overcome issues due to 1/f flicker noise in standard electronics
- Development of an easy-to-use portable device with battery power supply and wireless output data interface.

Thanks for your attention!

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Backup slides

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“Katane” – HW Architecture (2)

MicroTCA.4 benefits:

- It supports high-speed data communication protocols such as Serial-RapidIO and PCIe, enabling fast and efficient data exchange between cards in the system.
- It provides mechanisms for precise timing and synchronization. Essential in applications requiring coordination between multiple cards and devices.
- Future-Proofing: the modular and open nature of the MicroTCA.4 standard allows for upgrades and advancements in technology without requiring a complete system overhaul.

This modular division also ensures :

- Greater flexibility - this way, we can keep the processors while changing the converters in view of designing of a general-purpose RCS.
- Easier maintenance
- Simplifies the system's blocks development